Analog Power AM3459P

## P-Channel 60-V (D-S) MOSFET

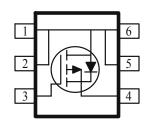
These miniature surface mount MOSFETs utilize High Cell Density process. Low r<sub>DS(on)</sub> assures minimal power loss and conserves energy, making this device ideal for use in power management circuitry. Typical applications are PWMDC-DC converters, power management in portable and battery-powered products such as computers, printers, battery charger, telecommunication power system, and telephones power system.

•	Low r <sub>DS(on)</sub> Provides Higher Efficiency and
	Extends Battery Life

- Miniature SO-8 Surface Mount Package Saves Board Space
- High power and current handling capability
- Extended VGS range (±25) for battery pack applications

PRODUCT SUMMARY			
V <sub>DS</sub> (V)	$r_{DS(on)}(\Omega)$	$I_{D}(A)$	
-60	0.310	2.1	
-00	$0.465 @ V_{GS} = -4.5V$	1.7	





ABSOLUTE MAXIMUM RATINGS (T <sub>A</sub> = 25 °C UNLESS OTHERWISE NOTED)					
Parameter		Symbol	Maximum	Units	
Drain-Source Voltage			-60	V	
Gate-Source Voltage			±20	V	
Continuous Durin Comment <sup>a</sup>	$T_A=25^{\circ}C$	T.,	2.1		
Continuous Drain Current <sup>a</sup>	$T_A=25^{\circ}C$ $T_A=70^{\circ}C$	П	1.7	A	
Pulsed Drain Current <sup>b</sup>		$I_{DM}$	±15		
Continuous Source Current (Diode Conduction) <sup>a</sup>		$I_S$	-1.7	A	
D D: a	$T_A=25^{\circ}C$	D	2.0	W	
Power Dissipation <sup>a</sup>	$T_A=25^{\circ}C$ $T_A=70^{\circ}C$	Ir D	1.3	VV	
Operating Junction and Storage Temperature Range		$T_{J}, T_{stg}$	-55 to 150	°C	

THERMAL RESISTANCE RATINGS					
Parameter		Symbol	Maximum	Units	
M . I	t <= 5 and	D	62.5	°C/W	
Maximum Junction-to-Ambient <sup>a</sup>	$t \le 5 \text{ sec}$	$R_{ heta JA}$	110	°C/W	

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## Notes

- a. Surface Mounted on 1" x 1" FR4 Board.
- b. Pulse width limited by maximum junction temperature

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SPECIFICATIONS (T <sub>A</sub> = 25°C UNLESS OTHERWISE NOTED)							
Parameter	Symbol	Test Conditions	Limits			T124	
rarameter	Symbol		Min	Тур	Max	Unit	
Static							
Gate-Threshold Voltage	V <sub>GS(th)</sub>	$V_{DS} = V_{GS}$ , $I_D = -250 \text{ uA}$	-1				
Gate-Body Leakage	I <sub>GSS</sub>	$V_{DS} = 0 \text{ V}, V_{GS} = \pm 20 \text{ V}$			±100	nA	
Zara Cata Valtaga Prain Current	IDSS	$V_{DS} = -48 \text{ V}, V_{GS} = 0 \text{ V}$			-1	uA	
Zero Gate Voltage Drain Current	IDSS	$V_{DS} = -48 \text{ V}, V_{GS} = 0 \text{ V}, T_J = 55^{\circ}\text{C}$			-10		
On-State Drain Current <sup>A</sup>	I <sub>D(on)</sub>	$V_{DS} = -5 \text{ V}, V_{GS} = -10 \text{ V}$	-20			A	
D i G O D i A		$V_{GS} = -10 \text{ V}, I_D = -2.1 \text{ A}$			310	mΩ	
Drain-Source On-Resistance <sup>A</sup>	fDS(on)	$V_{GS} = -4.5 \text{ V}, I_D = -1.7 \text{ A}$			465		
Forward Tranconductance <sup>A</sup>	gs	$V_{DS} = -15 \text{ V}, I_D = -2.1 \text{ A}$		8		S	
Diode Forward Voltage	V <sub>SD</sub>	$I_S = -2.5 \text{ A}, V_{GS} = 0 \text{ V}$			-1.2	V	
Dynamic <sup>b</sup>							
Total Gate Charge	Qg	$V_{DS} = -30 \text{ V}, V_{GS} = -4.5 \text{ V},$		18			
Gate-Source Charge	Qgs	$V_{DS} = -30 \text{ V}, V_{GS} = -4.3 \text{ V},$ $I_{D} = -2.1 \text{ A}$		5		nC	
Gate-Drain Charge	$Q_{gd}$	ID = -2.1  A		2			
Turn-On Delay Time	td(on)			8			
Rise Time	<b>t</b> r	$V_{DD} = -30 \text{ V}, R_L = 30 \Omega, ID = -1 \text{ A},$		10		nS	
Turn-Off Delay Time	t <sub>d(off)</sub>	$VGEN = -10 V$ , $RG = 6\Omega$		35		113	
Fall-Time	$t_{\mathrm{f}}$			12			

## Notes

- a. Pulse test:  $PW \le 300us duty cycle \le 2\%$ .
- b. Guaranteed by design, not subject to production testing.

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