AN3211K, AN3211S

VTR Recording Video Signal Processing Circuits

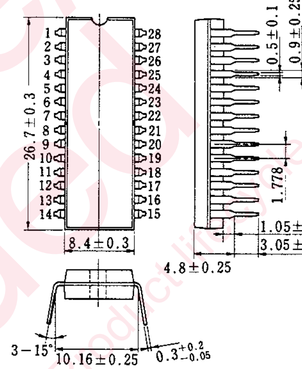
■ Outline

The AN3211K and the AN3211S are integrated circuits designed for VTR recording video signal processing circuits.

■ Features

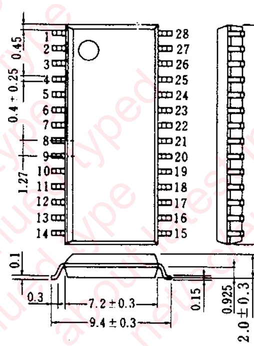
- Dynamic emphasis characteristics : 5.5dB(at f=1MHz, input level=−20dB)
- Built-in carrier interleaving circuit)
- Built-in low pass filter (sync-separation circuit)
- Supply voltage:V_{cc}=5V

AN3211K Unit : mm



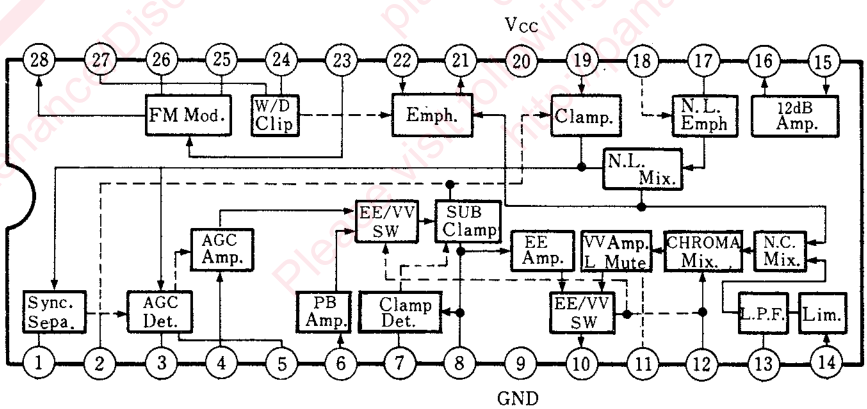
28-Lead Shrunk DIL Plastic Package

AN3211S Unit : mm



28-Lead PANAFLAT Package (SO-28D)

■ Block Diagram



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■ Absolute Maximum Ratings (Ta=25℃)

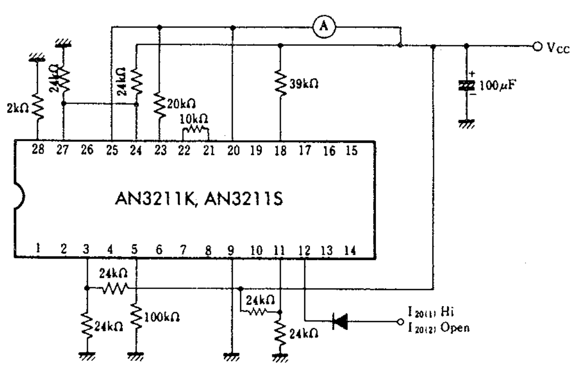
Item	Symbol	Rating	Unit
Supply Voltage	V_{CC}	6.0	V
Power Dissipation(Ta=70℃)	P_D	250	mW
Operating Ambient Temperature	T_{opr}	−20∼+70	℃
Storage Temperature	T_{stg}	−55∼+150	℃

■ Electrical Characteristics (V_{cc}=5V, Ta=25℃)

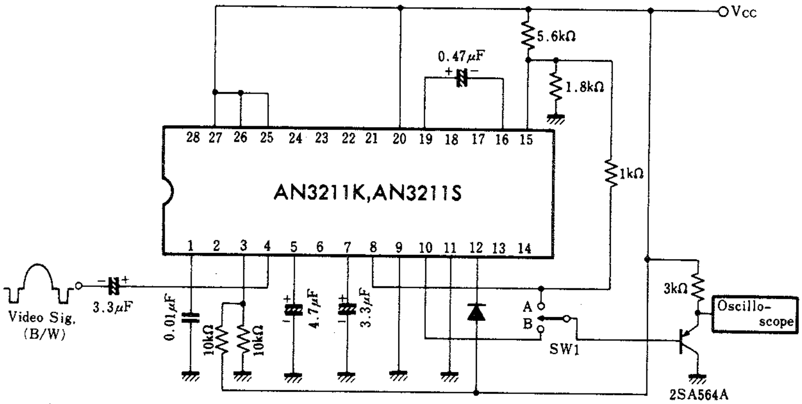
Item	Symbol	Test Circuit	Condition	min.	typ.	max.	Unit
Circuit Current(1)	$I_{20(1)}$	1	Pin ⑫ H_i (Rec.)	14.5		35.5	mA
Circuit Current(2)	$I_{20(2)}$	1	Pin ⑫ Open (PB)	14.5		35.5	mA
AGC Output Amplification	v_8	2	Pin ⑫ Hi, Video Input 1V_{P-P}	0.4		0.8	V_{P-P}
AGC Control Sensitivity	Δv_8	2	Pin ⑫ Hi, Video Input 0.5∼2V_{P-P}			1.5	dB
PB Amp. Gain	$G_{6\text{-}8}$	3	Pin ⑫ Open	6.8		9.9	dB
12dB Amp. Gain	$G_{15\text{-}16}$	3		10.4		13.4	dB
FM Oscillation Frequency	f_o	4	Pin ⑫ Hi, Co=39pF, Ro=12kΩ	2.9		3.9	MHz
FM Output 2nd High Frequency	$2f_o$	4	Pin ⑫ Hi, Co=39pF, Ro=12kΩ			−33	dB
FM Oscillation Output Amplification	v_{28}	4	Pin ⑫ Hi, Co=39pF, Ro=12kΩ	0.65		1.35	V_{P-P}
Frequency Control Sensitivity FM Oscillation	β_{28}	4	Pin ⑫ Hi, Co=39pF, Ro=8.2∼15kΩ	11.4		14.5	kHz/μA
Sync. Spea. Input Sensitivity	S_{19}	5	Video Input V/S=5/2	0.45			V_{P-P}
Sync. Spea. Output Amplification	v_2	5	Video Input V/S=5/2	4.3			V_{P-P}
NL Limiter Gain	$v_{17\text{-}21}$	6	Pin ⑫ Hi	20		40	mV_{P-P}
NL Limiter Output Amplification(1)	$v_{21(1)}$	6	Pin ⑫ Hi	26		64	mV_{P-P}
NL Limiter Output Amplification(2)	$v_{21(2)}$	6	Pin ⑫ Hi, Pin ⑱ Lo	6		2.6	mV_{P-P}
NC Limiter Gain	$v_{14\text{-}10}$	7	Pin ⑫ Open	30		70	mV_{P-P}
NC Limiter Output Amplification	v_{10}	7	Pin ⑫ Open	65		125	mV_{P-P}
EE Amp. Gain	$G_{8\text{-}10}$	2	Pin ⑫ Hi	9.7		11.6	dB
VV Amp. Gain	$v_{19\text{-}10}$	3	Pin ⑫ Open	1.65		2.15	V_{P-P}
Chroma Amp. Gain	$G_{12\text{-}10}$	7		5.3		8.8	dB
EE/VV Crosstalk	$CT_{19\text{-}10}$	8	E≧4.0V			−40	dB
Mute Crosstalk	$CT'_{19\text{-}10}$	8	Pin ⑫ Lo, Pin ⑪ Hi			−40	dB
EE/VV Changeover Sensitivity	S_{12}	8		4			V
FM Oscillation Carrier Interleave	Δf_o*	9	Pin ⑫ Hi	5.9		9.9	kHz
V offset	$\Delta v_{19\text{-}10}$*	3	Pin ⑫ Lo	30		110	mV

Note : Operating Supply Voltage Range V_{cc}=4.5∼5.5V * It is design value but not a guaranteed value.

Test Circuit 1 ($I_{20(1)}$, $I_{20(2)}$)



Test Circuit 2 (v_8, Δv_8, $G_{8\text{-}10}$)



● v_8

IN: 1.0$V_{P\text{-}P}$

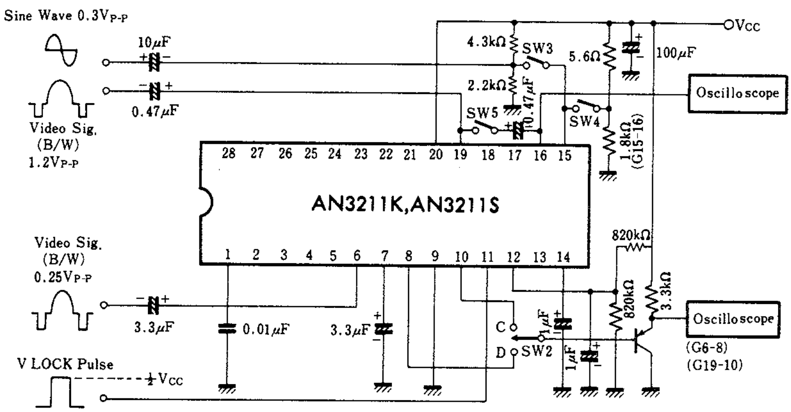
● Δv_8

Output amplification change between IN: 0.5$V_{P\text{-}P}$ to 2.0$V_{P\text{-}P}$

● G_{8-10}

IN: 1.0$V_{P\text{-}P}$
Ratio of output when SW1 is B to output when SW1 is A

Test Circuit 3 ($G_{6\text{-}8}$, $G_{15\text{-}16}$, $v_{19\text{-}10}$, $\Delta v_{19\text{-}10}$)



● G_{6-8}

IN: ⑥pin 0.25$V_{P\text{-}P}$
SW2: D

● G_{15-16}

IN: ⑮pin 0.3$V_{P\text{-}P}$
SW3: ON
SW4: OFF
SW5: OFF

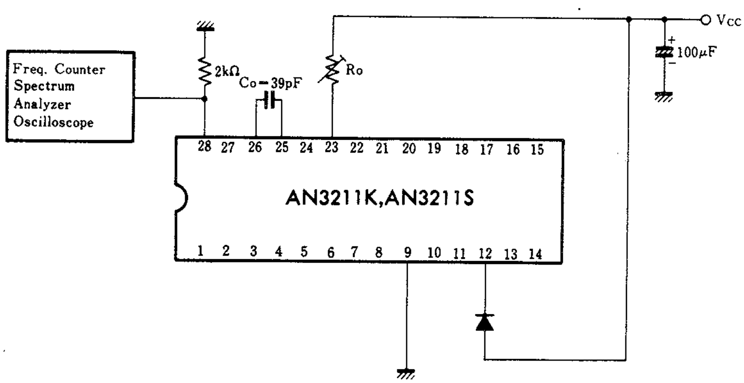
● v_{19-10}

IN: ⑲pin 1.2$V_{P\text{-}P}$
SW2: C
SW5: OFF

● Δv_{19-10}

IN: ⑲pin 1.2$V_{P\text{-}P}$
SW2: C
SW5: OFF

Test Circuit 4 (f_0, $2f_0$, v_{28}, β_{28})



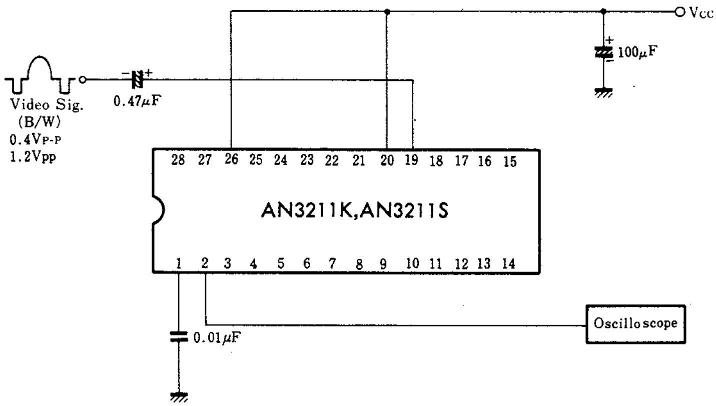
● fo, 2fo, v_{28}

Ro = 12kΩ

● β_{28}

Measure a change of oscillation frequency when Ro = 8.2kΩ ~ 15KΩ

Test Circuit 5 (S_{19}, v_2)



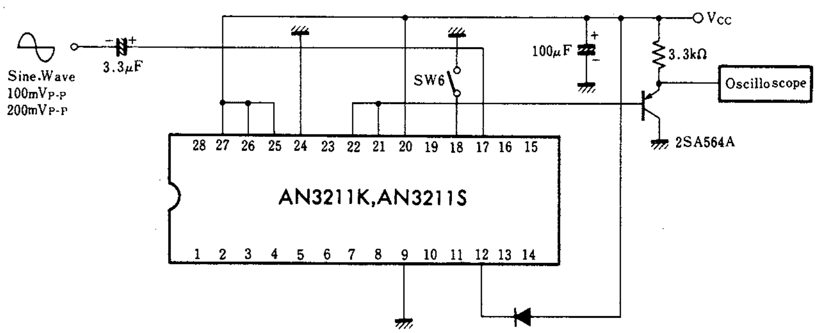
● S_{19}

IN:0.4V_{P-P}

● v_2

IN:1.2V_{P-P}

Test Circuit 6 ($v_{17\text{-}21}$, $v_{21(1)}$, $v_{21(2)}$)



● v_{17-21}

IN:100mV_{P-P}

● $v_{21}(1)$

IN:200mV_{P-P}

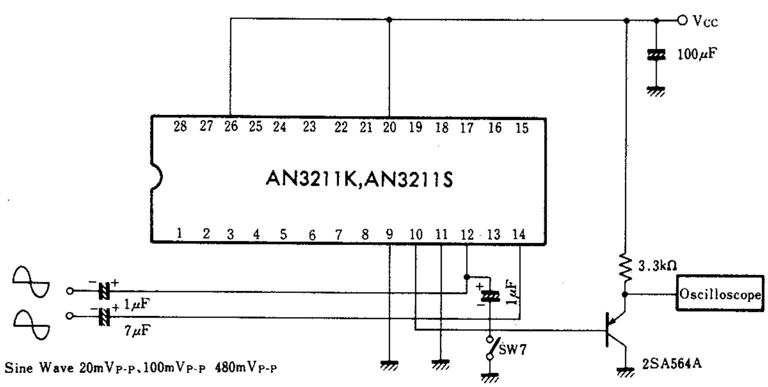
SW6:OFF

● $v_{21}(2)$

IN:200mV_{P-P}

SW6:ON

Test Circuit 7 ($v_{14\text{-}10}$, v_{10}, $G_{12\text{-}10}$)



● v_{14-10}

IN:20mV_{P-P}

1MHz

SW7:ON

● v_{10}

IN:100mV_{P-P}

1MHz

SW7:ON

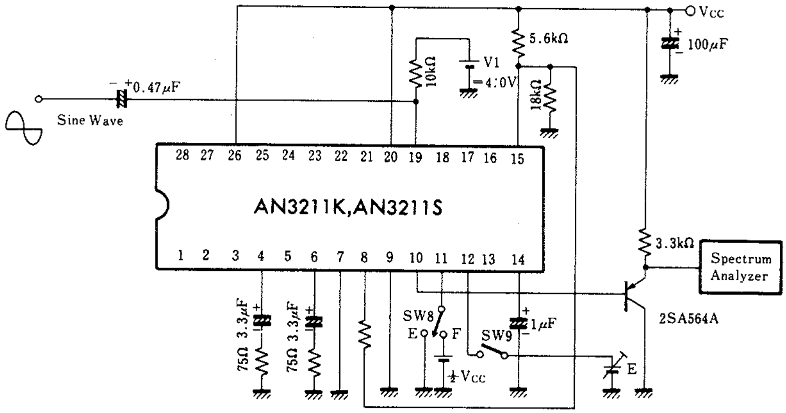
● G_{17-10}

IN:480mV_{P-P}

1MHz

SW7:OFF

Test Circuit 8 ($CT_{19\text{-}10}$, $CT'_{19\text{-}10}$, S_{12})



● CT_{19-10}

IN: 0.25V_{P-P} 1MHz

Measure the attenuation when SW9 is turned from OFF to ON.

● CT'_{19-10}

IN: 0.25V_{P-P} 1MHz

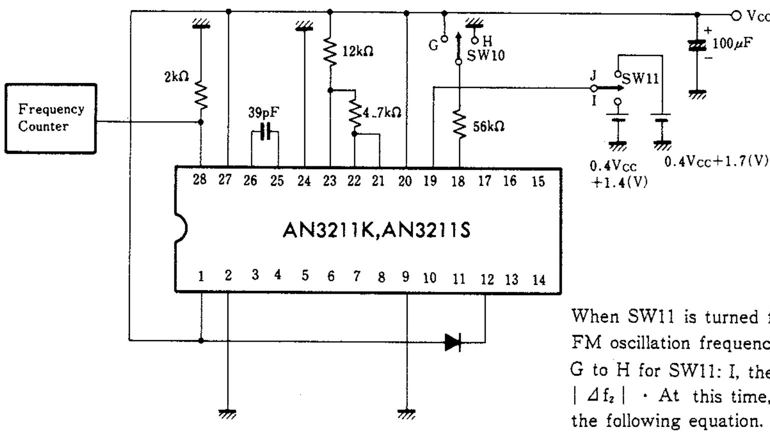
Measure the attenuation when SW8 is turned from E to F.

● S_{12}

IN: 0.25V_{P-P} 1MHz

Pin ⑫ voltage when the output signal for SW9:ON becomes −40dB or less.

Test Circuit 9 (Δf_0)



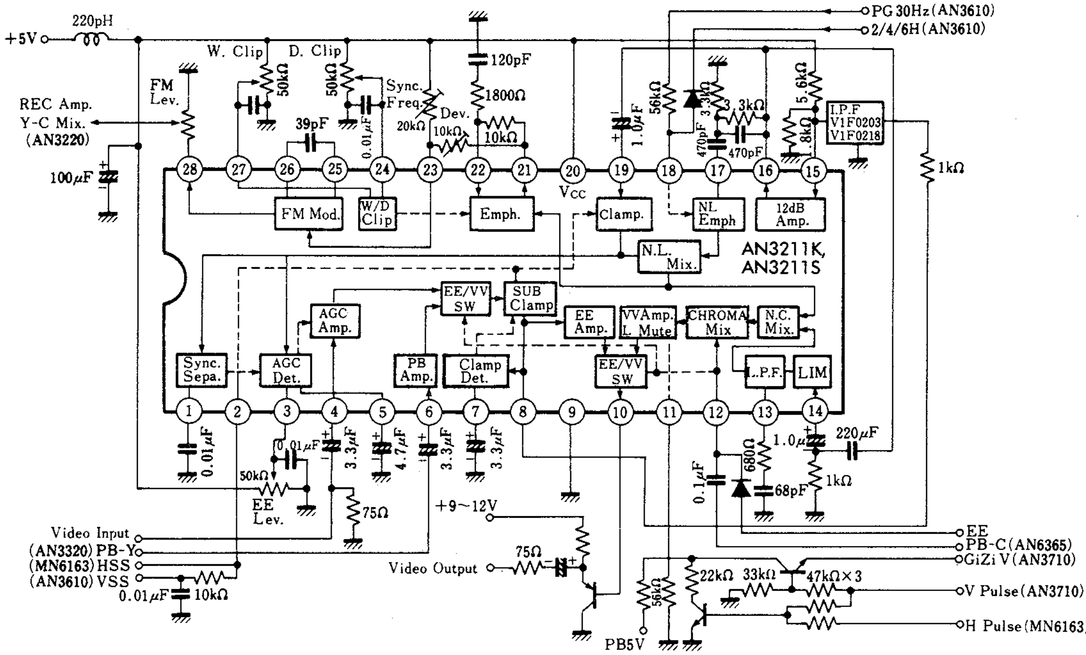
When SW11 is turned from I to J for SW10:G, the difference of FM oscillation frequency is $|\Delta f_1|$. When SW10 is turned from G to H for SW11: I, the difference of FM oscillation frequency is $|\Delta f_2|$. At this time, FM carrier interleave ratio Δfo is qiven by the following equation.

$$\Delta fo = \frac{|\Delta f_2|}{|\Delta f_1|} 250\,(\mathrm{kHz})$$

■ Pin

Pin No.	Pin Name	Pin No.	Pin Name
1	Sync Tip Level Detect	15	12dB Amp. Input
2	Sync Output	16	12dB Amp. Output
3	EE Level Adjustment	17	Non Linear Emphasis Sub-side Input
4	Video Signal Input During Recording	18	PG Input & 2/4/6H Select
5	AGC Detection	19	Main Clamp Input
6	Video Signal Input During PB	20	V_{CC}
7	Sub Clamp Detect	21	Main Emphasis Output
8	Sub Clamp Output	22	FB Amp. Input
9	GND	23	Mod. Input
10	EE/VV Output	24	Dark Clip Level Adjustment
11	Dummy Sync pulse Input	25	Mod.
12	PB Chroma Input	26	Mod.
13	Noise Canceller L.P.F.	27	White Clip Level Adjustment
14	Noise Canceller H.P.F-side Input	28	FM Output

■ Application Circuit

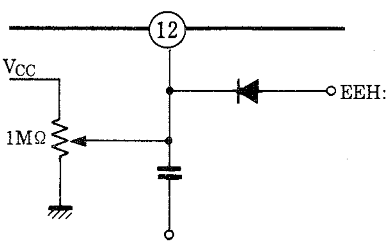


Notes for Use

In the electrical characteristics table of dummy V offset V_{19-10}, −30 to 110 (mV) is listed as reference value. If exceeded beyond this max. value, V synchronization for special regeneration is not made, resulting in being under minimum of the value. In such cases, a skew may be generated on the top of the display screen.

In these specifications for product, the reference value, from the view point of the set quality purpose, is listed just for reference for design. However, it is very unstable if used for ICs. So please be sure to take some measures such as external adjustment, etc. for this point when you use.

(Example of external adjustment circuit)



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