

ROHS COMPLIANT

Vishay Siliconix

P-Channel 20-V (D-S) MOSFET

PRODUCT SUMMARY				
V _{DS} (V)	R_{DS(on)} (Ω)	I _D (A)	Q _g (Typ.)	
- 20	0.030 at V _{GS} = - 4.5 V	- 12 ^a		
	0.041 at V _{GS} = - 2.5 V	- 12 ^a	15 nC	
	0.056 at V _{GS} = - 1.8 V	- 12 ^a	15110	
	0.150 at V _{GS} = - 1.5 V	- 2		

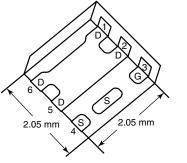
PowerPAK SC-70-6L-Single

FEATURES

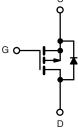
- Halogen-free
- TrenchFET[®] Power MOSFET
- New Thermally Enhanced PowerPAK[®] SC-70 Package
 - Small Footprint Area
 - Low On-Resistance

APPLICATIONS

 Load Switch, PA Switch and Battery Switch for Portable Devices



Marking Code



Ordering Information: SiA411DJ-T1-GE3 (Lead (Pb)-free and Halogen-free)

P-Channel MOSFET

Parameter		Symbol	Limit	Unit	
Drain-Source Voltage	V _{DS}	- 20	- V		
Gate-Source Voltage		V _{GS}			± 8
	T _C = 25 °C		- 12 ^a		
Continuous Drain Current (T _{.1} = 150 °C)	T _C = 70 °C	I _D	- 12 ^a		
(5)	T _A = 25 °C	D	- 8.8 ^{b, c}		
	T _A = 70 °C		- 7 ^{b, c}	A	
Pulsed Drain Current		I _{DM}	- 20		
Continuous Source-Drain Diode Current	T _C = 25 °C	I _S	- 12 ^a		
Commode Source Drain Diode Ourient	T _A = 25 °C	'5	- 2.9 ^{b, c}	7	
	T _C = 25 °C		19		
Maximum Power Dissipation	T _C = 70 °C	PD	12	w	
	T _A = 25 °C	' D	3.5 ^{b, c}	vv	
	T _A = 70 °C		2.2 ^{b, c}		
Operating Junction and Storage Temperature Ra	Т _Ј , Т _{stg}	- 55 to 150	°C		
Soldering Recommendations (Peak Temperatur		260			

THERMAL RESISTANCE RATINGS						
Parameter		Symbol	Typical	Maximum	Unit	
Maximum Junction-to-Ambient ^{b, f}	t ≤ 5 s	R _{thJA}	28	36	°C/W	
Maximum Junction-to-Case (Drain)	Steady State	R _{thJC}	5.3	6.5	- 0/11	

Notes:

a. Package limited.

b. Surface Mounted on 1" x 1" FR4 board.

c. t = 5 s.

e. Rework Conditions: manual soldering with a soldering iron is not recommended for leadless components.

f. Maximum under Steady State conditions is 80 °C/W.

d. See Solder Profile (http://www.vishay.com/ppg?73257). The PowerPAK SC-70 is a leadless package. The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper tip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection.

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SPECIFICATIONS $T_J = 25 \degree C_z$	unless oth	erwise noted					
Parameter	Symbol	Test Conditions	Min.	Тур.	Max.	Unit	
Static							
Drain-Source Breakdown Voltage	V _{DS}	$V_{GS} = 0 V, I_D = -250 \mu A$	- 20			V	
V _{DS} Temperature Coefficient	$\Delta V_{DS}/T_{J}$	L _ 250 uA		- 19.5		mV/°C	
V _{GS(th)} Temperature Coefficient	$\Delta V_{GS(th)}/T_J$	$\frac{1}{V_{GS(th)}/T_J} I_D = -250 \ \mu A$		2.3		mv/ C	
Gate-Source Threshold Voltage	V _{GS(th)}	$V_{DS} = V_{GS}$, $I_D = -250 \ \mu A$	- 0.4		- 1	V	
Gate-Source Leakage	I _{GSS}	$V_{DS} = 0 V$, $V_{GS} = \pm 8 V$			± 100	nA	
Zero Gate Voltage Drain Current	I _{DSS}	$V_{DS} = -20 \text{ V}, \text{ V}_{GS} = 0 \text{ V}$			- 1	μΑ	
		V_{DS} = - 20 V, V_{GS} = 0 V, T_{J} = 55 °C			- 10		
On-State Drain Current ^a	I _{D(on)}	$V_{DS}{\leq}$ - 5 V, V_{GS} = - 4.5 V	- 20			А	
		V _{GS} = - 4.5 V, I _D = - 5.9 A		0.025	0.030)	
	R _{DS(on)}	V _{GS} = - 2.5 V, I _D = - 5.0 A		0.033	0.041	Ω	
Drain-Source On-State Resistance ^a		V _{GS} = - 1.8 V, I _D = - 1.8 A		0.045	0.056		
		V _{GS} = - 1.5 V, I _D = - 0.7 A		0.075	0.150		
Forward Transconductance ^a	9 _{fs}	V _{DS} = - 10 V, I _D = - 5.9 A		21		S	
Dynamic ^b				I	•		
Input Capacitance	C _{iss}			1200		pF	
Output Capacitance	C _{oss}			210			
Reverse Transfer Capacitance	C _{rss}			155			
Tabal Oaks Observes		V_{DS} = - 10 V, V_{GS} = - 8 V, I_{D} = - 8.8 A		25	38		
Total Gate Charge	Qg	V _{DS} = - 10 V, V _{GS} = - 4.5 V, I _D = - 8.8 A		15	23		
Gate-Source Charge	Q _{gs}			2.5			
Gate-Drain Charge	Q _{gd}			4			
Gate Resistance	Rg	f = 1 MHz		5		Ω	
Turn-On Delay Time	t _{d(on)}			12	20	-	
Rise Time	t _r	V_{DD} = - 10 V, R_L = 1.4 Ω		65	100		
Turn-Off Delay Time	t _{d(off)}	$t_{d(off)}$ I _D \cong - 7 A, V _{GEN} = - 4.5 V, R _g = 1 Ω		40	60		
Fall Time	t _f	t _f		100	150		
Turn-On Delay Time	t _{d(on)}			5	10	- ns	
Rise Time	t _r	V_{DD} = - 10 V, R_L = 1.4 Ω		25	35		
Turn-Off Delay Time	t _{d(off)}	$I_{\rm D} \cong$ - 7 A, V _{GEN} = - 8 V, R _g = 1 Ω		40	60]	
Fall Time	t _f			12	20	1	
Drain-Source Body Diode Characterist	ics	·					
Continuous Source-Drain Diode Current	۱ _S	T _C = 25 °C			- 12	А	
Pulse Diode Forward Current	I _{SM}				20		
Body Diode Voltage	V _{SD}	I _S = - 7 A, V _{GS} = 0 V		- 0.85	- 1.2	V	
Body Diode Reverse Recovery Time	t _{rr}			20	40	ns	
Body Diode Reverse Recovery Charge	Q _{rr}	- Ι _F = - 7 A, di/dt = 100 A/μs, Τ _J = 25 °C		10	20	nC	
Reverse Recovery Fall Time	t _a	$\mu_{\rm F} = 7.7$, $\mu_{\rm H} \alpha_{\rm C} = 100 \text{ Av} \mu_{\rm S}$, $\mu_{\rm S} = 20.0$		13			
Reverse Recovery Rise Time	t _b			7		ns	

Notes:

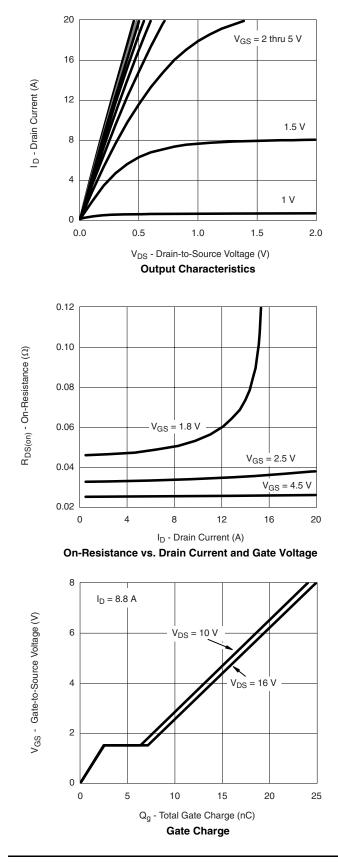
a. Pulse test; pulse width \leq 300 μ s, duty cycle \leq 2 %. b. Guaranteed by design, not subject to production testing.

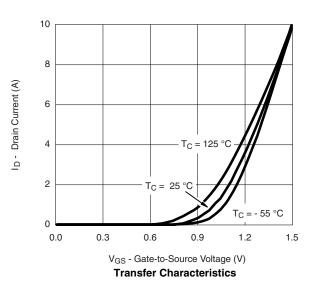
Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

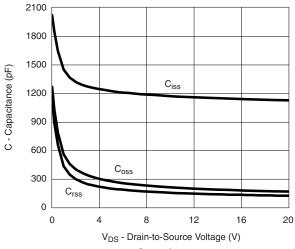


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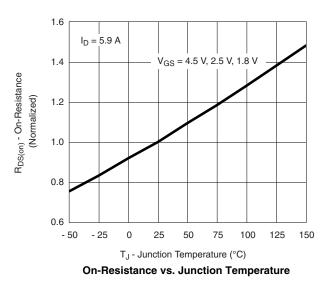
TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted











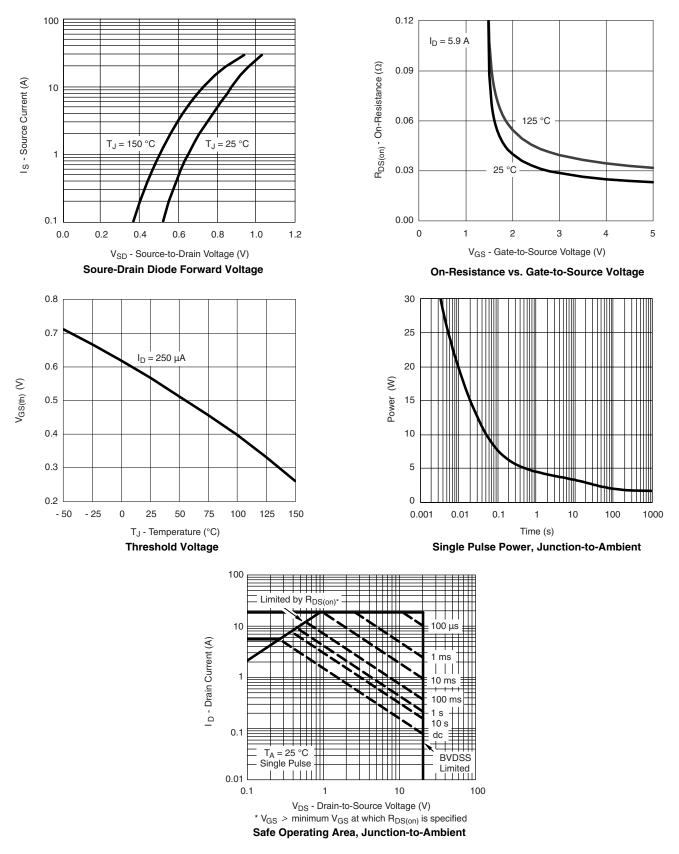
Document Number: 74464 S-80435-Rev. C, 03-Mar-08

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TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted

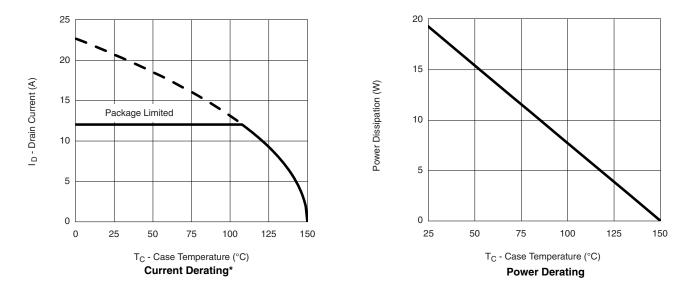






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TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



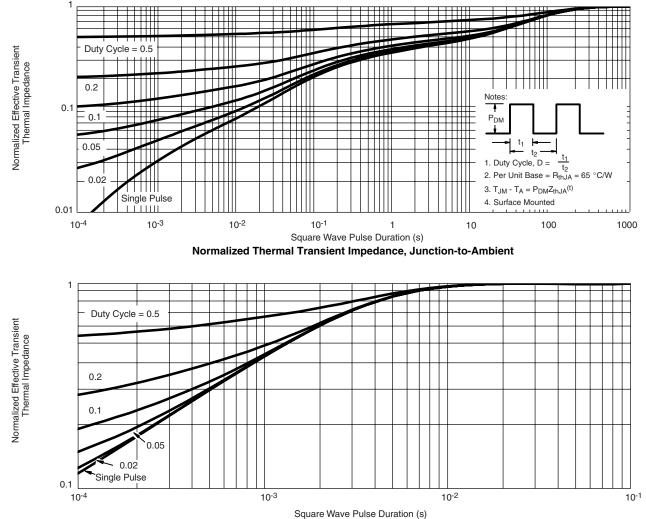
* The power dissipation P_D is based on $T_{J(max)} = 150$ °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit.

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TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



Normalized Thermal Transient Impedance, Junction-to-Case

Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package/tape drawings, part marking, and reliability data, see http://www.vishay.com/ppg?74464.



PowerPAK[®] SC70-6L

VISHA

b PIN2 PIN1 PIN3 _ ₹



b

PIN3

__ ₿

PIN2

PIN1

¥

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¹



RECOMMENDED PAD LAYOUT FOR PowerPAK[®] SC70-6L Single



Dimensions in mm/(Inches)

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