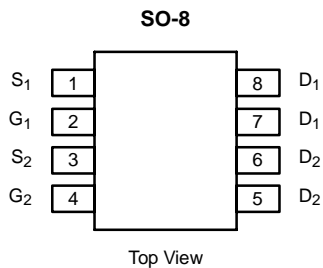




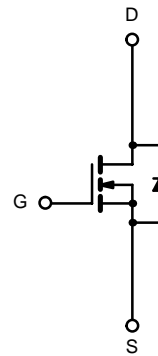
## Dual N-Channel 100-V (D-S) MOSFET

**TrenchFET®**  
Power MOSFETs

PRODUCT SUMMARY		
V <sub>DS</sub> (V)	r <sub>DS(on)</sub> (Ω)	I <sub>D</sub> (A)
100	0.150 @ V <sub>GS</sub> = 10 V	2.6
	0.180 @ V <sub>GS</sub> = 6 V	2.4



Ordering Information: Si4982DY  
Si4982DY-T1 (with Tape and Reel)



N-Channel MOSFET

ABSOLUTE MAXIMUM RATINGS (T <sub>A</sub> = 25°C UNLESS OTHERWISE NOTED)			
Parameter	Symbol	Limit	Unit
Drain-Source Voltage	V <sub>DS</sub>	100	V
Gate-Source Voltage	V <sub>GS</sub>	±20	
Continuous Drain Current (T <sub>J</sub> = 150°C) <sup>a</sup>	I <sub>D</sub>	T <sub>A</sub> = 25°C	A
		T <sub>A</sub> = 70°C	
Pulsed Drain Current	I <sub>DM</sub>	20	
Continuous Source Current (Diode Conduction) <sup>a</sup>	I <sub>S</sub>	1.7	
Maximum Power Dissipation <sup>a</sup>	P <sub>D</sub>	T <sub>A</sub> = 25°C	W
		T <sub>A</sub> = 70°C	
Operating Junction and Storage Temperature Range	T <sub>J</sub> , T <sub>stg</sub>	-55 to 150	°C

THERMAL RESISTANCE RATINGS			
Parameter	Symbol	Limit	Unit
Maximum Junction-to-Ambient <sup>a</sup>	R <sub>thJA</sub>	62.5	°C/W

Notes

a. Surface Mounted on FR4 Board, t ≤ 10 sec.

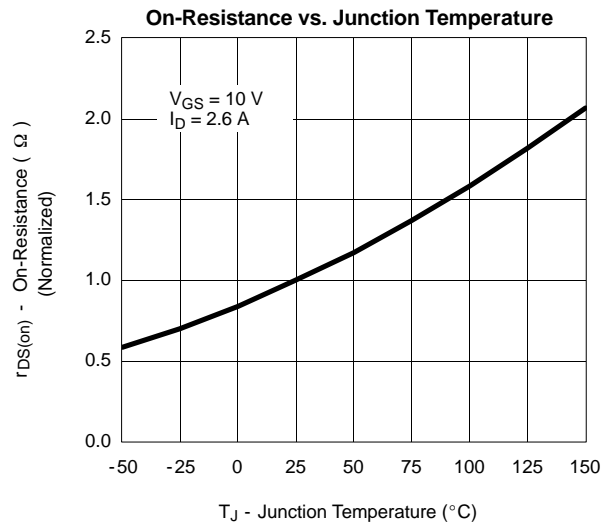
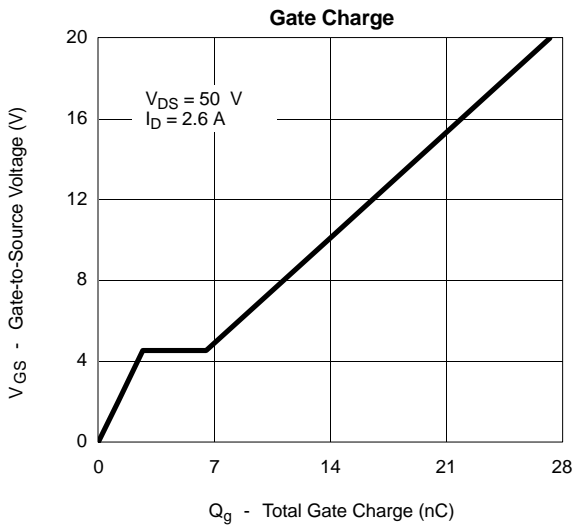
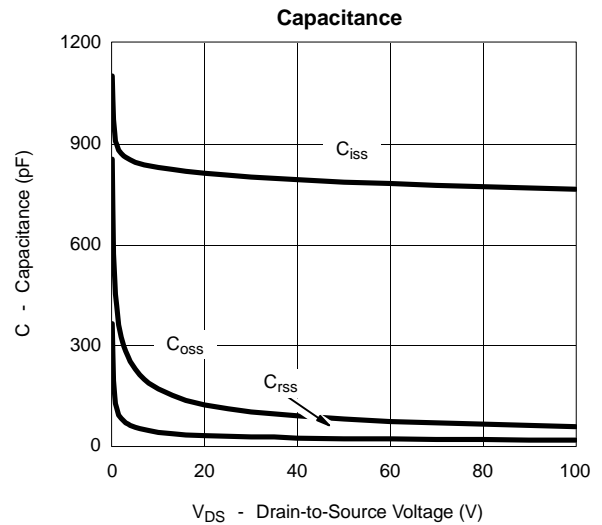
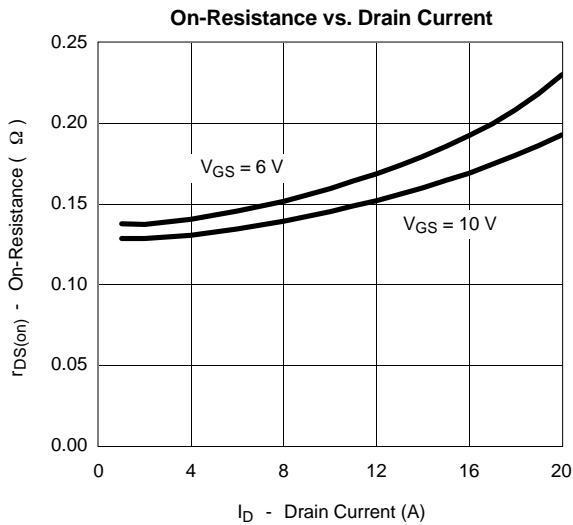
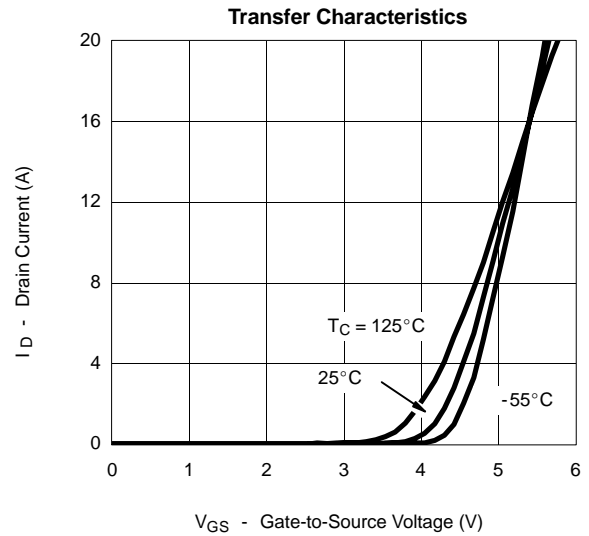
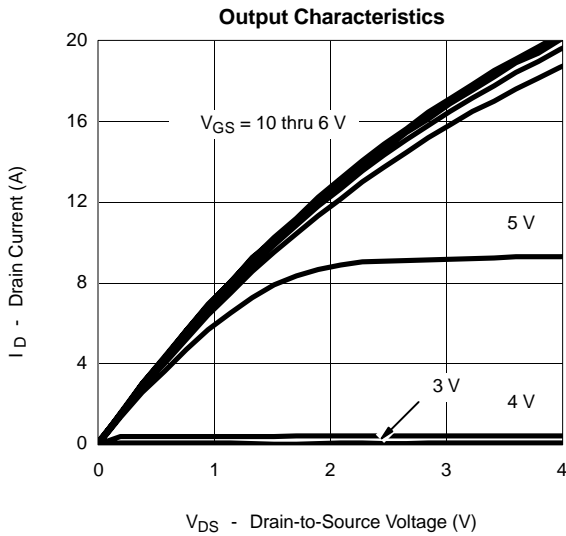
SPECIFICATIONS (T <sub>J</sub> = 25 °C UNLESS OTHERWISE NOTED)						
Parameter	Symbol	Test Condition	Min	Typ <sup>a</sup>	Max	Unit
<b>Static</b>						
Gate Threshold Voltage	V <sub>GS(th)</sub>	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = 250 μA	2			V
Gate-Body Leakage	I <sub>GSS</sub>	V <sub>DS</sub> = 0 V, V <sub>GS</sub> = ± 20 V			± 100	nA
Zero Gate Voltage Drain Current	I <sub>DSS</sub>	V <sub>DS</sub> = 100 V, V <sub>GS</sub> = 0 V			1	μA
		V <sub>DS</sub> = 100 V, V <sub>GS</sub> = 0 V, T <sub>J</sub> = 55 °C			20	
On-State Drain Current <sup>b</sup>	I <sub>D(on)</sub>	V <sub>DS</sub> = 5 V, V <sub>GS</sub> = 10 V	15			A
Drain-Source On-State Resistance <sup>b</sup>	r <sub>DS(on)</sub>	V <sub>GS</sub> = 10 V, I <sub>D</sub> = 2.6 A		0.130	0.150	Ω
		V <sub>GS</sub> = 6 V, I <sub>D</sub> = 2.4 A		0.140	0.180	
Forward Transconductance <sup>b</sup>	g <sub>fs</sub>	V <sub>DS</sub> = 15 V, I <sub>D</sub> = 2.6 A		11		S
Diode Forward Voltage <sup>b</sup>	V <sub>SD</sub>	I <sub>S</sub> = 1.7 A, V <sub>GS</sub> = 0 V			1.2	V
<b>Dynamic<sup>a</sup></b>						
Total Gate Charge	Q <sub>g</sub>	V <sub>DS</sub> = 50 V, V <sub>GS</sub> = 10 V, I <sub>D</sub> = 2.6 A		15	30	nC
Gate-Source Charge	Q <sub>gs</sub>			2.7		
Gate-Drain Charge	Q <sub>gd</sub>			4.0		
Gate Resistance	R <sub>g</sub>		1		4.4	Ω
Turn-On Delay Time	t <sub>d(on)</sub>	V <sub>DD</sub> = 50 V, R <sub>L</sub> = 50 Ω I <sub>D</sub> ≅ 1 A, V <sub>GEN</sub> = 10 V, R <sub>G</sub> = 6 Ω		10	20	ns
Rise Time	t <sub>r</sub>			10	20	
Turn-Off Delay Time	t <sub>d(off)</sub>			30	60	
Fall Time	t <sub>f</sub>			10	20	
Source-Drain Reverse Recovery Time	t <sub>rr</sub>	I <sub>F</sub> = 1.7 A, di/dt = 100 A/μs		60	90	

## Notes

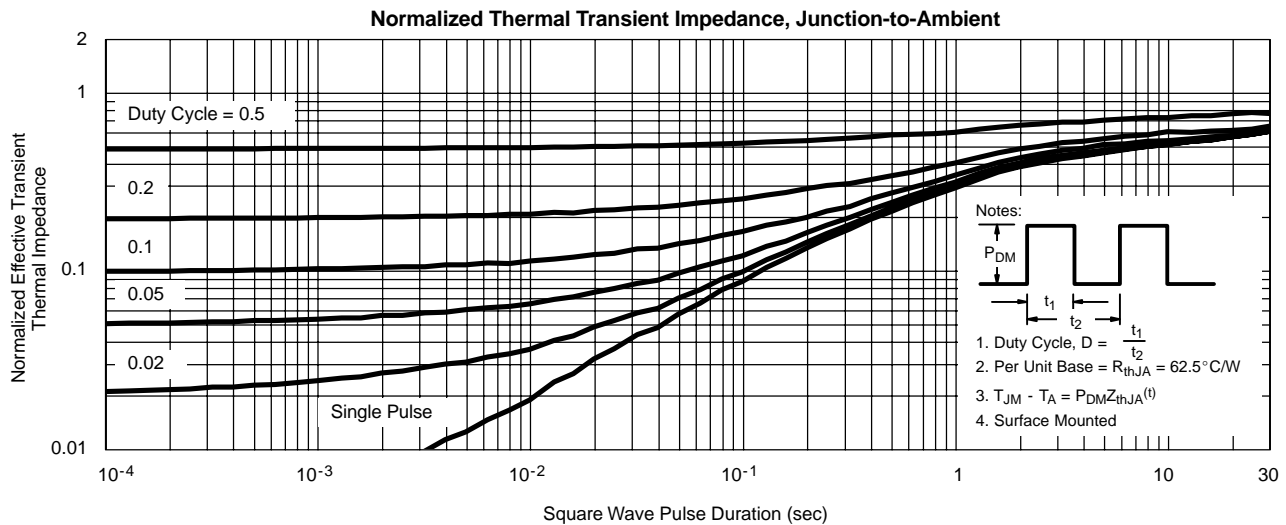
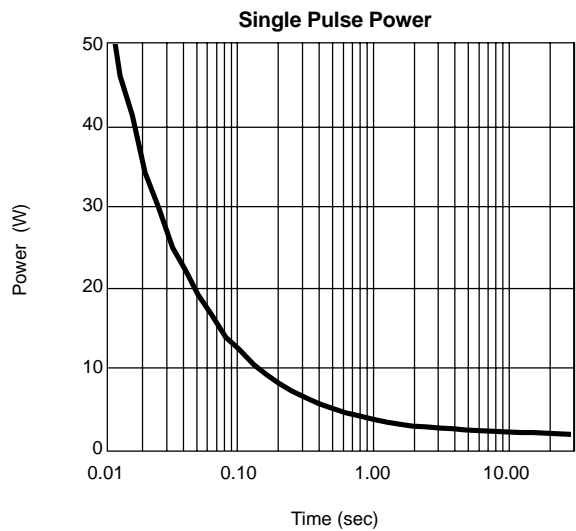
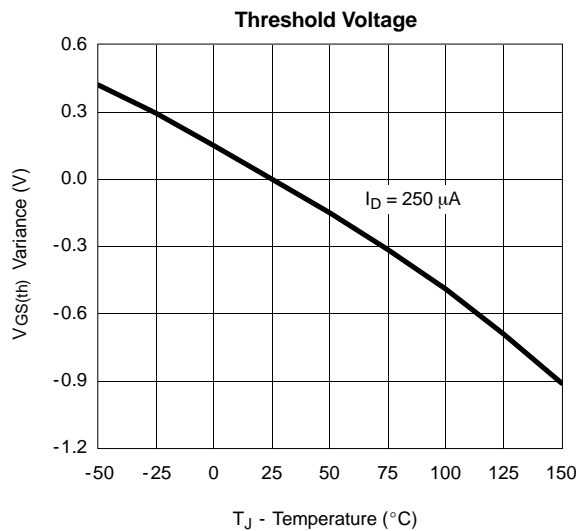
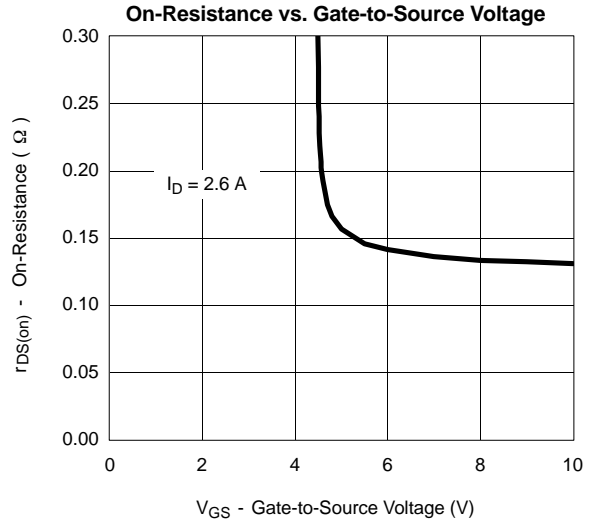
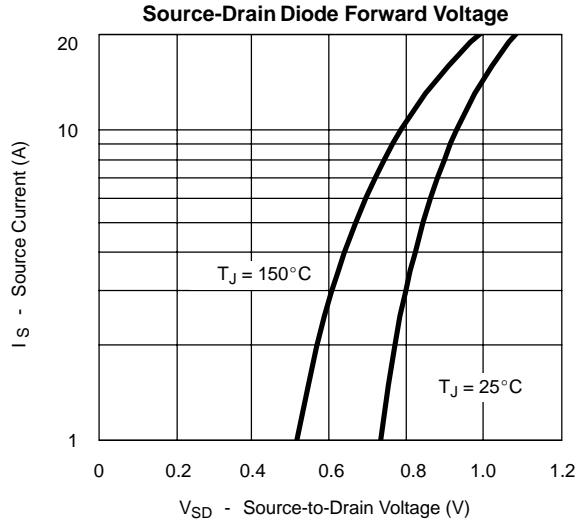
- a. For design aid only; not subject to production testing.  
 b. Pulse test; pulse width ≤ 300 μs, duty cycle ≤ 2%.



**TYPICAL CHARACTERISTICS (25°C UNLESS NOTED)**



**TYPICAL CHARACTERISTICS (25 °C UNLESS NOTED)**





## Disclaimer

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