SMP25N06, SMP25N05

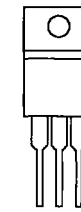
N-Channel Enhancement Mode Transistors

PRODUCT SUMMARY

PART NUMBER	$V_{(BR)DSS}$ (V)	$r_{DS(ON)}$ (Ω)	I_D (A)
SMP25N06	60	0.060	25
SMP25N05	50	0.060	25

TO-220AB

TOP VIEW



1 GATE
2 DRAIN (Connected to TAB)
3 SOURCE

1 2 3

ABSOLUTE MAXIMUM RATINGS (T_C = 25°C Unless Otherwise Noted)

PARAMETERS/TEST CONDITIONS		SYMBOL	LIMITS SMP25N06	LIMITS SMP25N05	UNITS
Gate-Source Voltage		V_{GS}	±20	±20	V
Continuous Drain Current	T_C = 25°C	I_D	25	25	A
	T_C = 100°C		16	16	
Pulsed Drain Current[1]		I_{DM}	100	100	
Avalanche Current (See Figure 9)		I_{AR}	25	25	
Repetitive Avalanche Energy[2]	L = 0.05 mH	E_{AR}	15	15	mJ
Power Dissipation	T_C = 25°C	P_D	85	85	W
	T_C = 100°C		34	34	
Operating Junction & Storage Temperature Range		T_J, T_{stg}	-55 to 150		°C
Lead Temperature ($^1/_{16}$" from case for 10 sec.)		T_L	300		

THERMAL RESISTANCE RATINGS

THERMAL RESISTANCE	SYMBOL	TYPICAL	MAXIMUM	UNITS
Junction-to-Case	R_{thJC}		1.47	K/W
Junction-to-Ambient	R_{thJA}		80	
Case-to-Sink	R_{thCS}	1.0		

[1]Pulse width limited by maximum junction temperature (refer to transient thermal impedance data, Figure 11).
[2]Duty cycle ≤ 1%.

ELECTRICAL CHARACTERISTICS (T_J = 25°C Unless Otherwise Noted)

PARAMETER		SYMBOL	TEST CONDITIONS	TYP	LIMITS MIN	LIMITS MAX	UNIT
STATIC							
Drain-Source Breakdown Voltage	SMP25N06	$V_{(BR)DSS}$	V_{GS} = 0 V, I_D = 250 µA	65	60		V
	SMP25N05			60	50		
Gate Threshold Voltage		$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 1000 µA	3.3	2.0	4.0	
Gate-Body Leakage		I_{GSS}	V_{DS} = 0 V, V_{GS} = ±20 V			±100	nA
Zero Gate Voltage Drain Current		I_{DSS}	V_{DS} = $V_{(BR)DSS}$, V_{GS} = 0 V			250	µA
			V_{DS} = 0.8 x $V_{(BR)DSS}$, V_{GS} = 0 V, T_J = 125°C			1000	
On-State Drain Current[1]		$I_{D(ON)}$	V_{DS} = 5 V, V_{GS} = 10 V	35	25		A
Drain-Source On-State Resistance[1]		$r_{DS(ON)}$	V_{GS} = 10 V, I_D = 12.5 A	0.05		0.060	Ω
			V_{GS} = 10 V, I_D = 12.5 A, T_J = 125°C	0.08		0.11	
Forward Transconductance[1]		g_{fs}	V_{DS} = 15 V, I_D = 12.5 A	9.0	5.0		S
DYNAMIC							
Input Capacitance		C_{iss}	V_{GS} = 0 V, V_{DS} = 25 V, f = 1 MHz	1020			pF
Output Capacitance		C_{oss}		500			
Reverse Transfer Capacitance		C_{rss}		120			
Total Gate Charge[2]		Q_g	V_{DS} = 0.5 x $V_{(BR)DSS}$, V_{GS} = 10 V, I_D = 25 A	28		40	nC
Gate-Source Charge[2]		Q_{gs}		8		15	
Gate-Drain Charge[2]		Q_{gd}		15		22	
Turn-On Delay Time[2]		$t_{d(on)}$	V_{DD} = 30 V, R_L = 2.4 Ω, I_D ≃ 12.5 A, V_{GEN} = 10 V, R_G = 4.7 Ω	15		50	ns
Rise Time[2]		t_r		20		75	
Turn-Off Delay Time[2]		$t_{d(off)}$		25		50	
Fall Time[2]		t_f		15		50	
SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS (T_C = 25°C)							
Continuous Current		I_S				25	A
Pulsed Current[3]		I_{SM}				100	
Forward Voltage[1]		V_{SD}	I_F = I_S, V_{GS} = 0 V	1.25		2.4	V
Reverse Recovery Time		t_{rr}	I_F = I_S, dI_F/dt = 100 A/µs	100			ns
Reverse Recovery Charge		Q_{rr}		0.15			µC

[1]*Pulse test: Pulse Width ≤ 300 µsec, Duty Cycle ≤ 2%.*
[2]Independent of operating temperature.
[3]Pulse width limited by maximum junction temperature (refer to transient thermal impedance data, Figure 11).

TYPICAL CHARACTERISTICS (25°C Unless Otherwise Specified)

Figure 1. Output Characteristics

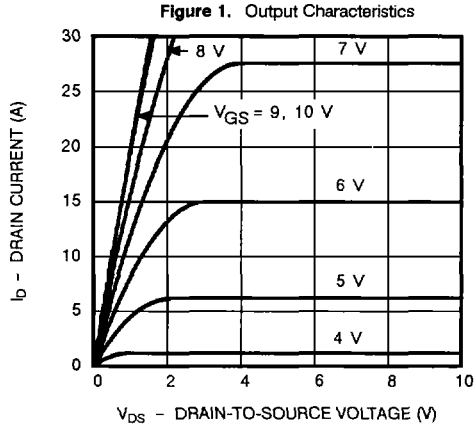


Figure 2. Transfer Characteristics

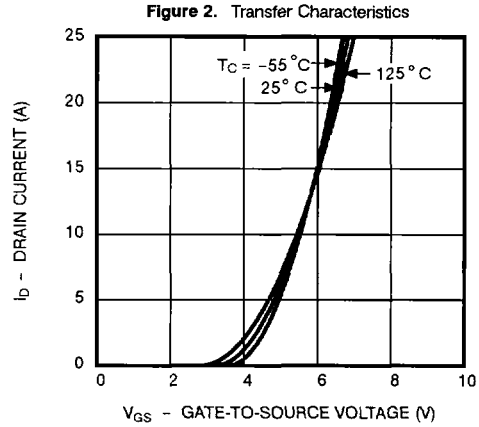


Figure 3. Transconductance

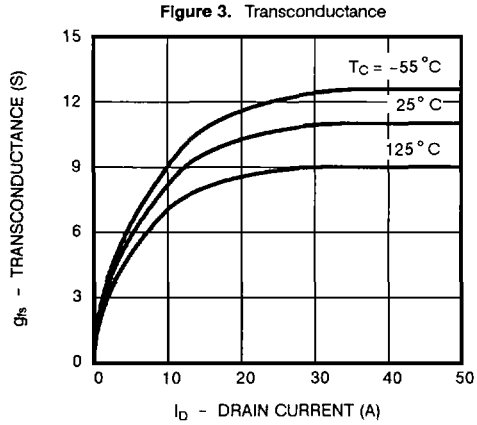


Figure 4. On-Resistance

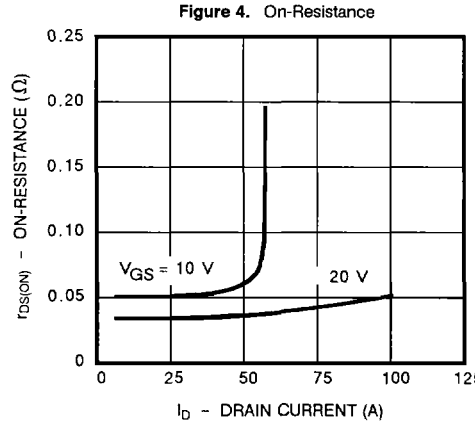


Figure 5. Capacitance

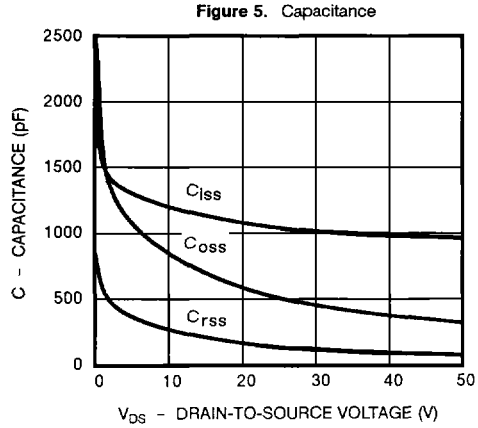
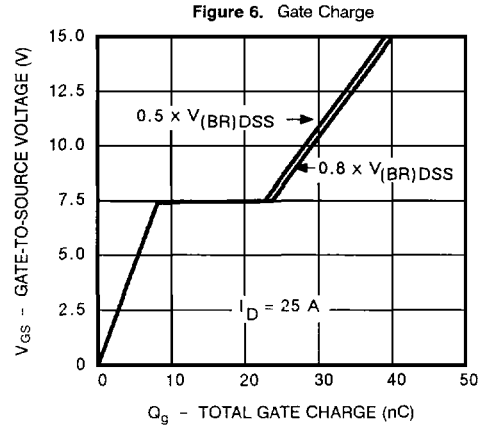


Figure 6. Gate Charge



4

TYPICAL CHARACTERISTICS (Cont'd)

Figure 7. On-Resistance vs.Junction Temperature

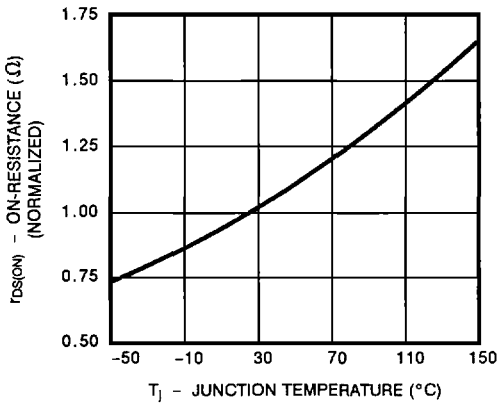
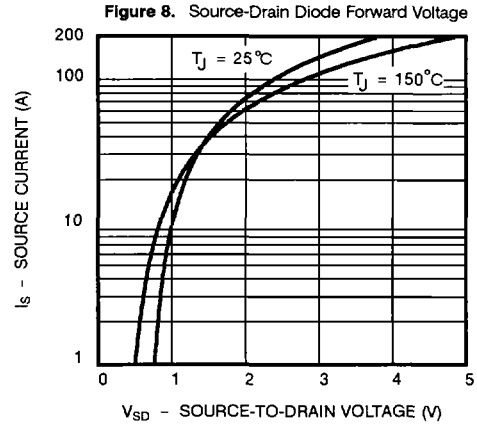


Figure 8. Source-Drain Diode Forward Voltage



THERMAL RATINGS

Figure 9. Maximum Avalanche and Drain Current vs. Case Temperature

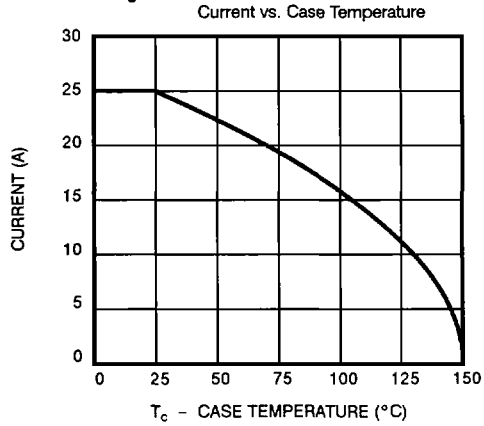
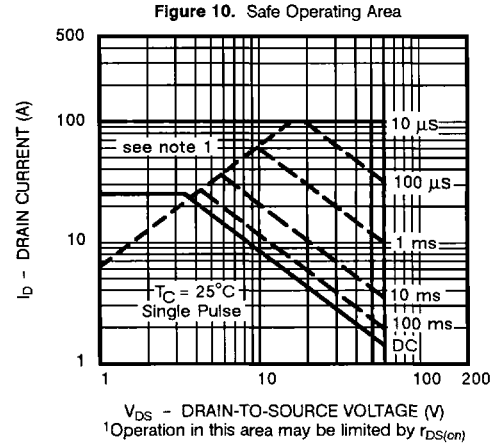


Figure 10. Safe Operating Area



[1]Operation in this area may be limited by $r_{DS(on)}$

Figure 11. Normalized Effective Transient Thermal Impedance, Junction-to-Case