

S1R72U06

Data Sheet

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1. Overview

The S1R72U06 is a serial (UART/SPI) - USB 2.0 host/device bridge LSI supporting USB 2.0 FS/LS. The main CPU controls the LSI's USB functions using simplified commands. No USB driver is required. The USB classes supported are Mass Storage class (for USB host operation) and Human Interface Device class (for USB host/device operation).

2. Features

2. Features

■ Ease of use and easy connections (serial connections)

Uses simplified commands to control USB functions

The main CPU controls this LSI's USB functions using simplified commands. No USB driver needs to be installed.

The UART (2-wire asynchronous) or SPI (clock synchronous) serial interface permits the easy connection of various CPU types.

■ Built-in regulator

USB regulator

Core voltage regulator

The S1R72U06 has two regulators: one (input range: 3.3 to 5.0 V) to generate 3.3 V for the USB and another (input voltage: 3.3 to 5.0 V) to generate the internal core voltage of 1.8 V. This allows the S1R72U06 to operate from a single power source as long as the supplied voltage is at least 3.3 V.

■ Built-in VBUS supply function

No external VBUS power SW required

The S1R72U06 features a built-in VBUS supply function for USB host operations, eliminating the need for the external VBUS power SW previously required by the USB host controller. The S1R72U06 features an interface that controls the external VBUS power SW if the built-in VBUS supply function cannot supply adequate current. If necessary, connect an external VBUS power SW to ensure sufficient current capacity for bus-powered devices.

■ Product (system) development support function

History display

The S1R72U06 uses a serial interface (asynchronous type) to display the history of internal LSI processing, etc. This function provides useful information during product (system) development.

3. Block Diagram

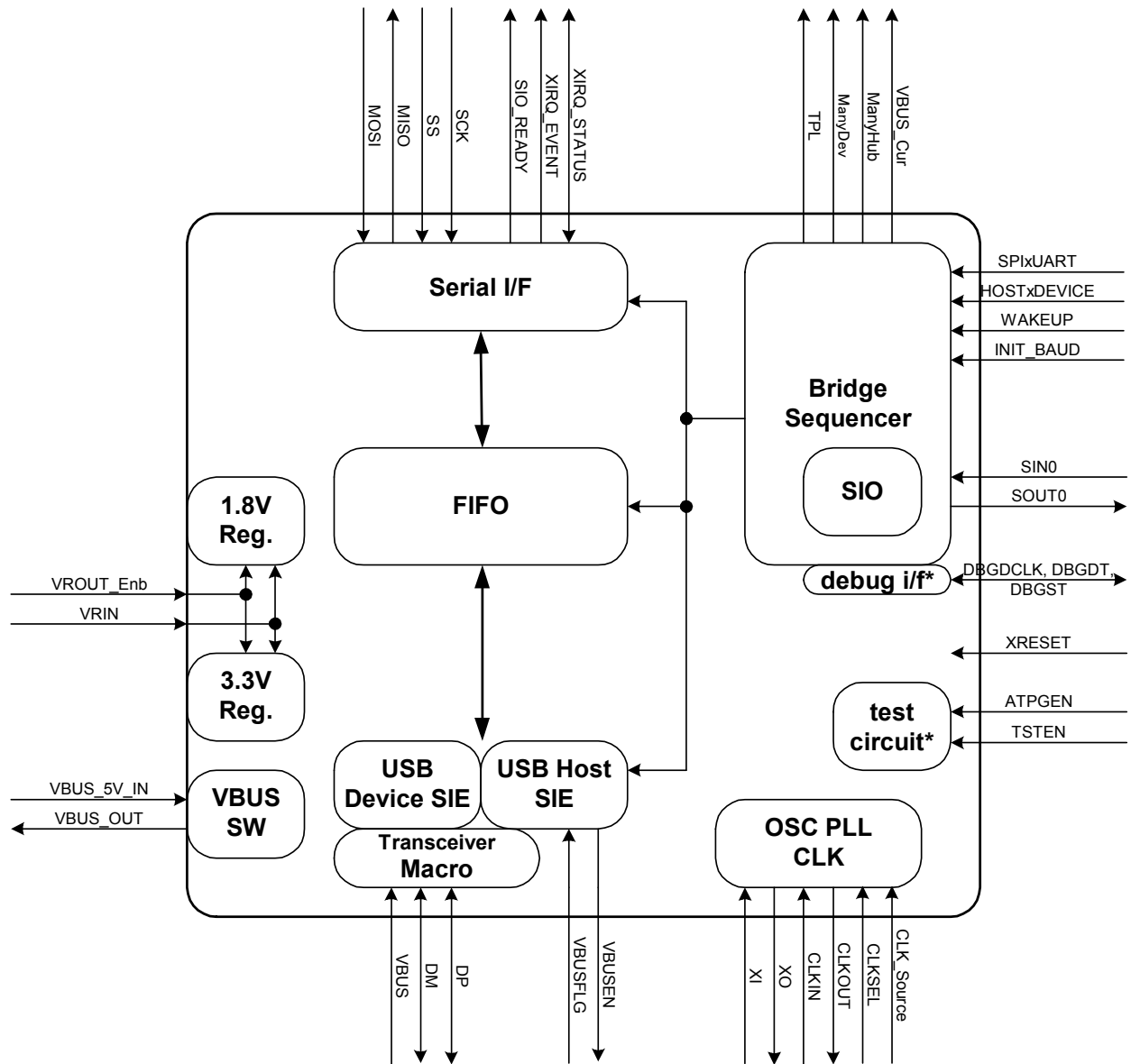


Figure 3.1 Block diagram

4. Functions

4. Functions

4.1 Serial I/F (UART/SPI)

The S1R72U06 is connected to the main CPU via UART (2-wire asynchronous) or SPI (clock synchronous). When using with UART, set the SPIxUART mode setting pin to Low. When using with SPI, set the SPIxUART mode setting pin to High.

The interface voltage (CVDD) can be used across a broad range, from 1.8 to 5.0 V.

- UART connection (asynchronous serial I/F)

Initial baud rate: 300/9600 bps (set by mode setting pin INIT_BAUD)

Baud rate: Settable (max. 3 Mbps)

lsb first

8-bit data

1/2 stop bit

Odd/Even/No parity

- SPI connection (clock synchronous serial I/F)

SPI slave

Mode 0 (Positive pulse latch first)

Baud rate: Max. 6 Mbps (SCK pin input)

msb first

8-bit data

4.2 USB Host SIE

The USB host function complies with the USB 2.0 (Universal Serial Bus Specification Revision 2.0) standard. It supports FS (12 Mbps) and LS (1.5 Mbps) speed modes. The USB functions are controlled by the Bridge Sequencer block inside the LSI. The USB classes supported are the Mass Storage Class and the Human Interface Device Class.

4.3 USB Device SIE

The USB device function complies with the USB 2.0 (Universal Serial Bus Specification Revision 2.0) standard. It supports FS (12 Mbps) and LS (1.5 Mbps) speed modes. The USB function is controlled by the Bridge Sequencer block inside the LSI. The USB class supported is the Human Interface Device Class.

4.4 Transceiver Macro

This is a USB analog macro block shared by host and device.

4.5 FIFO

This FIFO block serves as a buffer for data between the serial interface and the USB.

4.6 Bridge Sequencer

This controls the USB functions based on commands from the serial interface.

4.7 SIO

This block is used to display the history of the product (system) development support functions and for analog tests.

4.8 Debug I/F

This is a debugging pin for the built-in Bridge Sequencer. It is not intended for use by the user and should be disregarded.

4.9 1.8-V Regulator

This regulator generates 1.8-V internal core voltage. The range of input voltages is from 3.3 to 5.0 V.

4.10 3.3-V Regulator

This regulator generates 3.3 V for the USB. The range of input voltages is from 3.3 to 5.0 V.

4.11 VBUS SW

This is a VBUS output block built into the LSI.

4.12 Test Circuit

This is a circuit for IC tests. It is not intended for use by the user and should be disregarded.

5. Pin Layout Diagram

5. Pin Layout Diagram

			36	35	34	33	32	31	30	29	28	27	26	25			
			WAKEUP	HOSTXDEV	SPIUART	SCK	CVDD	SS	MISO	XRESET	MOSI	XIRQ_STATUS	XIRQ_EVENT	SIO_READY			
37	ATPGEN														TPL	24	
38	INIT_BAUD														ManyDev	23	
39	CLKSEL														ManyHub	22	
40	CLKIN														VBUS_Cur	21	
41	CLK_Source														VSS	20	
42	CLKOUT														(NC)	19	
43	VSS														DBGDT	18	
44	TSTEN														DBGST	17	
45	VR0UT_Enb														DBGDCLK	16	
46	LVDD														SIN0	15	
47	VRIN														SOUT0	14	
48	VSS														VBUSEN	13	
			VBUS_OUT	VBUS_5V_IN	VSS	VRIN	LVDD3	VSS	DM	DP	VBUS	XI	XO	VBUSFLAG			
			1	2	3	4	5	6	7	8	9	10	11	12			

Figure 5.1 Package pin layout diagram (common to QFP and QFN)

6. Pin Functions

GENERAL (CVDD system)					
BGA	QFP	Name	I/O	RESET	Pin description
-	29	XRESET	IN	-	Reset signal
-	39	CLKSEL	IN	-	Clock frequency selection Set the frequency input from the clock source (CLKIN or XI pin). 1: 24 MHz 0: 12 MHz
-	41	CLK_Source	IN	-	Clock source selection Set whether the clock source is input from the CLKIN or XI pin. 1: CLKIN 0: XI
-	40	CLKIN	IN	-	Clock input 12 MHz / 24MHz If the clock input is from the XI pin, set this pin to Low.
-	42	CLKOUT	OUT	Low	Clock output Refer to the <i>S1R72U06 Technical Manual</i> for information on how to change the clock output. 48 MHz / 24 MHz / 12 MHz / 6 MHz / 3 MHz / STOP

OSC (LVDD system)					
BGA	QFP	Name	I/O	RESET	Pin description
-	10	XI	IN	-	Internal oscillator circuit input If the clock input is from the CLKIN pin, set this pin to Low. 12 MHz / 24 MHz
-	11	XO	OUT	-	Internal oscillator circuit output If the clock input is from the CLKIN pin, leave this pin open.

TEST (LVDD, CVDD systems)					
BGA	QFP	Name	I/O	RESET	Pin description
-	44	TSTEN	IN(PD)	-	Test pin (*1); not intended for use by user
-	37	ATPGEN	IN(PD)	-	Test pin (*1); not intended for use by user

PD: Pull-down I/Os are used.

*1 This is pulled down inside the LSI. However, we recommend fixing it at Low on the circuit board.

USB (UVDD3 system)					
BGA	QFP	Name	I/O	RESET	Pin description
-	9	VBUS	IN	-	VBUS input pin VBUS input pin when S1R72U06 is used as USB device. Leave this pin open when using S1R72U06 as a USB host.
-	8	DP	BI	Hi-Z	USB data line Data+
-	7	DM	BI	Hi-Z	USB data line Data-

6. Pin Functions

VBUS (UVDD3 system)					
BGA	QFP	Name	I/O	RESET	Pin description
-	12	VBUSFLG	IN(PU)	-	USB power switch fault detection signal 1: Normal, 0: Error CMOS Schmitt input Use when external USB power switch is added. Leave open when not used.
-	13	VBUSEN	OUT	Low	USB power switch control signal Use when external USB power switch is added. Leave open when not used.

PU: Pull-up I/Os are used.

Serial I/F (CVDD system): Main CPU					
BGA	QFP	Name	I/O	RESET	Pin description
-	30	MISO	Tri	High	Serial data output (Hi-z is output when the SS pin is set to High even when using in UART mode.)
-	28	MOSI	IN	-	Serial data input
-	31	SS	IN	-	Slave selection In SPI mode (Can be used to control output from the MISO pin even when using in UART mode. If Hi-z output is not required, fix this pin at Low.)
-	33	SCK	IN	-	Serial clock In SPI mode (Fix at low when using in UART mode.)
-	25	SIO_READY	OUT	Low	Communication ready notification pin Refer to the <i>S1R72U06 Technical Manual</i> for detailed instructions on using this pin. Leave open when not used.
-	27	XIRQ_STATUS	OUT	High	Status notification Refer to the <i>S1R72U06 Technical Manual</i> for detailed instructions on using this pin. Leave open when not used.
-	26	XIRQ_EVENT	OUT	High	Event read request Refer to the <i>S1R72U06 Technical Manual</i> for detailed instructions on using this pin. Leave open when not used.

Serial I/F (UVDD3 system): History Display					
BGA	QFP	Name	I/O	RESET	Pin description
-	15	SIN0	IN	-	Asynchronous serial data IN Serial data IN pin for history display. Refer to the <i>S1R72U06 Development Support Manual</i> for specifics of history display. Fix at High when not used.
-	14	SOUT0	OUT	High	Asynchronous serial data OUT Serial data OUT pin for history display. Refer to the <i>S1R72U06 Development Support Manual</i> for specifics of history display. Leave open when not used.

DEBUG I/F (UVDD3 system)

BGA	QFP	Name	I/O	RESET	Pin description
-	16	DBGDCLK	OUT	High	Not used (*1)
-	18	DBGDT	BI(PU)	-	Not used (*2)
-	17	DBGST	OUT	Low	Not used (*1)

PU: Pull-up I/Os are used.

*1 Leave open.

*2 This is pulled up in the LSI. However, an external pull-up of about 10 kΩ is recommended.

GPI (CVDD system)

BGA	QFP	Name	I/O	RESET	Pin description
-	34	SPIxUART	IN	-	Setting pin 0: UART mode 1: SPI mode
-	35	HOSTxDEVICE	IN	-	Setting pin 1: HOST mode, 0: DEVICE mode Switching modes resets the LSI.
-	36	WAKEUP	IN	-	Wake-up pin Used to resume from SLEEP state. Rising edge activates the wake-up trigger.
-	38	INIT_BAUD	IN	-	Initial baud rate setting pin 1: 9600bps 0: 300bps UART baud rate can be set to between 300 bps and 3 Mbps using the serial port setting. Refer to the <i>S1R72U06 Technical Manual</i> for detailed instructions on making serial port settings.

GPO (CVDD system)

BGA	QFP	Name	I/O	RESET	Pin description
-	24	TPL	OUT	Low	Unsupported Device 1: Error, 0: - Used for USB Compliance Testing. Leave open when not used.
-	23	ManyDev	OUT	Low	Too Many Devices 1: Error, 0: - Used for USB Compliance Testing. Leave open when not used.
-	22	ManyHub	OUT	Low	Too Many Hubs 1: Error, 0: - Used for USB Compliance Testing. Leave open when not used.
-	21	VBUS_Cur	OUT	Low	VBUS Over Current 1: Error, 0: - Used for USB Compliance Testing. Leave open when not used.

6. Pin Functions

Regulator (VRIN system)					
BGA	QFP	Name	I/O	RESET	Pin description
-	4, 47	VRIN	Power	-	Regulator input Connect Cin = 1.0 μ F to each pin. <u>Make sure to keep this open when not using the regulator.</u>
-	45	VR0UT_Enb	IN	-	Enables the regulator Set this to the same level as VRIN when using the regulator. <u>Make sure to set this to Low when not using the regulator.</u>

VBUS SW (VBUS_5V_IN system)					
BGA	QFP	Name	I/O	RESET	Pin description
-	2	VBUS_5V_IN	Power	-	VBUS generation input Voltage input pin for built-in VBUS supply function. The power supply (VSWIN in 8.3.5) should be provided even when this function is not used.
-	1	VBUS_OUT	Power	-	VBUS output VBUS output pin for built-in VBUS supply function. Leave open when this function will not be used.

POWER					
BGA	QFP	Name	Voltage	Pin description	
-	5	UVDD3	3.3V	Power supply for USB When using regulator: Connect Cout = 1.0 μ F. When not using regulator: Apply the voltage indicated to the left.	
-	46	LVDD	1.8V	Internal power supply, test power supply, OSC power supply When using regulator: Connect Cout = 1.0 μ F. When not using regulator: Apply the voltage indicated to the left.	
-	32	CVDD	1.8 to 5.0V	Power supply for main CPU I/F	
-	3, 6, 20, 43, 48	VSS	0V	GND	

7. Commands

Communication with the main CPU is implemented via commands. For detailed information on commands, refer to the *S1R72U06 UART Interface Manual* and the *S1R72U06 SPI Interface Manual*.

8. Electrical Characteristics

8. Electrical Characteristics

8.1 Absolute Maximum Ratings

Item	Code	Rating	Unit
Power supply voltage	CVDD VRIN (*1)	-0.3 to 7.0	V
	UVDD3	-0.3 to 4.0	V
	LVDD (*2)	-0.3 to 2.5	V
Input voltage	VI (*3)	-0.3 to CVDD+0.5 -0.3 to UVDD3+0.5 -0.3 to LVDD+0.5	V
	VBUS_5V_IN	-0.3 to 7.0	V
Output voltage	VO (*3)	-0.3 to CVDD+0.5 -0.3 to UVDD3+0.5 -0.3 to LVDD+0.5	V
	VBUS_OUT	VBUS_5V_IN+0.3	V
Output current/pin	Iout	±10	mA
Storage temperature	Tstg	-65 to 150	°C

*1 $VRIN \geq UVDD3$, $VRIN \geq LVDD$

*2 $CVDD$, $UVDD3 \geq LVDD$

*3 Power supply voltages

8.2 Recommended Operating Conditions

Item	Code	Min.	Typ.	Max.	Uni
Power supply voltage	CVDD	1.65	1.80 to 5.00	5.50	V
	VRIN	3.00	3.30 to 5.00	5.50	V
	UVDD3	3.00	3.30	3.60	V
	LVDD	1.65	1.80	1.95	V
Input voltage	VI (*)	-0.3	-	CVDD+0.3 UVDD3+0.3 LVDD+0.3	V
Ambient temperature	T _a	-40	25	85	°C

* Power supply voltages for each pin

[Precautions for power ON sequence]

Be careful of the power supply timing when providing an external power supply without using a built-in regulator. Refer to “8.4.1 Power supply input/cutoff timing” for more information.

8.3 DC Characteristics

8.3.1 Current consumption

Item	Code	Condition	Min.	Typ.	Max.	Unit
Power supply current (*1)						
Power supply current	IDDH0	CVDD = 5.5V	-	5	-	mA
	IDDH1	UVDD3 = 3.6V	-	5 *2	-	mA
	IDDL	LVDD = 1.95V	-	25 *2	-	mA
	IDDR	VRIN = 5.5V	-	30 *3	-	mA
Power supply current (Static current) (*4)						
Power supply current	IDDS	Max. condition of each power supply Fixed to power supply or GND	-	50	-	μA
Input leak						
Input leakage current	IL	Max. condition of each power supply	-5	-	5	μA

*1 At recommended operating conditions (Ta = 25°C). Operating current for Seiko Epson evaluation board configuration.

*2 Operating current for Seiko Epson evaluation board configuration with external power supply and no built-in regulator.

*3 Operating current for Seiko Epson evaluation board configuration with built-in regulator.

*4 Static current when Ta = 25°C and when using regulator.

8. Electrical Characteristics

8.3.2 Input characteristics

Item	Code	Condition	Min.	Typ.	Max.	Unit
Input characteristics						
Pin:		LVDD-system pin				
"H" level input voltage	VIH1	LVDD = 1.95V	1.27	-	-	V
"L" level input voltage	VIL1	LVDD = 1.65V	-	-	0.57	V
Input characteristics (Schmitt)						
Pin:		CVDD- and UVDD3-system pin				
"H" level trigger voltage	VT1+	CVDD = 5.5V CVDD = 3.6V CVDD = 1.95V UVDD3 = 3.6V	-	-	4.00 2.52 1.36 2.52	V
"L" level trigger voltage	VT1-	CVDD = 4.5V CVDD = 3.0V CVDD = 1.65V UVDD3 = 3.0V	0.80 0.75 0.42 0.75	-	-	V
Hysteresis voltage	$\Delta V1$	CVDD = 4.5V CVDD = 3.0V CVDD = 1.65V UVDD3 = 3.0V	0.30 0.30 0.17 0.30	-	-	V
Schmitt input characteristics (USB: FS)						
Pin:		DP, DM				
"H" level trigger voltage	VTU+	UVDD3 = 3.6V	-	-	2.0	V
"L" level trigger voltage	VTU-	UVDD3 = 3.0V	0.8	-	-	V
Input characteristics (USB: FS differential input)						
Pin:		DP, DM pair				
Differential input sensitivity	VDSU	UVDD3 = 3.0V Differential input voltage: 0.8 to 2.5 V	0.2	-	-	V
Input characteristics						
Pin:		VBUSFLG, DBGDT				
Pull-up resistance	RPLU	VI = 0V (UVDD3 = 3.0V)	52	160	384	k Ω
Input characteristics						
Pin:		ATPGEN				
Pull-down resistance	RPLD	VI = CVDD (CVDD = 4.5V)	32	100	240	k Ω
		VI = CVDD (CVDD = 3.0V)	52	160	384	
		VI = CVDD (CVDD = 1.65V)	200	600	1440	
Input characteristics						
Pin:		TSTEN				
Pull-down resistance	RPLDL	VI = LVDD (LVDD = 1.65V)	40	120	288	k Ω
Input characteristics						
Pin name:		VBUS				
Pull-down resistance	RPLDB	VI = 5.0V	100	125	165	k Ω

8. Electrical Characteristics

8.3.3 Output characteristics

(V_{SS}=0V)

Item	Code	Condition	Min.	Typ.	Max.	Unit
Output characteristics	Pin:	SIO_READY, XIRQ_EVENT, XIRQ_STATUS, TPL, ManyDev, ManyHUB, VBUS_Cur, VBUSEN				
"H" level output voltage	VOH1	CVDD = 4.5V (IOH = -2.0mA) CVDD = 3.0V (IOH = -1.4mA) CVDD = 1.65V (IOH = -0.6mA) UVDD3 = 3.0V (IOH = -1.4mA)	CVDD - 0.4 CVDD - 0.4 CVDD - 0.4 UVDD3 - 0.4	-	-	V
"L" level output voltage	VOL1	CVDD = 4.5V (IOH = 2.0mA) CVDD = 3.0V (IOH = 1.4mA) CVDD = 1.65V (IOH = 0.6mA) UVDD3 = 3.0V (IOH = 1.4mA)	-	-	0.4 0.4 0.4 0.4	V
Output characteristics	Pin:	MISO, SOUT0, CLKOUT				
"H" level output voltage	VOH2	CVDD = 4.5V (IOH = -4.0mA) CVDD = 3.0V (IOH = -2.8mA) CVDD = 1.65V (IOH = -1.2mA) UVDD3 = 3.0V (IOH = -2.8mA)	CVDD - 0.4 CVDD - 0.4 CVDD - 0.4 UVDD3 - 0.4	-	-	V
"L" level output voltage	VOL2	CVDD = 4.5V (IOH = 4.0mA) CVDD = 3.0V (IOH = 2.8mA) CVDD = 1.65V (IOH = 1.2mA) UVDD3 = 3.0V (IOH = 2.8mA)	-	-	0.4 0.4 0.4 0.4	V
Output characteristics (USB: FS)	Pin:	DP, DM				
"H" level output voltage	VOHUF	UVDD3 = 3.0V	2.8	-	-	V
"L" level output voltage	VOLUF	UVDD3 = 3.6V	-	-	0.3	V
Output characteristics	Pin:	CVDD-system pin				
OFF-STATE leakage current	IOZ	CVDD = 5.5V VOH = CVDD VOL = VSS	-5	-	5	μA

8. Electrical Characteristics

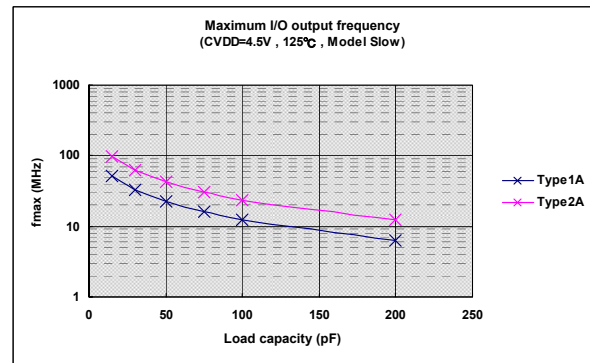
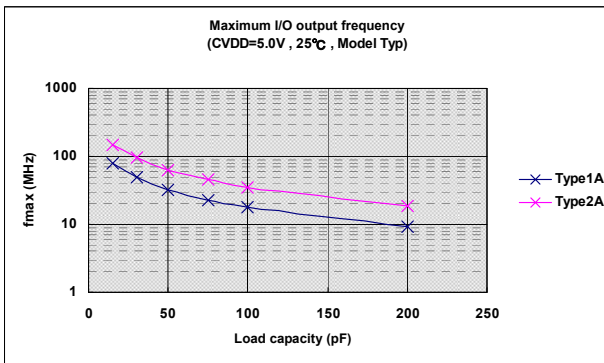
○ Fmax-Cl

<Output buffer types>

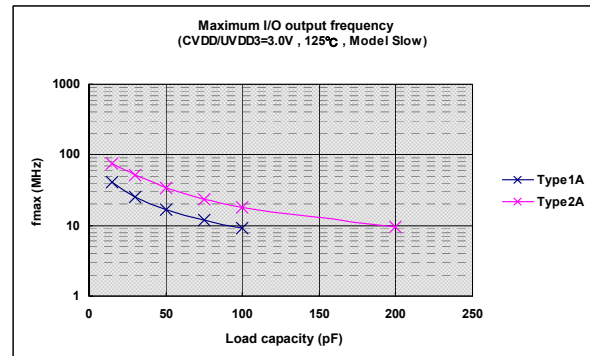
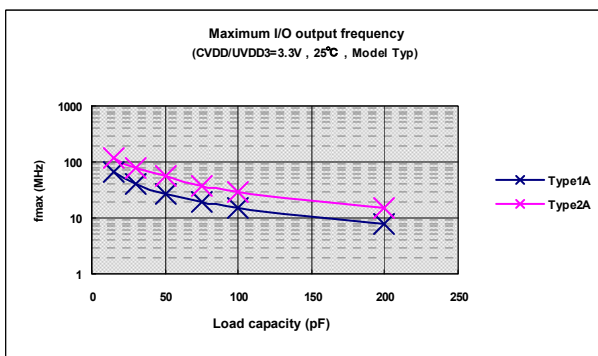
Type1A: SIO_READY, XIRQ_EVENT, XIRQ_STATUS, TPL, ManyDev, ManyHUB, VBUS_Cur, VBUSEN

Type2A: MISO, SOUT0, CLKOUT

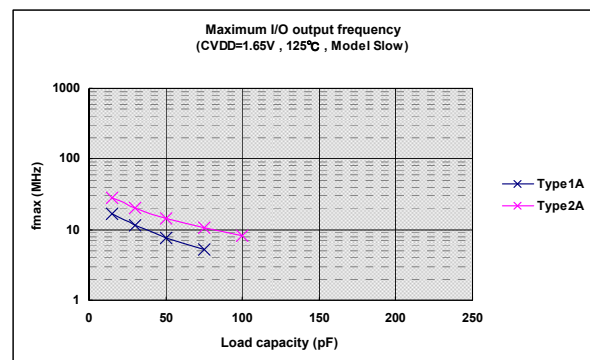
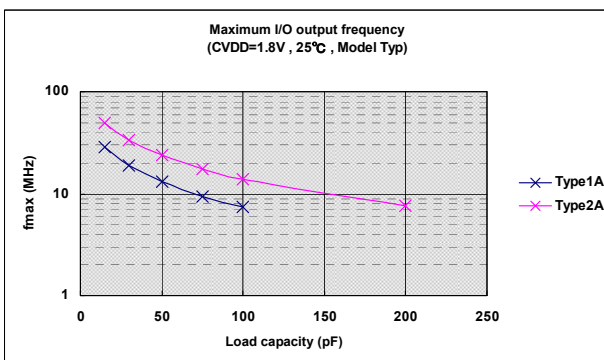
■ Using 5.0 V IO voltage



■ Using 3.3 V IO voltage



■ Using 1.8 V IO voltage



8.3.4 Pin capacitance

Item	Code	Condition	Min.	Typ.	Max.	Unit
Pin capacitance	Pin name:	All input pins				
Input pin capacitance	CI	f = 1MHz	-	-	8	pF
Pin capacitance	Pin name:	All output pins				
Output pin capacitance	CO	f = 1MHz	-	-	8	pF
Pin capacitance	Pin name:	All output pins except DP and DM				
Input/output pin capacitance	CB	f = 1MHz	-	-	8	pF
Pin capacitance	Pin name:	DP, DM				
Input/output pin capacitance (USB)	CBU	f = 1MHz	-	-	15	pF

8. Electrical Characteristics

8.3.5 VBUS supply function characteristics

Item	Code	Condition	Min.	Typ.	Max.	Unit
Input voltage	VSWIN		3.0	5.0	5.5	V
On resistance	RSWON	VBUS_5V_IN = 5.0V VBUS_5V_IN = 3.0V	-	2.4 3.5	4.0 -	Ω
Off leakage current	ISWOFF	VBUS_5V_IN = 5.0V VBUS_5V_IN = 3.0V	-	10 10	100 100	nA
Overcurrent detection	ISWLMT	VBUS_5V_IN = 5.0V VBUS_5V_IN = 3.0V	21 -	26 17	35 -	mA
Overcurrent response time	TSWOFF	Overcurrent → VBUS Off	300			μ s

8.3.6 Fail-safe cell

The S1R72U06 uses fail-safe cells for certain pins. Fail-safe cells have the following advantages:

- They prevent input leakage currents when a power supply is applied to input pins or input/output pins in the input state, even if the signal input exceeds the power supply voltage. (Note that a leakage current of approximately 30 μA will occur for pins with pull-up resistance.)
- No input leakage current occurs when the power supply is cut off, even when an external input signal is applied.

Note that while signals with a voltage level exceeding the operating voltage can be received, the signal voltage that can be applied to the fail-safe cell cannot exceed the absolute maximum rating.

<Fail-safe fitted pins>

MISO, MOSI, SCK, SS, SIO_READY, XIRQ_EVENT, XIRQ_STATUS, SPIxUART, HOSTxDEVICE, WAKEUP, INIT_BAUD, TPL, ManyDev, ManyHUB, VBUS_Cur, SIN0, SOUT0, VBUSFLG, VBUSEN, CLKOUT, CLKIN, CLK_Source, CLKSEL, DBGDCLK, DBGDT, DBGST, XRESET, ATPGEN

8. Electrical Characteristics

8.4 AC Characteristics

8.4.1 Power supply input/cutoff timing

A. Power supply input/cutoff timing (for LVDD \Rightarrow HVDD / HVDD \Rightarrow LVDD: recommended conditions)

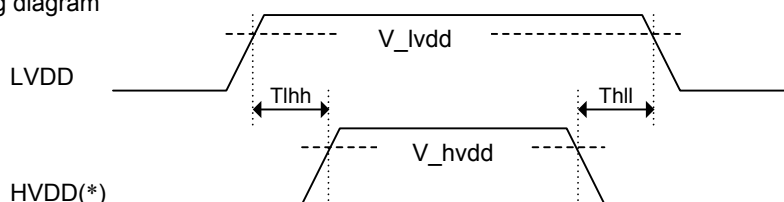
Timing parameters

Item	Code	Min.	Typ.	Max.	Unit
HVDD power supply input timing	Tlhh	0	-	10	sec
HVDD cutoff timing	Thll	0	-	10	sec

Voltage parameters

Item	Code	Voltage conditions		Unit
		Input	Cutoff	
LVDD initial voltage	V_lvdd	LVDD_min	LVDD_min	V
HVDD initial voltage	V_hvdd	HVDD_min	HVDD_min	V

Timing diagram



B. Power supply input/cutoff timing (for HVDD LVDD / LVDD \Rightarrow HVDD)

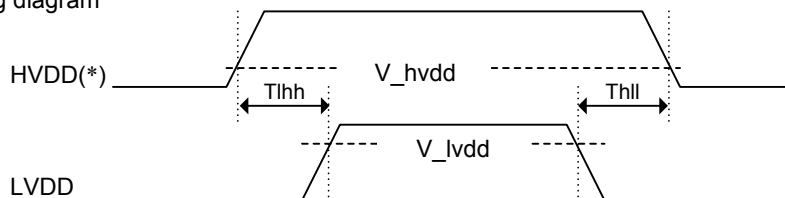
Timing parameters

Item	Code	Min.	Typ.	Max.	Unit
LVDD power supply input timing	Tlhh	0	-	1	sec
LVDD cutoff timing	Thll	0	-	1	sec

Voltage parameters

Item	Code	Voltage conditions		Unit
		Input	Cutoff	
LVDD initial voltage	V_lvdd	LVDD_min	LVDD_min	V
HVDD initial voltage	V_hvdd	0.1	0.1	V

Timing diagram

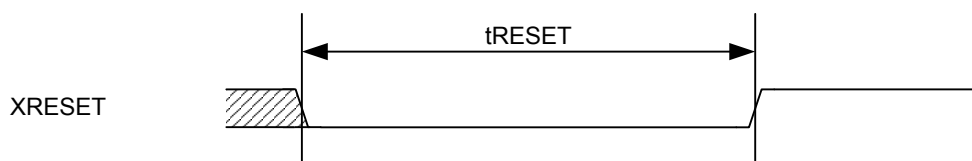


* HVDD refers to USB UVDD3 or interface CVDD.

* For LVDD \Rightarrow HVDD timing, refer to A for input and B for cutoff.

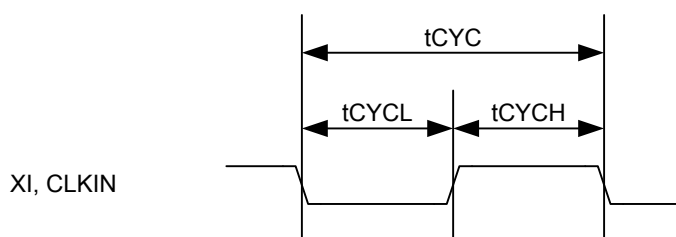
For HVDD \Rightarrow LVDD timing, refer to B for input and A for cutoff.

8.4.2 Reset timing



Code	Description	min	typ	max	Unit
tRESET	Reset pulse width	40	-	-	ns

8.4.3 Clock timing



Code	Description	Min.	Typ.	Max.	Unit
tCYC	Clock cycle (CLKSEL = "L")	-	12.000	-	MHz
tCYC	Clock cycle (CLKSEL = "H")	-	24.000	-	MHz
tCYCL tCYCH	Clock duty	45	50	55	%

* The clock source selected must satisfy the accuracy requirements under USB standards. FS: 2,500 ppm, LS: 15,000 ppm

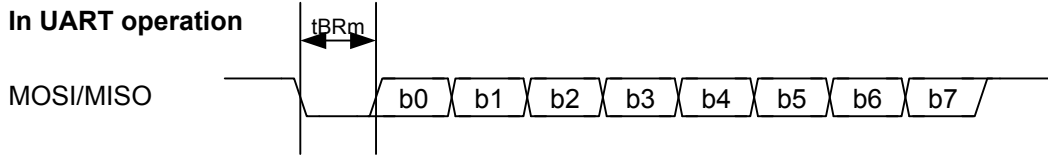
8.4.4 USB I/F timing

Complies with USB 2.0 (Universal Serial Bus Specification Revision 2.0) standard.

8. Electrical Characteristics

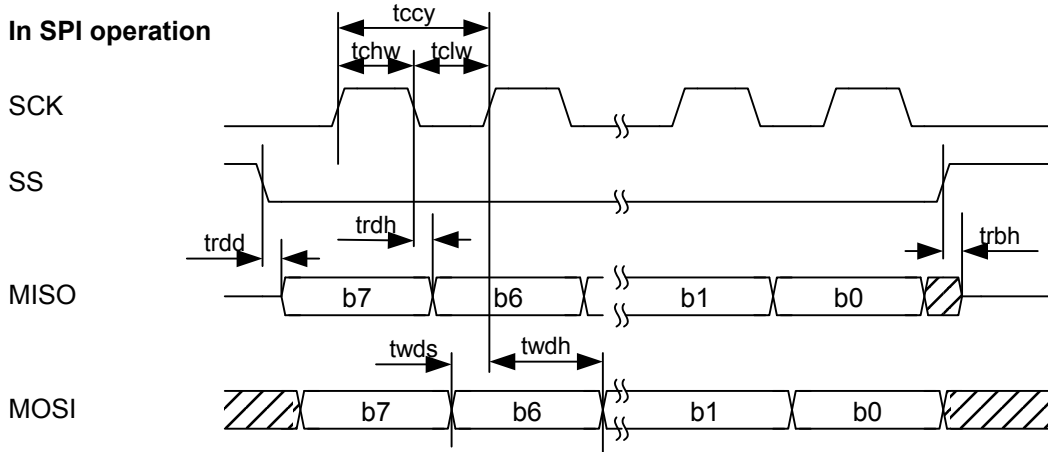
8.4.5 Serial I/F (main CPU) timing

In UART operation



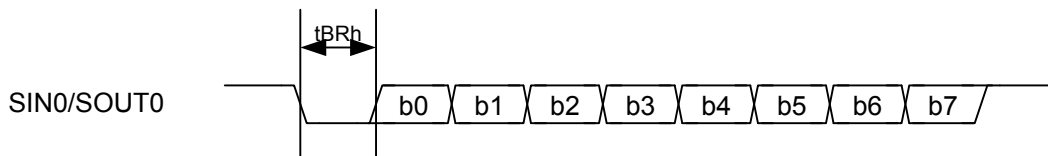
Code	Description	Min.	Typ.	Max.	Unit
t_{BRm}	Baud rate	300	-	3M	bps

In SPI operation



Code	Description	Min.	Typ.	Max.	Unit
t_{ccy}	Clock cycle	-	-	6M	Hz
t_{ch}	Clock High width	50	-	-	ns
t_{cl}	Clock Low width	50	-	-	ns
$trdd$	Data output start delay	2	-	20	ns
$trdh$	Data output switchover delay	-	-	35	ns
$trbh$	Data output hold	-	-	20	ns
$twds$	Received data setup	10	-	-	ns
$twdh$	Received data hold	5	-	-	ns

8.4.6 Serial I/F (history display) timing



Code	Description	Min.	Typ.	Max.	Unit
t_{BRh}	Baud rate	-	38400	-	bps

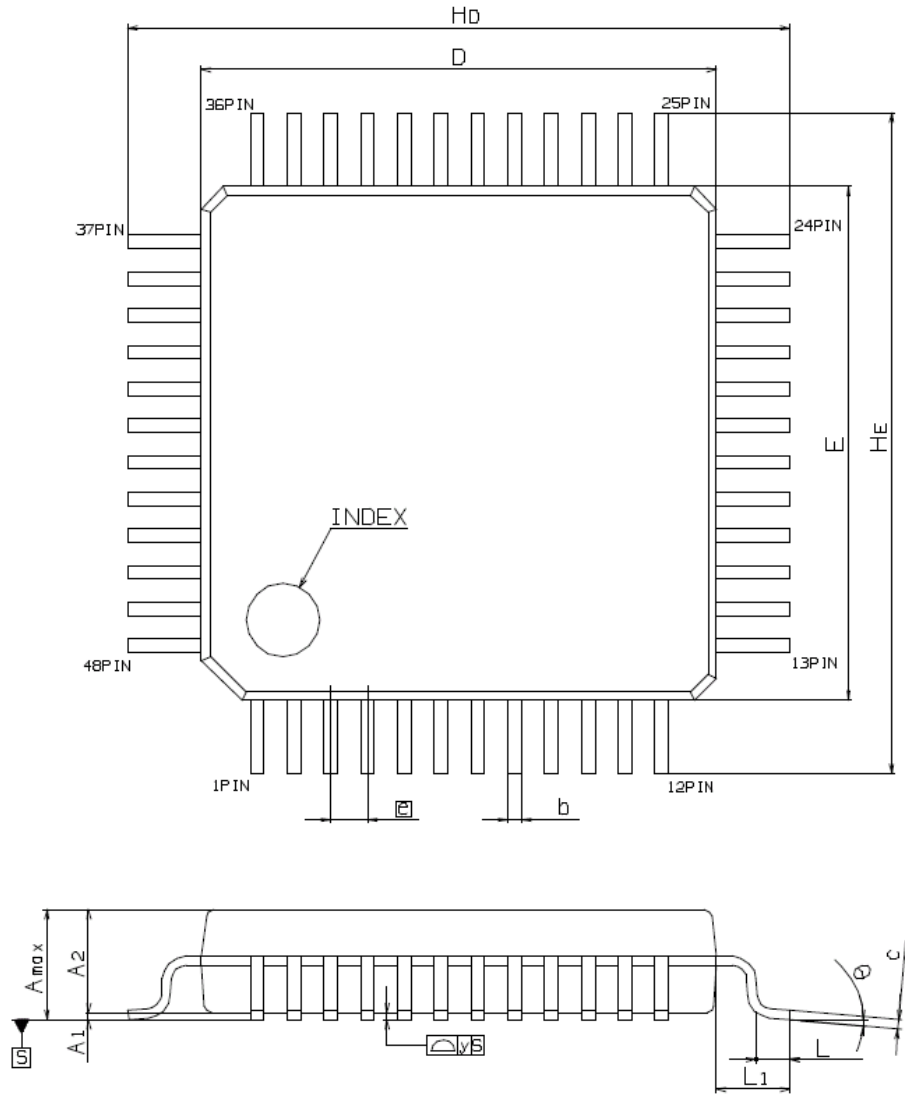
9. Connection Examples

Refer to the *S1R72U06 Evaluation Board Manual*.

10. External Dimensions Diagrams

10. External Dimensions Diagrams

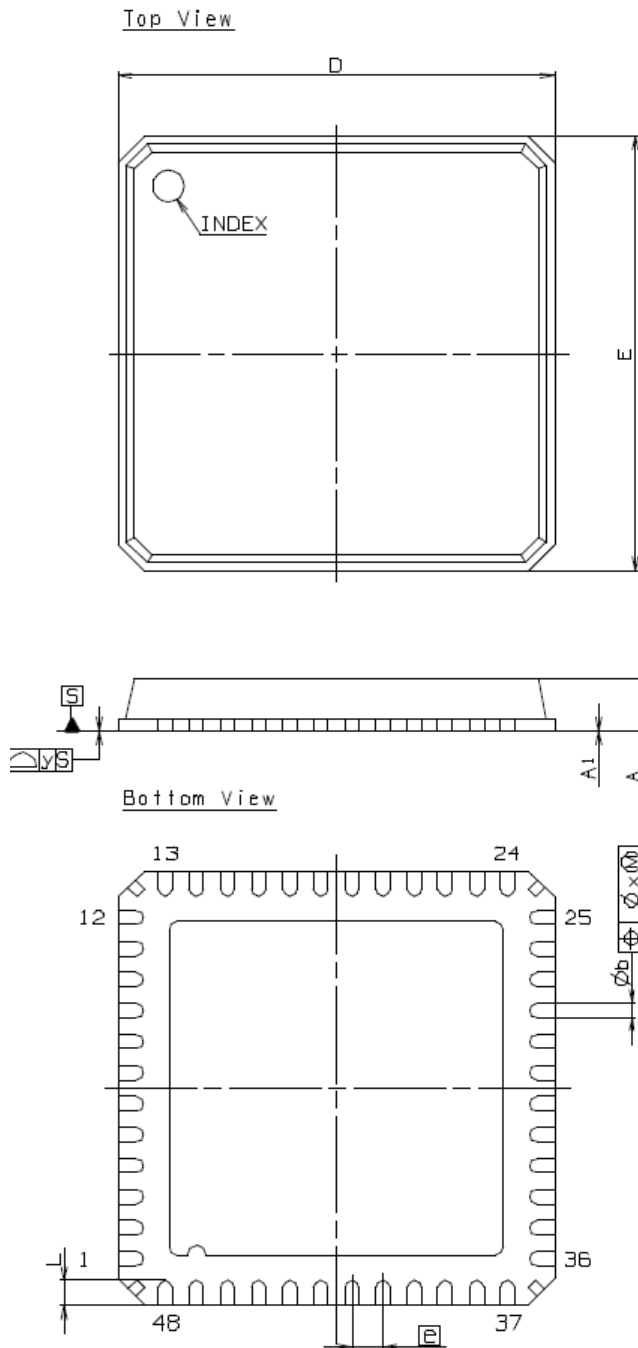
10.1 QFP12-48



Symbol	Dimension in Millimeters		
	Min	Nom	Max
E	-	7	-
D	-	7	-
A _{max}	-	-	1.7
A ₁	-	0.1	-
A ₂	-	1.4	-
Ⓜ	-	0.5	-
b	0.13	-	0.27
c	0.09	-	0.2
θ	0°	-	10°
L	0.3	-	0.7
L ₁	-	1	-
H _E	-	9	-
H _b	-	9	-
y	-	-	0.08

1 = 1mm

10.2 QFN7-48



Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	-	7	-
E	-	7	-
A	-	-	1
A1	0	-	-
b	0.17	-	0.3
ϕ	-	0.5	-
L	0.3	-	0.5
x	-	-	0.1
y	-	-	0.08

1 = 1mm

11. Product Codes

11. Product Codes

Product code	Description
S1R72U06F12E100	QFP12-48 package
S1R72U06F07E100	QFN7-48 package

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