

## **Enhanced Product (EP) Single Synchronous Buck Pulse-Width Modulation (PWM) Controller**

The ISL6406MREP and ISL6406MVEP are adjustable frequency, synchronous buck switching regulators optimized for generating lower voltages for distributed DC/DC architectures. Both devices feature an adjustable output voltage.

Designed to drive N-Channel MOSFETs in a synchronous buck topology, the ISL6406MREP and ISL6406MVEP integrate the control, output adjustment and protection functions into a single package.

The ISL6406MREP and ISL6406MVEP provide simple, single feedback loop, voltage-mode control with fast transient response. The output voltage can be precisely regulated to as low as 0.8V. The error amplifier features a 15MHz gain-bandwidth product and 6V/ $\mu$ s slew rate which enables high converter bandwidth for fast transient performance.

Protection from overcurrent conditions is provided by monitoring the  $r_{DS(ON)}$  of the upper MOSFET to inhibit PWM operation appropriately. This approach simplifies the implementation and improves efficiency by eliminating the need for a current sense resistor.

The wide programmable switching frequency range of 100kHz to 700kHz allows the use of small surface mount inductors and capacitors. The device also provides external frequency synchronization making it an ideal choice for DC/DC converter applications.

### **Device Information**

The specifications for an Enhanced Product (EP) device are defined in a Vendor Item Drawing (VID), which is controlled by the Defense Supply Center in Columbus (DSCC). "Hot-links" to the applicable VID and other supporting application information are provided on our website.

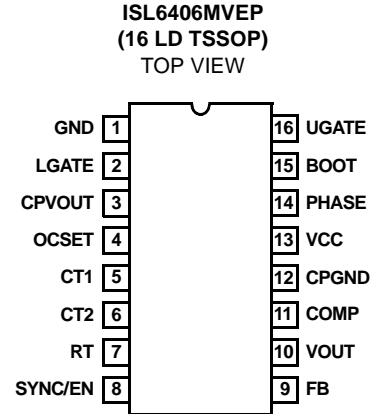
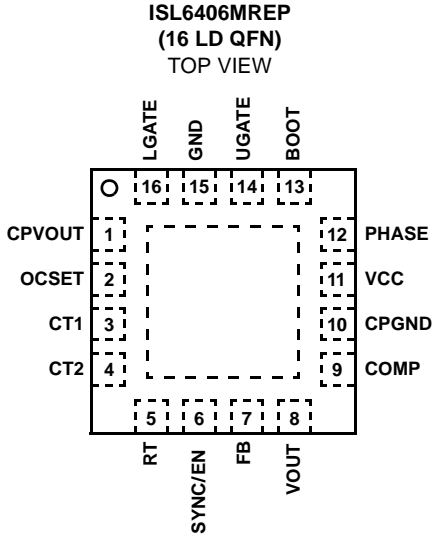
### **Features**

- Specifications per DSCC VID V62/08610
- Full Mil-Temp Electrical Performance from -55°C to +125°C
- Controlled Baseline with One Wafer Fabrication Site and One Assembly/Test Site
- Full Homogeneous Lot Processing in Wafer Fab
- No Combination of Wafer Fabrication Lots in Assembly
- Full Traceability Through Assembly and Test by Date/Trace Code Assignment
- Enhanced Process Change Notification
- Enhanced Obsolescence Management
- Eliminates Need for Up-Screening a COTS Component
- Operates from 3.3V/5V Input
- 0.8V to  $V_{IN}$  Output Range
  - 0.8V Internal Reference
  - $\pm 2.1\%$  Reference Accuracy Over-Temperature
- Simple Single-Loop Control Design
  - Voltage-Mode PWM Control
- Fast Transient Response
  - High-Bandwidth Error Amplifier
- Lossless, Programmable Overcurrent Protection
  - Uses Upper MOSFET's  $r_{DS(on)}$
- Programmable Switching Frequency 100kHz to 700kHz
- External Frequency Synchronization
- Internal Soft-Start

### **Applications**

- 3V/5V DC/DC Converter Modules
- Distributed DC/DC 3.3V, 2.5V and 1.8V Power Architectures for DSP, Logic, and Memory
- Power Supplies for Microprocessors
  - PCs
  - Embedded Controllers
- Memory Supplies
- Personal Computer Peripherals

**Pinouts**



**Ordering Information**

VENDOR PART NUMBER (Notes 1, 2)	VENDOR ITEM DRAWING	PART MARKING	TEMP. RANGE (°C)	PACKAGE	PKG. DWG. #
ISL6406MREP	V62/08610-01XB	6406MREP	-55 to +125	16 Ld 5x5 QFN	L16.5x5B
ISL6406MREP-TK	V62/08610-01XB	6406MREP	-55 to +125	16 Ld 5x5 QFN	L16.5x5B
ISL6406MVEP	V62/08610-01YB	6406 MVEP	-55 to +125	16 Ld TSSOP	M16.173
ISL6406MVEP-TK	V62/08610-01YB	6406 MVEP	-55 to +125	16 Ld TSSOP	M16.173

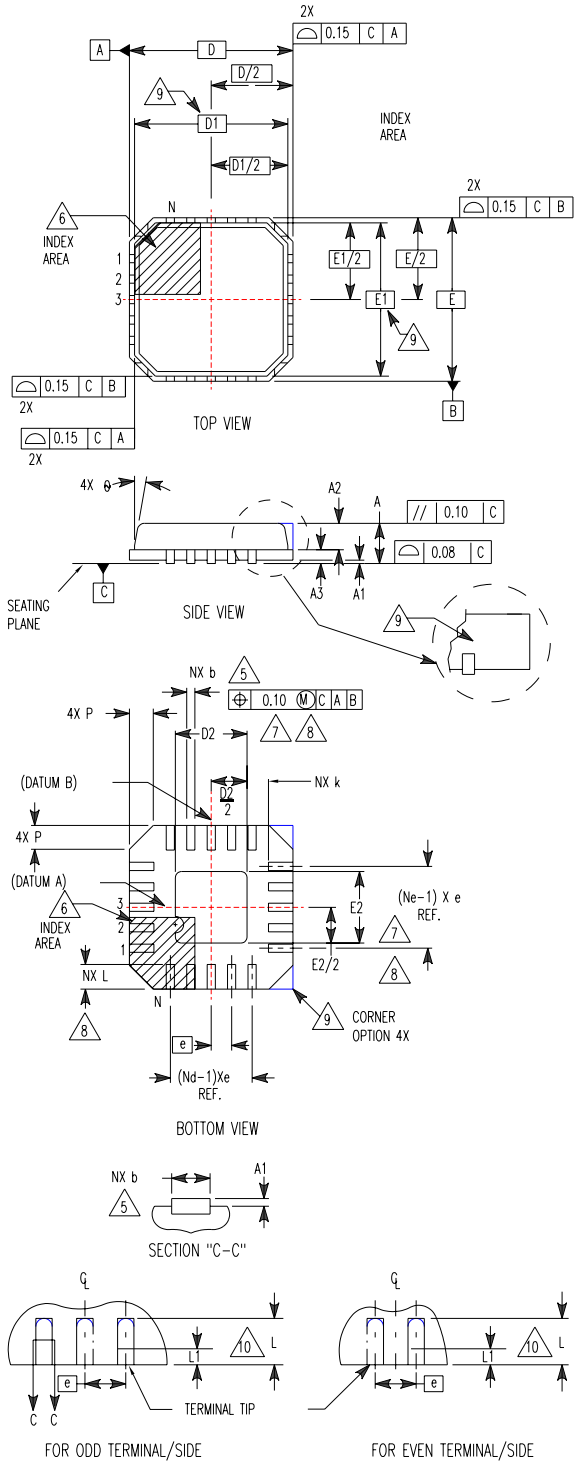
NOTES:

1. "-TK" suffix IS for 1,000 piece quantity tape and reel. Please refer to TB347 for details on reel specifications.
2. Devices must be procured to the VENDOR PART NUMBER.

**Quad Flat No-Lead Plastic Package (QFN)  
Micro Lead Frame Plastic Package (MLFP)**

**L16.5x5B**

16 LEAD QUAD FLAT NO-LEAD PLASTIC PACKAGE  
(COMPLIANT TO JEDEC MO-220VHHB ISSUE C)



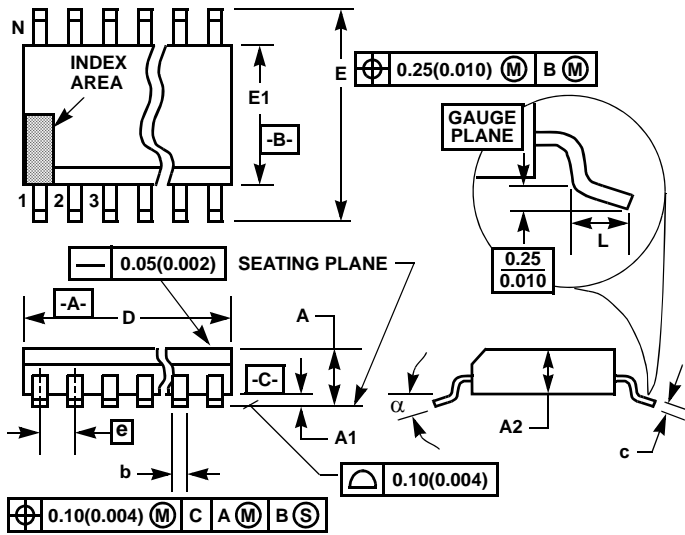
SYMBOL	MILLIMETERS			NOTES
	MIN	NOMINAL	MAX	
A	0.80	0.90	1.00	-
A1	-	-	0.05	-
A2	-	-	1.00	9
A3	0.20 REF			9
b	0.28	0.33	0.40	5, 8
D	5.00 BSC			-
D1	4.75 BSC			9
D2	2.95	3.10	3.25	7, 8
E	5.00 BSC			-
E1	4.75 BSC			9
E2	2.95	3.10	3.25	7, 8
e	0.80 BSC			-
k	0.25	-	-	-
L	0.35	0.60	0.75	8
L1	-	-	0.15	10
N	16			2
Nd	4			3
Ne	4			3
P	-	-	0.60	9
theta	-	-	12	9

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**NOTES:**

1. Dimensioning and tolerancing conform to ASME Y14.5-1994.
2. N is the number of terminals.
3. Nd and Ne refer to the number of terminals on each D and E.
4. All dimensions are in millimeters. Angles are in degrees.
5. Dimension b applies to the metallized terminal and is measured between 0.15mm and 0.30mm from the terminal tip.
6. The configuration of the pin #1 identifier is optional, but must be located within the zone indicated. The pin #1 identifier may be either a mold or mark feature.
7. Dimensions D2 and E2 are for the exposed pads which provide improved electrical and thermal performance.
8. Nominal dimensions are provided to assist with PCB Land Pattern Design efforts, see Intersil Technical Brief TB389.
9. Features and dimensions A2, A3, D1, E1, P & theta are present when Anvil singulation method is used and not present for saw singulation.
10. Depending on the method of lead termination at the edge of the package, a maximum 0.15mm pull back (L1) maybe present. L minus L1 to be equal to or greater than 0.3mm.

Thin Shrink Small Outline Plastic Packages (TSSOP)



M16.173  
16 LEAD THIN SHRINK SMALL OUTLINE PLASTIC PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	-	0.043	-	1.10	-
A1	0.002	0.006	0.05	0.15	-
A2	0.033	0.037	0.85	0.95	-
b	0.0075	0.012	0.19	0.30	9
c	0.0035	0.008	0.09	0.20	-
D	0.193	0.201	4.90	5.10	3
E1	0.169	0.177	4.30	4.50	4
e	0.026 BSC		0.65 BSC		-
E	0.246	0.256	6.25	6.50	-
L	0.020	0.028	0.50	0.70	6
N	16		16		7
α	0°	8°	0°	8°	-

NOTES:

1. These package dimensions are within allowable dimensions of JEDEC MO-153-AB, Issue E.
2. Dimensioning and tolerancing per ANSI Y14.5M-1982.
3. Dimension "D" does not include mold flash, protrusions or gate burrs. Mold flash, protrusion and gate burrs shall not exceed 0.15mm (0.006 inch) per side.
4. Dimension "E1" does not include interlead flash or protrusions. Interlead flash and protrusions shall not exceed 0.15mm (0.006 inch) per side.
5. The chamfer on the body is optional. If it is not present, a visual index feature must be located within the crosshatched area.
6. "L" is the length of terminal for soldering to a substrate.
7. "N" is the number of terminal positions.
8. Terminal numbers are shown for reference only.
9. Dimension "b" does not include dambar protrusion. Allowable dambar protrusion shall be 0.08mm (0.003 inch) total in excess of "b" dimension at maximum material condition. Minimum space between protrusion and adjacent lead is 0.07mm (0.0027 inch).
10. Controlling dimension: MILLIMETER. Converted inch dimensions are not necessarily exact. (Angles in degrees)

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All Intersil U.S. products are manufactured, assembled and tested utilizing ISO9000 quality systems. Intersil Corporation's quality certifications can be viewed at [www.intersil.com/design/quality](http://www.intersil.com/design/quality)

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