DECT SiGe Front End IC

Description

The U7004B is a monolithic SiGe transmit/receive front end IC with power amplifier, internally 50-Ω matched, low-noise amplifier and T/R switch driver. It is especially designed for operation in TDMA systems like DECT. Due to the ramp-control feature and a very low quiescent current an external switch transistor for V_S is not required.

Electrostatic sensitive device.
Observe precautions for handling.

Features

- Single 3-V supply voltage
- High-power-added efficient power amplifier (P_{out} typ. 26.5 dBm)
- Ramp-controlled output power
- Low-noise preamplifier (NF typ. 1.8 dB)
- Biasing for external PIN diode T/R switch
- Current-saving standby mode
- Few external components

Block Diagram

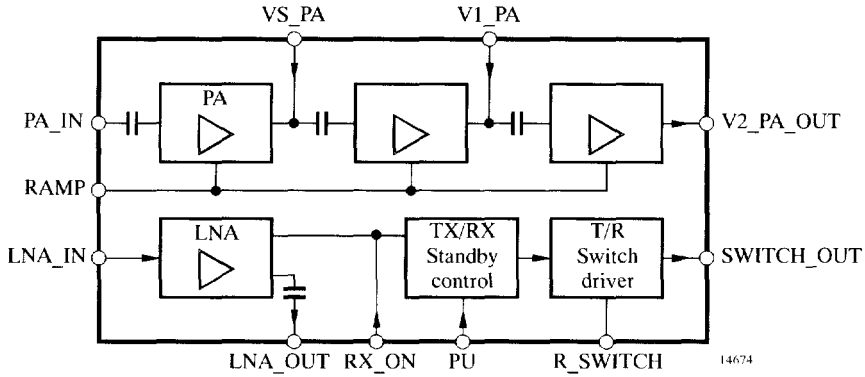

Figure 1. Block diagram

Ordering Information

Extended Type Number	Package	Remarks
U7004B-MFS	SSO20	Tube
U7004B-MFSG3	SSO20	Taped and reeled

Pin Description

Pin	Symbol	Function
1	R_SWITCH	Resistor to GND sets the PIN diode current
2	SWITCH_OUT	Switched current output for PIN diode
3	GND1	Ground
4	LNA_IN	Low-noise amplifier input
5	GND2	Ground
6	V1_PA	Inductor to power supply for power amplifier
7	GND3	Ground
8	GND4	Ground
9	GND5	Ground
10	V2_PA_OUT	Inductor to power supply and matching network for power amplifier output
11	GND6	Ground
12	GND7	Ground
13	VS_PA	Supply voltage for power amplifier
14	RAMP	Power-ramping control input
15	PA_IN	Power amplifier input
16	VS_LNA	Supply-voltage input for low-noise amplifier
17	GND8	Ground
18	LNA_OUT	Low-noise amplifier output
19	RX_ON	RX active high
20	PU	Power-up active high

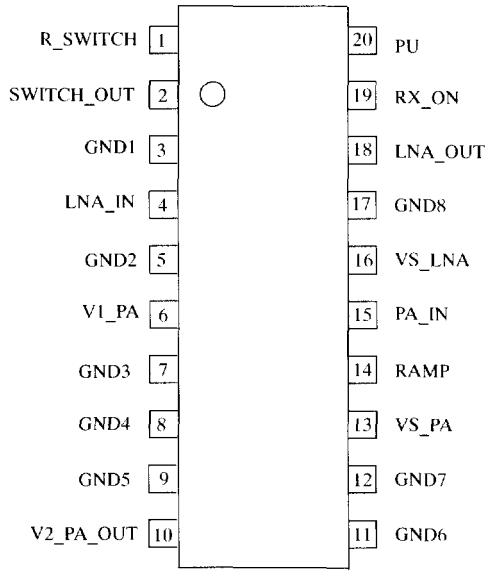

Figure 2. Pinning

Absolute Maximum Ratings

All voltages refer to GND (Pins 3, 5, 7, 8, 9, 11, 12 and 17)

Parameter		Symbol	Value	Unit
Supply voltage	Pins 6, 10, 13 and 16 (no RF)	V_S	5	V
Duty cycle PA			50	%
Burst duration PA			5	ms
Junction temperature		T_j	150	°C
Storage temperature		T_{stg}	-40 to +125	°C
Input power PA Pin 15		P_{inPA}	+10	dBm
Input power LNA Pin 4		P_{inLNA}	-5	dBm
ESD protection according to ESD-S5.2-1994			Class M1	

Thermal Resistance

Parameter	Symbol	Value	Unit
Junction ambient	R_{thJA}	95	K/W

Operating Range

All voltages refer to GND (Pins 3, 5, 7, 8, 9, 11, 12 and 17). The following table represents the sum of all supply currents depending on the TX/RX mode. Power supply points are VS_LNA, VS_PA, V1_PA, V2_PA_OUT.

Parameter		Symbol	Min.	Typ.	Max.	Unit
Supply voltage	Pins 6, 10 and 13	V_S	2.7	3.6	4.6	V
Supply voltage	Pin 16	V_S	2.7	3.6	4.6	V
Supply current	TX RX	I_S I_S		450 8		mA mA
Standby current	PU = 0	I_S		10		µA
Ambient temperature		T_{amb}	-25	+25	+70	°C

Electrical Characteristics

Test conditions (unless otherwise specified): V_S = 3.6 V, T_{amb} = 25°C, pulsed mode, duty cycle 4.17%, t_{on} = 417 µs

Parameter	Test Conditions / Pins	Symbol	Min.	Typ.	Max.	Unit
Power amplifier [1]						
Supply voltage	Pins 6, 10 and 13	V_S	2.7	3.6	4.6	V
Supply current	TX	I_{S_TX}		450		mA
	RX (PA off)	I_{S_RX}			10	µA
Standby current	Standby	$I_{S\_standby}$			10	µA
Frequency range	TX	f	1.88		1.94	GHz
Power gain	TX Pin 15 to Pin 10	Gp		28		dB
Gain-control range	TX	ΔGp		48		dB
Ramping voltage	TX, power gain (max) Pin 14	$V_{RAMP\ max}$		2.1		V
Ramping current		I_{RAMP}		0.5	2.0	mA
Power-added efficiency	TX	PAE		30		%
Saturated output power	TX, referred to Pin 10	P_{sat}		26.5		dBm
Input matching [2]	TX Pin 15	VSWRin		<2.0:1		
Output matching [2]	TX Pin 10	VSWRout		<2.0:1		
Harmonics @P 1dB	TX Pin 10	2 fo 3 fo		-30		dBc
Max. input power	Pin 15	P_{inPA}		10		dBm
Stability (non harmonic emission)	TX Pin 10 P_{in} = 2 dBm, V_{RAMP} = 2 V VSWRout <10:1 (all phases)			-60		dBc
T/R-switch driver (current programmed by external resistor from R_SWITCH to GND)						
Switch-out current output	Standby Pin 2	$I_{S\_O\_standby}$			2	µA
	RX	$I_{S\_O\_RX}$			2	µA
	TX @ 100 Ω	$I_{S\_O\_100}$		1		mA
	TX @ 1.2 kΩ	$I_{S\_O\_1k2}$		3		mA
	TX @ 33 kΩ	$I_{S\_O\_33k}$		10		mA

Note 1) Power amplifier shall be unconditional stable, maximum duty cycle 50%, maximum load mismatch and duration: load VSWR = 20:1 (all phases) 10 s, Z_G = 50 Ω

2) With external matching network (see figures 13 and 14)

Electrical Characteristics (continued)

Test conditions (unless otherwise specified): V_S = 3.6 V, T_{amb} = 25°C, pulsed mode, duty cycle 4.17%, t_{on} = 417 µs

Parameter	Test Conditions / Pins	Symbol	Min.	Typ.	Max.	Unit
Low-noise amplifier [3]						
Supply voltage	All Pin 16	V_S	2.7	3.6	4.6	V
Supply current	RX	I_S		8		mA
Supply current (LNA and control logic)	TX (control logic active) Pin 16	I_S		300		µA
Standby current	Standby Pin 16	I_S		1	10	µA
Frequency range	RX	f	1.88		1.94	GHz
Power gain	RX Pin 4 to Pin 18	Gp	17	19		dB
Noise figure	RX	NF		1.8	2.0	dB
Gain compression	RX, referred to Pin 18	P1dB		-7		dBm
3rd-order input interception point	RX	IIP3		-15		dBm
Input matching	RX	VSWRin		<2:1		
Output matching	RX	VSWRout		<2:1		
Logic input levels (RX_ON, PU)						
High input level	= '1' Pins 19 and 20	V_{iH}	2.4		V_S	V
Low input level	= '0'	V_{iL}	0		0.5	V
High input current	= '1'	I_{iH}		40		µA
Low input current	= '0'	I_{iL}		0		µA

3) Low-noise amplifier shall be unconditional stable

Control Logic

	PU
Power up	1
Standby	0

	RX_ON
RX mode	1
TX mode	0

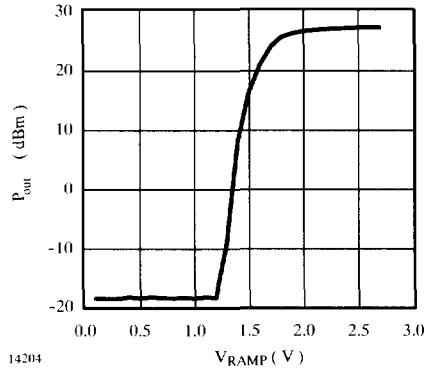

Figure 3. Output power vs. ramp voltage

Input / Output Circuits

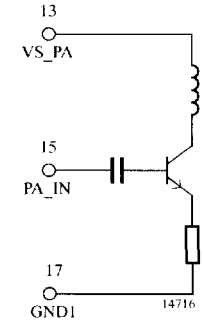

Figure 4.

Input / Output Circuits (continued)

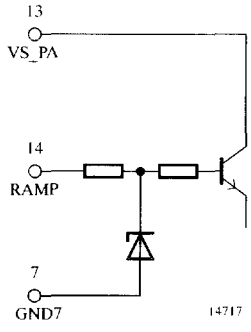

Figure 5.

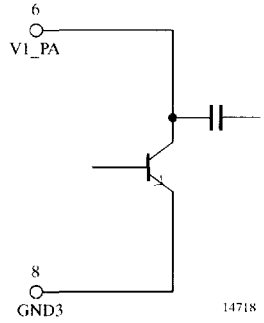

Figure 6.

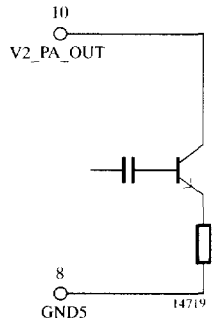

Figure 7.

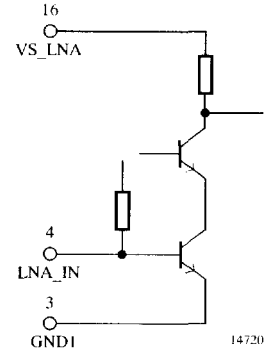

Figure 8.

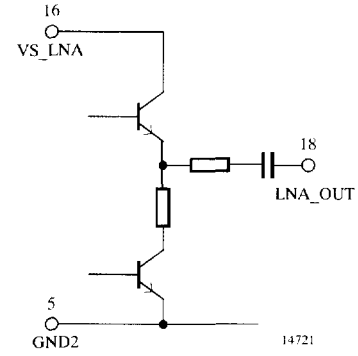

Figure 9.

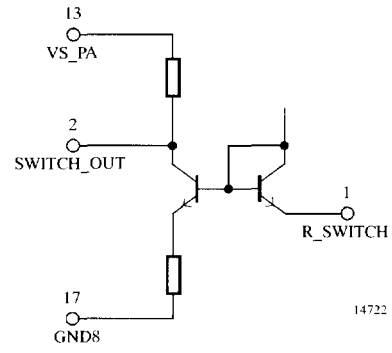

Figure 10.

Input / Output Circuits (continued)

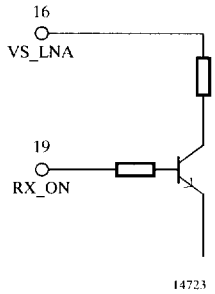

Figure 11.

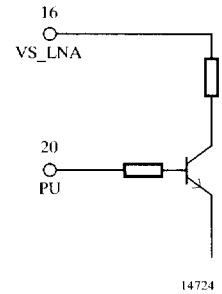

Figure 12.

Typical Application Circuit

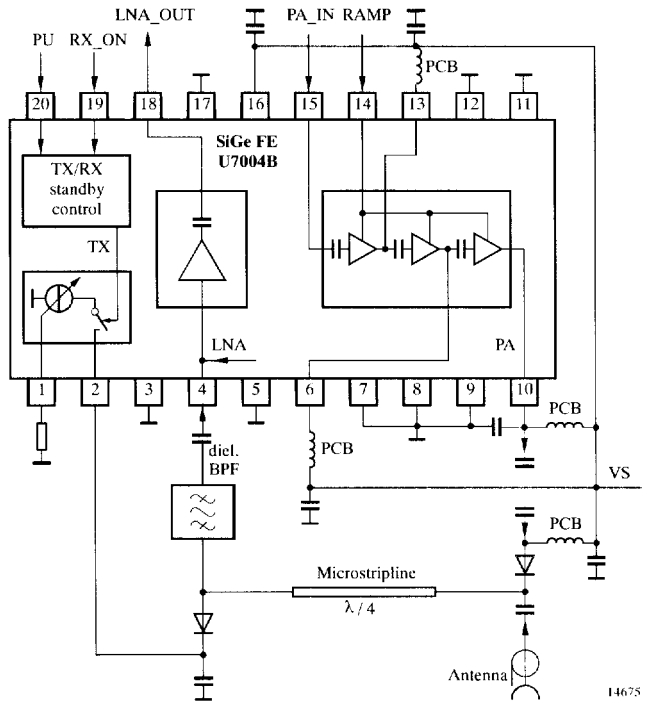

Figure 13. Typical schematic

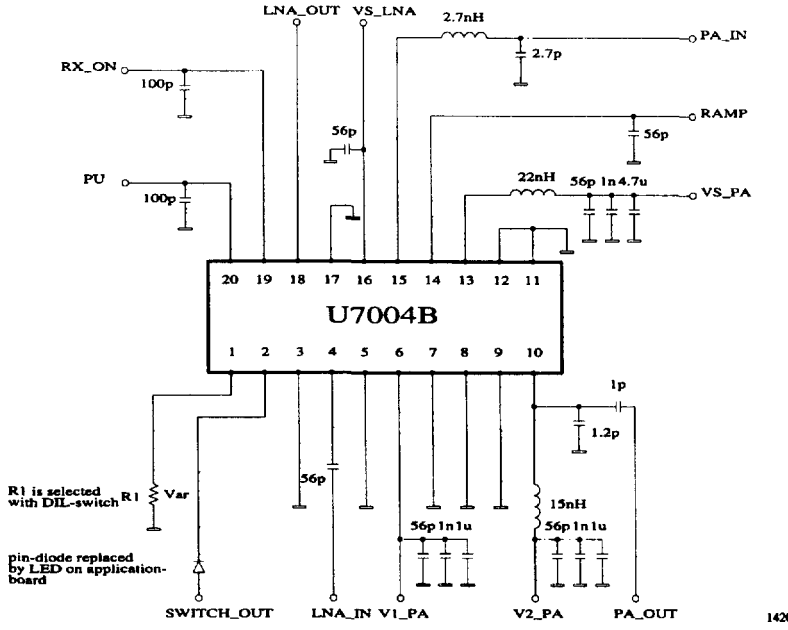

Figure 14. U7004B application board schematic

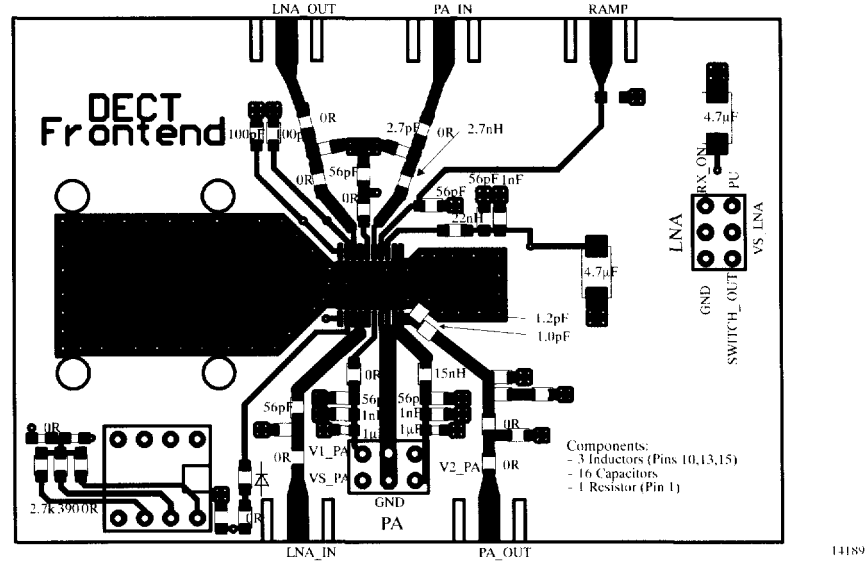

Figure 15. U7004B application board layout

Package Information

Package SSO20
Dimensions in mm