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Revision B2
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Sil3112A
PCI to Serial ATA Controller

MSL™ Technology
SATALink™

Silicon Image

Datasheet

Silicon Image, Inc.
1060 E Arques Ave
Sunnyvale CA 94085
(408) 616-4000
www.siliconimage.com

PCI LOCAL BUS

Silicon Image, Inc.
1060 E Arques Ave
Sunnyvale CA 94085, USA.

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Revision History:

Version	Comment	Date
Rev. A	First draft (derived from SiI3112 Data Sheet)	7/23/02
Rev. A1	Changed Absolute Maximum rating Voltage for VDDDO, VDDD and VDDI - Table 2-1 – Added VDDD for the DC specification – Table 2-2 – Changed VDDI (1.8 +/- 0.09 Volt) form (1.8 +/- 0.2 Volt) – Pin Descriptions -	8/27/02
Rev. A2	Revised Power supply current value Added pin 4 description Revised Table 3-1 SiI3112A Pin Listing	10/28/02
Rev. A3	Added Table 2-3 SATA Interface DC Specifications Added Table 2-4 SATA Interface Timing Specifications Added Table 2-5 SATA Interface Transmitter Output Jitter Characteristics Added Table 2-6 CLKI SerDes Reference Clock Input Requirements Removed Section 2-7 Power Supply Bypass Considerations Changed pin name for pin number 4 from SCAN_CK to NC	11/25/02
Rev. B	Removed CleanupAndRequestSense command code 13h in supported command list Defined RJ_{250UI}, DJ_{250UI} in Table 2-5 SATA Interface Transmitter Output Jitter Characteristics Removed Memory Write and Invalidate (Memory Write) support from PCI bus target operations	1/15/03
Rev. B1	Removed WriteFPDMAQueued and ReadFPDMAQueued command from supported command list Corrected inconsistence sentence (minor fixed including miss typing)	4/8/03
Rev. B2	Changed the rating for VIN in Table 2-1 Absolute Maxmum rating	6/30/03

1 Overview

The Silicon Image SiI3112A is a single-chip solution for a PCI to Serial ATA controller. It accepts host commands through the PCI bus, processes them and transfers data between the host and Serial ATA devices. It can be used to control two independent Serial ATA channels. Each channel has its own Serial ATA bus and will support one Serial ATA device. The SiI3112A supports a 32-bit 66 MHz PCI bus and the Serial ATA Generation 1 transfer rate of 1.5 Gb/s (150 MB/s).

1.1 Key Benefits

The Silicon Image SiI3112A PCI to Serial ATA Controller is the perfect single-chip solution for designs that need to accommodate storage peripherals with the new Serial ATA interface. Any system with a PCI bus interface can simply add the Serial ATA interface by adding a card with the SiI3112A and loading the driver into the system.

The SiI3112A comes complete with drivers for Windows 98, Windows Millennium, Windows NT 4.0, Windows 2000, XP, Netware and Linux.

1.2 Features

1.2.1 Overall Features

- Standalone PCI to Serial ATA host controller chip
- Compliant with PCI Specification, revision 2.2.
- Compliant with Programming Interface for Bus Master IDE Controller, revision 1.0.
- Driver support for Win98, WinME, NT4, Win2K, XP, Netware and Linux
- Supports up to 4Mbit external FLASH or EPROM for BIOS expansion.
- Supports an external EEPROM, FLASH or EPROM for programmable device ID, subsystem vendor ID, subsystem product ID and PCI sub-class code.
- Supports the Silicon Image specific driver for special chip functions.
- Fabricated in a 0.18µ CMOS process with a 1.8 volt core and 3.3 volt (5V tolerant) I/Os.
- Supports Plug and Play
- Supports SATA active signal for LED implementation
- Available in a 144-pin TQFP package.

1.2.2 PCI Features

- Supports 66 MHz PCI with 32-bit data.
- Supports PCI PERR and SERR reporting.
- Supports PCI bus master operations: Memory Read, Memory Read Multiple, and Memory Write.
- Supports PCI bus target operations: Configuration Read, Configuration Write, I/O Read, I/O Write, Memory Read, Memory Write, Memory Read Line (Memory Read) and Memory Read Multiple (Memory Read)
- Supports byte alignment for odd-byte PCI address access.
- Supports jumper configurable PCI class code.
- Supports programmable and EEPROM, FLASH and EPROM loadable PCI class code.
- Supports Base Address Register 5 in memory space.

1.2.3 Serial ATA Features

- Integrated Serial ATA Link and PHY logic
- Compliant with Serial ATA 1.0 specifications
- Supports two independent Serial ATA channels.
- Supports Serial ATA Generation 1 transfer rate of 1.5Gb/s.
- Supports Spread Spectrum in receiver
- Single PLL architecture, 1 PLL for both ports
- Programmable drive strengths for Backplane applications

1.2.4 Other Features

- Features independent 256-byte FIFOs (32-bit x 64 deep) per Serial ATA channel for host reads and writes.
- Features Serial ATA to PCI interrupt masking.
- Features Watch Dog Timer for fault resiliency.

1.3 Applications

- PC motherboards
- Serial ATA drive add on cards
- Serial ATA RAID controllers

1.4 References

For more details about the Serial ATA technology, the reader is referred to the following industry specifications:

- Serial ATA / High Speed Serialized AT Attachment specification, Revision 1.0
- PCI Local Bus Specification Revision 2.2
- Advanced Power Management Specification Revision 1.0
- PCI IDE Controller Specification Revision 1.0
- Programming Interface for Bus Master IDE Controller, Revision 1.0

1.5 Functional Description

SiI3112A is a PCI-to-Serial ATA controller chip that transfers data between the PCI bus and storage media (e.g. hard disk drive, etc). The SiI3112A consists of the following functional blocks:

- PCI Interface. Provides the interface to any system that has a PCI bus. Instructions and system clocks are based on this interface.
- Serial ATA Interface. Two separate channels (Primary and Secondary) to access storage media such as hard disk drive, floppy disk drive, CD-ROM.

1.6 Functional Block Diagram

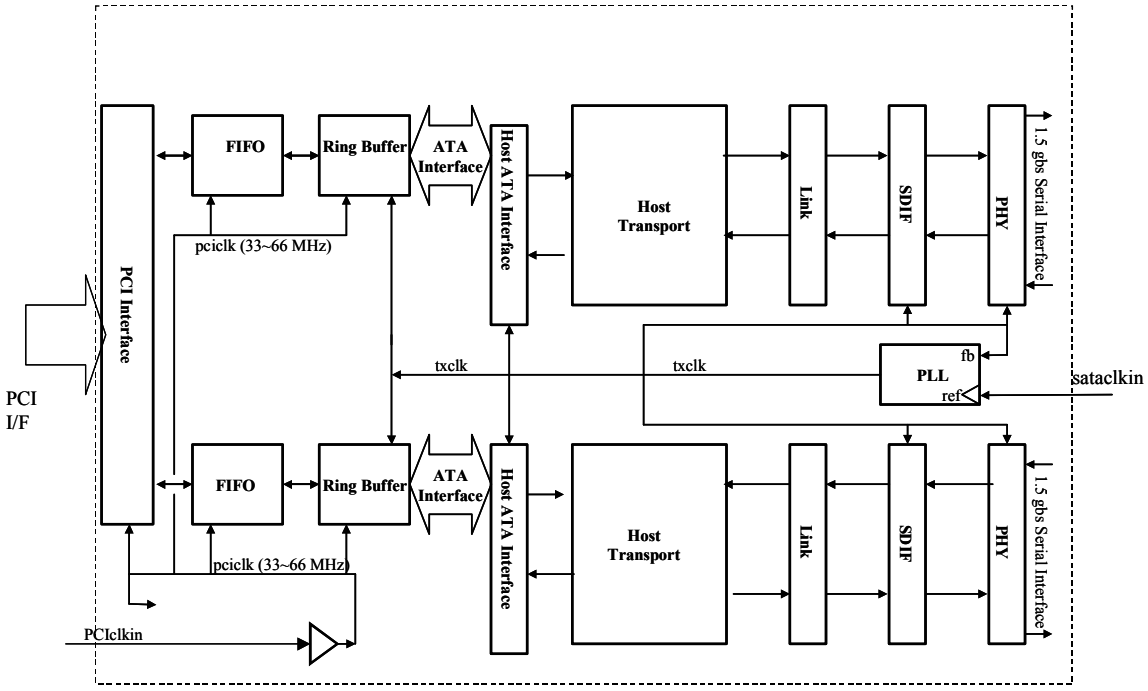

Figure 1-1 : SiI3112A Block Diagram

1.7 PCI Interface

The SiI3112A PCI interface is compliant with the PCI Local Bus Specification (Revision 2.2). The SiI3112A can act as a PCI master and a PCI slave, and contains the SiI3112A PCI configuration space and internal registers. When the SiI3112A needs to access shared memory, it becomes the bus master of the PCI bus and completes the memory cycle without external intervention. In the mode when it acts as a bridge between the PCI bus and the Serial ATA bus it will behave as a PCI slave.

1.8 PCI Initialization

Generally, when a system initializes a module containing a PCI device, the configuration manager reads the configuration space of each PCI device on the PCI bus. Hardware signals select a specific PCI device based on a bus number, a slot number, and a function number. If a device that is addressed (via signal lines) responds to the configuration cycle by claiming the bus, then that function's configuration space is read out from the device during the cycle. Since any PCI device can be a multifunction device, every supported function's configuration space needs to be read from the device. Based on the information read, the configuration manager will assign system resources to each supported function within the device. Sometimes new information needs to be written into the function's configuration space. This is accomplished with a configuration write cycle.

1.9 PCI Bus Operations

SiI3112A behaves either as a PCI master or a PCI slave device at any time and switches between these modes as required during device operation.

As a PCI slave, the SiI3112A responds to the following PCI bus operations:

- I/O Read
- I/O Write
- Configuration Read
- Configuration Write
- Memory Read
- Memory Write

  All other PCI cycles are ignored by the SiI3112A.

As a PCI master, the SiI3112A generates the following PCI bus operations:

- Memory Read Multiple
- Memory Read
- Memory Write

1.10 PCI Configuration Space

This section describes how the SiI3112A implements the required PCI configuration register space. The intent of PCI configuration space definition is to provide an appropriate set of configuration registers that satisfy the needs of current and anticipated system configuration mechanisms, without specifying those mechanisms or otherwise placing constraints on their use. These registers allow for:

- Full device relocation (including interrupt binding)
- Installation, configurations, and booting without user interventions
- System address map construction by device-independent software

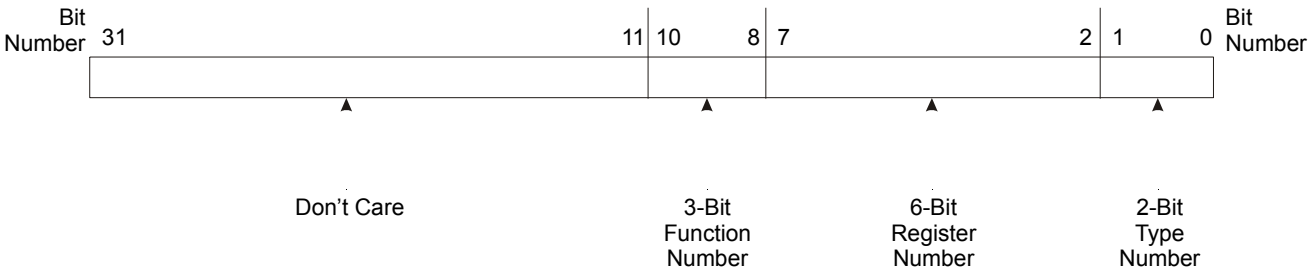

Figure 1-2: Address Lines During Configuration Cycle

SiI3112A only responds to Type 0 configuration cycles. Type 1 cycles, which pass a configuration request on to another PCI bus, are ignored.

The address phase during a SiI3112A configuration cycle indicates the function number and register number being addressed which can be decoded by observing the status of the address lines AD[31:0].

The value of the signal lines AD[7:2] during the address phase of configuration cycles selects the register of the configuration space to access. Valid values are between 0 and 15, inclusive. Accessing registers outside this range results in an all-0s value being returned on reads, and no action being taken on writes.

The Class Code register contains the Class Code, Sub-Class Code, and Register-Level Programming Interface registers.

All writable bits in the configuration space are reset to 0 by the hardware reset, PCI RESET (RST#) asserted. After reset, SiI3112A is disabled and will only respond to PCI configuration write and PCI configuration read cycles.

1.11 Deviations from the Specification

The SiI3112A product has been developed and tested to the specification listed in this document. As a result of testing and customer feedback, we may become aware of deviations to the specification that could affect the component's operation. To ensure awareness of these deviations by anyone considering the use of the SiI3112A, we have included an Errata section at the end of this specification. Please ensure that the Errata section is carefully reviewed. It is also important that you have the most current version of this specification. If there are any questions, please contact Silicon Image, Inc.

2 Electrical Characteristics

2.1 Device Electrical Characteristics

Specifications are for Commercial Temperature range, 0°C to +70°C, unless otherwise specified.

Symbol	Parameter	Ratings	Unit
VDDO	I/O Supply Voltage	4.0	V
VDDI, VDDD	Analog Supply Voltage Digital Supply Voltage	2.15	V
V_{IN}	Input Voltage	-0.3 ~ VDD+0.3	V
I_{OUT}	DC Output Current	16	mA
θ_{JA}	Thermal Resistance (Junction to Ambient)	39	°C/W
T_{STG}	Storage Temperature	-65 ~ 150	°C

Table 2-1 Absolute Maximum Ratings

Symbol	Parameter	Condition	Type	Limits			Unit
				Min	Typ	Max	
VDDI , VDDD	Supply Voltage (Digital, Analog)			1.71	1.8	1.89	V
VDDO	Supply Voltage(I/O)	-	-	3.0	3.3	3.6	V
$IDD_{1.8V}$	1.8V Supply Current				236[1]	285[2]	mA
$IDD_{3.3V}$	3.3V Supply Current	C_{LOAD}= 20pF			12[1]	30[2]	mA
V_{IH}	Input High Voltage	-	3.3V PCI	0.5xVDD	-	-	V
		-	Non-PCI	2.0	-	-	
V_{IL}	Input Low Voltage	-	3.3V PCI	-	-	0.3xVDD	V
		-	Non-PCI	-	-	0.8	
V+	Input High Voltage	-	Schmitt	-	1.8	2.3	V
V-	Input Low Voltage	-	Schmitt	0.5	0.9	-	V
V_H	Hysteresis Voltage	-	Schmitt	0.4	-	-	V
I_{IH}	Input High Current	V_{IN} = VDD	-	-10	-	10	µA
I_{IL}	Input Low Current	V_{IN} = VSS	-	-10	-	10	µA
V_{OH}	Output High Voltage	-	-	2.4	-	-	V
V_{OL}	Output Low Voltage	-	-	-	-	0.4	V
I_{OZ}	3-State Leakage Current	-	-	-10	-	10	µA

Notes: [1] Using the random data pattern (read/write operation) at 1.8V or 3.3V power supply, PCI interface = 33MHz
[2] Using the maximum toggling data pattern (read/write operation) at 1.89V or 3.6V power supply , PCI interface = 66MHz

Table 2-2 DC Specifications

Symbol	Parameter	Condition	Limits			Unit
			Min	Typ	Max	
V_{DOUT}	TX+/TX- differential peak-to-peak voltage swing.	Terminated by 50 Ohms. Tx Swing Value = 00	400	500	600	mV
V_{DIN}	RX+/RX- differential peak-to-peak input sensitivity		325			mV
V_{DIH}	RX+/RX- differential Input common-mode voltage		200	300	450	mV
V_{DOH}	TX+/TX-differential Output common-mode voltage		200	300	450	mV
Z_{DIN}	Differential input impedance	REXT = 1k 1% for 25MHz SerDes Ref Clk REXT = 4.99k 1% for 100MHz SerDes Ref Clk	85	100	115	ohms
Z_{DOUT}	Differential output impedance	REXT = 1k 1% for 25MHz SerDes Ref Clk REXT = 4.99k 1% for 100MHz SerDes Ref Clk	85	100	115	ohms

Table 2-3 SATA Interface DC Specifications

2.2 SATA Interface Timing Specifications

Symbol	Parameter	Condition	Limits			Unit
			Min	Typ	Max	
$T_{TX\_RISE\_FALL}$	Rise and Fall time at transmitter	20%-80%	133		274	ps
T_{TX_SKEW}	Tx differential skew				20	ps
$T_{TX\_DC\_FREQ}$	Tx DC clock frequency skew		-350		+350	ppm
$T_{TX\_AC\_FREQ}$	Tx AC clock frequency skew	SerDes Ref Clk = SSC AC modulation, subject to the "Downspread SSC" triangular modulation (30-33KHz) profile per 6.6.4.5 in SATA 1.0 specification	-5000		+0	ppm

Table 2-4 SATA Interface Timing Specifications

2.3 SATA Interface Transmitter Output Jitter Characteristics

Symbol	Parameter	Condition	Limits			Unit
			Min	Typ	Max	
RJ_{5UI}	5UI later Random Jitter	Measured at Tx output pins 1sigma deviation		3.6		ps rms
RJ_{250UI}	250UI later Random Jitter	Measured at Tx output pins 1sigma deviation		4.7		ps rms
DJ_{5UI}	5UI later Deterministic Jitter	Measured at Tx output pins peak to peak phase variation Random data pattern		20		ps
DJ_{250UI}	250UI later Deterministic Jitter	Measured at Tx output pins peak to peak phase variation Random data pattern		25		ps

Table 2-5 SATA Interface Transmitter Output Jitter Characteristics

2.4 CLKI SerDes Reference Clock Input Requirements

Symbol	Parameter	Condition	Limits			Unit
			Min	Typ	Max	
T_{CLKI_FREQ}	Norminal Frequency	REXT = 1k 1% REXT = 4.99k 1%		25 100		MHz
T_{CLKI_J}	CLKI frequency tolerance		-100		+100	ppm
$T_{CLKI\_RISE\_FALL}$	Rise and Fall time at CLKI	25MHz reference clock, 20%-80% 100MHz reference clock, 20%-80%			4 2	ns
$T_{CLKI\_RC\_DUTY}$	CLKI duty cycle	20%-80%	40		60	%

Table 2-6 CLKI SerDes Reference Clock Input Requirements

2.5 PCI 33 MHz Timing Specifications

Symbol	Parameter	Limits		Unit
		Min	Max	
T_{VAL}	CLK to Signal Valid – Bussed Signals	2.0	11.0	ns
$T_{VAL\ (PTP)}$	CLK to Signal Valid – Point to Point	2.0	11.0	ns
T_{ON}	Float to Active Delay	2.0	-	ns
T_{OFF}	Active to Float Delay	-	28.0	ns
T_{SU}	Input Setup Time – Bussed Signals	7.0	-	ns
$T_{SU\ (PTP)}$	Input Setup Time – Point to Point	10.0	-	ns
T_{H}	Input Hold Time	0.0	-	ns

Table 2-7 PCI 33 MHz Timing Specifications

2.6 PCI 66 MHz Timing Specifications

Symbol	Parameter	Limits		Unit
		Min	Max	
T_{VAL}	CLK to Signal Valid – Bussed Signals	2.0	6.0	ns
$T_{VAL\ (PTP)}$	CLK to Signal Valid – Point to Point	2.0	6.0	ns
T_{ON}	Float to Active Delay	2.0		ns
T_{OFF}	Active to Float Delay		14.0	ns
T_{SU}	Input Setup Time – Bussed Signals	3.0		ns
$T_{SU\ (PTP)}$	Input Setup Time – Point to Point	5.0		ns
T_{H}	Input Hold Time	0.0		ns

Table 2-8 PCI 66 MHz Timing Specifications

3 Pin Definition

3.1 SiI3112A Pin Listing

This section describes the pin-out of the SiI3112A PCI-to-Serial ATA host controller. Table 3-1 gives the pin numbers, pin names, pin types, drive types where applicable, internal resistors where applicable, and descriptions.

Pin #	Pin Name	Type	Drive	Internal Resistor	Description
1	VSS	GND	-	-	Ground
2	SCAN_EN	I	-	PD – 60k	Internal Scan Enable
3	VDDO	PWR			3.3Power
4	NC				
5	GNDD	GND	-	-	Digital Ground
6	VDDD	PWR	-	-	1.8V SerDes Power
7	GNDD	GND	-	-	Digital Ground
8	GNDA	GND	-	-	Analog Ground
9	RxP2	I			Channel 2 Differential Receive +ve
10	RxN2	I			Channel 2 Differential Receive -ve
11	GNDA	GND	-	-	Analog Ground
12	VDDD	PWR	-	-	1.8V SerDes Power
13	GNDD	GND	-	-	Digital Ground
14	GNDA	GND	-	-	Analog Ground
15	TxN2	O			Channel 2 Differential Transmit -ve
16	TxP2	O			Channel 2 Differential Transmit +ve
17	GNDA	GND	-	-	Analog Ground
18	GNDD	GND	-	-	Digital Ground
19	VDDD	PWR	-	-	1.8V SerDes Power
20	GNDD	GND	-	-	Digital Ground
21	GNDA	GND	-	-	Analog Ground
22	TxP1	O			Channel 1 Differential Transmit +ve
23	TxN1	O			Channel 1 Differential Transmit -ve
24	GNDA	GND	-	-	Analog Ground
25	VDDD	PWR	-	-	1.8V SerDes Power
26	GNDD	GND	-	-	Digital Ground
27	GNDA	GND	-	-	Analog Ground
28	RxN1	I			Channel 1 Differential Receive -ve
29	RxP1	I			Channel 1 Differential Receive +ve
30	GNDA	GND	-	-	Analog Ground
31	GNDD	GND	-	-	Digital Ground
32	VDDD	PWR	-	-	1.8V SerDes Power

Pin #	Pin Name	Type	Drive	Internal Resistor	Description
33	REXT	I			External Reference Resistor Input
34	GNDA	GND	-	-	Analog Ground
35	XTALI/CLKI	I			Crystal Oscillator Input or external clock input
36	XTALO	O			Crystal Oscillator Output
37	VDDO	PWR			3.3V supply for Crystal Oscillator
38	VSS	GND	-	-	Ground
39	VDDI	PWR	-	-	1.8V Volt Internal Core Power
40	EEPROM_SDAT	I/O		PU – 70k	EEPROM Serial Data
41	EEPROM_SCLK	I/O		PU – 70k	EEPROM Serial Clock
42	FL_ADDR[00] / IDE_CFG	I/O		PU – 70k	Flash Memory Address 0 / IDE-RAID Configuration
43	FL_ADDR[01] / BA5_EN	I/O		PU – 70k	Flash Memory Address 1 / Base Address Register 5 Enable
44	FL_ADDR[02]	O			Flash Memory Address 2
45	FL_WR_N	O		-	Flash Memory Write Strobe
46	VDDO	PWR	-	-	3.3 Volt Power
47	VSS	GND	-	-	Ground
48	FL_RD_N	O		-	Flash Memory Read Strobe
49	FL_ADDR[03]	O			Flash Memory Address 3
50	FL_ADDR[04]	O			Flash Memory Address 4
51	FL_ADDR[05]	O			Flash Memory Address 5
52	FL_ADDR[06]	O			Flash Memory Address 6
53	FL_ADDR[07]	O			Flash Memory Address 7
54	FL_ADDR[08]	O			Flash Memory Address 8
55	FL_ADDR[09]	O			Flash Memory Address 9
56	VDDI	PWR	-	-	1.8V Internal core Power
57	VSS	GND	-	-	Ground
58	FL_ADDR[10]	O			Flash Memory Address 10
59	FL_ADDR[11]	O			Flash Memory Address 11
60	FL_ADDR[12]	O			Flash Memory Address 12
61	FL_ADDR[13]	O			Flash Memory Address 13
62	FL_ADDR[14]	O			Flash Memory Address 14
63	FL_ADDR[15]	O		PU – 70k	Flash Memory Address 15
64	FL_ADDR[16]	O		PU – 70k	Flash Memory Address 16
65	FL_ADDR[17]	O		PU – 70k	Flash Memory Address 17
66	FL_ADDR[18]	O		PU – 70k	Flash Memory Address 18
67	TEST_MODE	I	-	PD – 60k	Test Mode Enable
68	FL_DATA[00]	I/O		PU – 70k	Flash Memory Data 0
69	FL_DATA[01]	I/O		PU – 70k	Flash Memory Data 1
70	FL_DATA[02]	I/O		PU – 70k	Flash Memory Data 2

Pin #	Pin Name	Type	Drive	Internal Resistor	Description
71	FL_DATA[03]	I/O		PU – 70k	Flash Memory Data 3
72	VDDO	PWR	-	-	3.3 Volt Power
73	VSS	GND	-	-	Ground
74	FL_DATA[04]	I/O		PU – 70k	Flash Memory Data 4
75	FL_DATA[05]	I/O		PU – 70k	Flash Memory Data 5
76	FL_DATA[06]	I/O		PU – 70k	Flash Memory Data 6
77	FL_DATA[07]	I/O		PU – 70k	Flash Memory Data 7
78	VSS	GND	-	-	Ground
79	VDDI	PWR	-	-	1.8V Internal core Power
80	VSS	GND	-	-	Ground
81	VDDI	PWR	-	-	1.8V Internal core Power
82	PCI_INTA_N	OD	PCI	-	PCI Interrupt
83	PCI_RST_N	I-Schmitt	-	-	PCI Reset
84	PCI_CLK	I	-	-	PCI Clock
85	PCI_GNT_N	I	-	-	PCI Bus Grant
86	PCI_REQ_N	T	PCI	-	PCI Bus Request
87	VDDO	PWR	-	-	3.3 Volt Power
88	VSS	GND	-	-	Ground
89	PCI_AD31	I/O	PCI	-	PCI Address/Data
90	PCI_AD30	I/O	PCI	-	PCI Address/Data
91	PCI_AD29	I/O	PCI	-	PCI Address/Data
92	PCI_AD28	I/O	PCI	-	PCI Address/Data
93	PCI_AD27	I/O	PCI	-	PCI Address/Data
94	PCI_AD26	I/O	PCI	-	PCI Address/Data
95	PCI_AD25	I/O	PCI	-	PCI Address/Data
96	PCI_AD24	I/O	PCI	-	PCI Address/Data
97	PCI_CBE3	I/O	PCI	-	PCI Command/Byte Enable
98	VDDI	PWR	-	-	1.8 Volt Core Power
99	VSS	GND	-	-	Ground
100	PCI_IDSEL	I	-	-	PCI ID Select
101	PCI_AD23	I/O	PCI	-	PCI Address/Data
102	PCI_AD22	I/O	PCI	-	PCI Address/Data
103	PCI_AD21	I/O	PCI	-	PCI Address/Data
104	PCI_AD20	I/O	PCI	-	PCI Address/Data
105	PCI_AD19	I/O	PCI	-	PCI Address/Data
106	PCI_AD18	I/O	PCI	-	PCI Address/Data
107	PCI_AD17	I/O	PCI	-	PCI Address/Data
108	VDDO	PWR	-	-	3.3 Volt Power
109	VSS	GND	-	-	Ground
110	PCI_AD16	I/O	PCI	-	PCI Address/Data

Pin #	Pin Name	Type	Drive	Internal Resistor	Description
111	PCI_CBE2	I/O	PCI	-	PCI Command/Byte Enable
112	PCI_FRAME_N	I/O	PCI	-	PCI Frame
113	PCI_IRDY_N	I/O	PCI	-	PCI Initiator Ready
114	PCI_PERR_N	I/O	PCI	-	PCI Parity Error
115	PCI_STOP_N	I/O	PCI	-	PCI Stop
116	PCI_DEVSEL_N	I/O	PCI	-	PCI Device Select
117	PCI_TRDY_N	I/O	PCI	-	PCI Target Ready
118	VDDI	PWR	-	-	1.8 Volt Core Power
119	VSS	GND	-	-	Ground
120	PCI_SERR_N	OD	PCI	-	PCI System Error
121	PCI_PAR	I/O	PCI	-	PCI Parity
122	PCI_CBE1	I/O	PCI	-	PCI Command/Byte Enable
123	PCI_AD15	I/O	PCI	-	PCI Address/Data
124	PCI_AD14	I/O	PCI	-	PCI Address/Data
125	PCI_AD13	I/O	PCI	-	PCI Address/Data
126	PCI_AD12	I/O	PCI	-	PCI Address/Data
127	PCI_AD11	I/O	PCI	-	PCI Address/Data
128	VDDO	PWR	-	-	3.3 Volt Power
129	VSS	GND	-	-	Ground
130	PCI_AD10	I/O	PCI	-	PCI Address/Data
131	PCI_M66EN	I	-	-	PCI 66 MHz Enable
132	PCI_AD09	I/O	PCI	-	PCI Address/Data
133	PCI_AD08	I/O	PCI	-	PCI Address/Data
134	PCI_CBE0	I/O	PCI	-	PCI Command/Byte Enable
135	PCI_AD07	I/O	PCI	-	PCI Address/Data
136	PCI_AD06	I/O	PCI	-	PCI Address/Data
137	PCI_AD05	I/O	PCI	-	PCI Address/Data
138	PCI_AD04	I/O	PCI	-	PCI Address/Data
139	PCI_AD03	I/O	PCI	-	PCI Address/Data
140	PCI_AD02	I/O	PCI	-	PCI Address/Data
141	PCI_AD01	I/O	PCI	-	PCI Address/Data
142	PCI_AD00	I/O	PCI	-	PCI Address/Data
143	MEM_CS_N	O		-	Memory Chip Select
144	VDDO	PWR	-	-	3.3 Volt Power

Table 3-1 Sil3112A Pin Listing

Pin Type	Pin Description
I	Input Pin with LVTTL Thresholds
I-Schmitt	Input Pin with Schmitt Trigger
O	Output Pin
T	Tri-state Output Pin
I/O	Bi-directional Pin
OD	Open Drain Output Pin

Table 3-2 Pin Types

PCI pins are 5V tolerant.

3.2 Sil3112A Pin Diagram

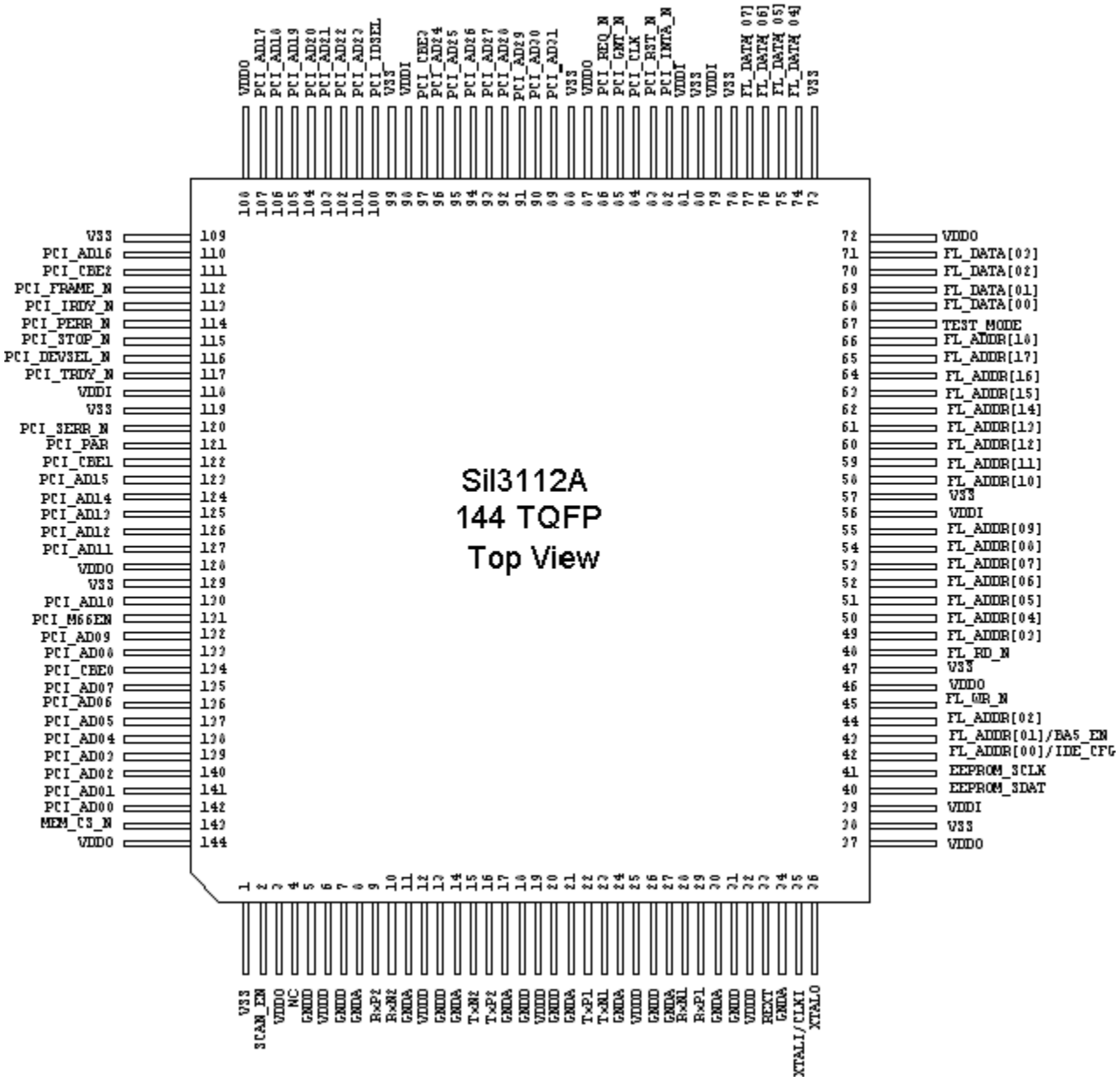

Figure 3-1. Sil3112A Pin Diagram

3.3 Sil3112A Pin Descriptions

3.3.1 PCI 66MHz 32-bit

PCI Address and Data

Pin Names: PCI_AD[31..0]
Pin Numbers: 89~96, 101~107, 110, 123~127,132, 133, 135~142
Address and Data buses are multiplexed on the same PCI pins. A bus transaction consists of an address phase followed by one or more data phases. PCI supports both read and write bursts. The address phase is the first clock cycle in which PCI_FRAME_N signal is asserted. During the address phase, PCI_AD[31:0] contain a physical address (32 bits). For I/O, this can be a byte address. For configuration and memory it is a DWORD address. During data phases, PCI_AD[7:0] contain the least significant byte (LSB) and PCI_AD[31:24] contain the most significant byte (MSB). Write data is stable and valid when PCI_IRDY_N is asserted; read data is stable and valid when PCI_TRDY_N is asserted. Data is transferred during those clocks where both PCI_IRDY_N and PCI_TRDY_N are asserted.

PCI Command and Byte Enables

Pin Names: PCI_CBE[3..0]
Pin Numbers: 97, 111, 122, 134
Command and Byte Enables are multiplexed on the same PCI pins. During the address phase of a transaction, PCI_CBE[3:0]_N define the bus command. During the data phase, PCI_CBE[3:0]_N are used as Byte Enables. Byte Enables are valid for the entire data phase and determine which byte lanes carry meaningful data.

PCI ID Select

Pin Name: PCI_IDSEL
Pin Number: 100
This signal is used as a chip select during configuration read and write transactions.

PCI Frame Cycle

Pin Name: PCI_FRAME_N
Pin Number: 112
Cycle Frame is driven by the current master to indicate the beginning and duration of an access. PCI_FRAME_N is asserted to indicate that a bus transaction is beginning. While PCI_FRAME_N is asserted, data transfers continue. When PCI_FRAME_N is de-asserted, the transaction is in the final data phase or has completed.

PCI Initiator Ready

Pin Name: PCI_IRDY_N
Pin Number: 113
Initiator Ready indicates the initializing agent's (bus master's) ability to complete the current data phase of the transaction. This signal is used with PCI_TRDY_N. A data phase is completed on any clock when both PCI_IRDY_N and PCI_TRDY_N are sampled as asserted. Wait cycles are inserted until both PCI_IRDY_N and PCI_TRDY_N are asserted together.

PCI Target Ready

Pin Name: PCI_TRDY_N
Pin Number: 117
Target Ready indicates the target agent's ability to complete the current data phase of the transaction. PCI_TRDY_N is used with PCI_IRDY_N. A data phase is completed on any clock when both PCI_TRDY_N and PCI_IRDY_N are sampled asserted. During a read, PCI_TRDY_N indicates that valid data is present on PCI_AD[31:0]. During a write, it indicates the target is prepared to accept data.

PCI Device Select

Pin Name: PCI_DEVSEL_N

Pin Number: 116
Device Select, when actively driven, indicates the driving device has decoded its address as the target of the current access. As an input, PCI_DEVSEL_N indicates to a master whether any device on the bus has been selected.

PCI Stop

Pin Name: PCI_STOP_N
Pin Number: 115
PCI_STOP_N indicates the current target is requesting that the master stop the current transaction.

PCI Parity Error

Pin Name: PCI_PERR_N
Pin Number: 114
PCI_PERR_N indicates a data parity error between the current master and target on PCI. On a write transaction, the target always signals data parity errors back to the master on PCI_PERR_N. On a read transaction, the master asserts PCI_PERR_N to indicate to the system that an error was detected.

PCI System Error

Pin Name: PCI_SERR_N
Pin Number: 120
System Error is for reporting address parity errors, data parity errors on Special Cycle Command, or any other system error where the result will be catastrophic. The PCI_SERR_N is a pure open drain and is actively driven for a single PCI clock by the agent reporting the error. The assertion of PCI_SERR_N is synchronous to the clock and meets the setup and hold times of all bused signals. However, the restoring of PCI_SERR_N to the de-asserted state is accomplished by a weak pull-up. Note that if an agent does not want a non-maskable interrupt (NMI) to be generated, a different reporting mechanism is required.

PCI Parity

Pin Name: PCI_PAR
Pin Number: 121
PCI_PAR is even parity across PCI_AD[31:0] and PCI_CBE[3:0]_N. Parity generation is required by all PCI agents. PCI_PAR is stable and valid one clock after the address phase. For data phases PCI_PAR is stable and valid one clock after either PCI_IRDY_N is asserted on a write transaction or PCI_TRDY_N is asserted on a read transaction. Once PCI_PAR is valid, it remains valid until one clock after the completion of the current data phase. (PCI_PAR has the same timing as PCI_AD[31:0] but delayed by one clock.)

PCI Request

Pin Name: PCI_REQ_N
Pin Number: 86
This signal indicates to the arbiter that this agent desires use of the PCI bus.

PCI Grant

Pin Name: PCI_GNT_N
Pin Number: 85
This signal indicates to the agent that access to the PCI bus has been granted. In response to a PCI request, this is a point-to-point signal. Every master has its own PCI_GNT_N, which must be ignored while PCI_RST_N is asserted.

PCI Interrupt A

Pin Name: PCI_INTA_N
Pin Number: 82
Interrupt A is used to request an interrupt on the PCI bus. PCI_INTA_N is open collector and is an open drain output.

PCI Clock Signal

Pin Names: PCI_CLK
Pin Number: 84
Clock Signal provides timing for all transactions on PCI and is an input to every PCI device. All other PCI signals (except PCI_RST_N, and PCI_INTA_N) are sampled on the rising edge of PCI_CLK. All other timing parameters are defined with respect to this edge.

PCI Reset

Pin Name: PCI_RST_N
Pin Number: 83
PCI_RST_N is an active low input that is used to set the internal registers to their initial state. PCI_RST_N is typically the system power-on reset signal as distributed on the PCI bus.

PCI M66EN

Pin Name: PCI_M66EN
Pin Number: 131
This pin configures the PCI bus operating frequency. When low, the PCI bus operates from 0 to 33 MHz. When high, the PCI bus operates from 33MHz to 66MHz.

3.3.2 Miscellaneous I/O

Ground

Pin Name: VSS
Pin Number: 1, 38, 47, 57, 73, 78, 80, 88, 99, 109,119, 129
Ground reference point to power supply.

TEST

Pin Name: TEST_MODE
Pin Number: 67
This pin is used, in conjunction with other pins, to enable various test functions within the device.

Power Supply

Pin Name(s): VDDO
Pin Number(s): 3, 37, 46, 72, 87, 108, 128, 144
Power Supply Input (3.3 +/- 0.3 Volt)

Pin Name(s): VDDI
Pin Number(s): 39, 56, 79, 81, 98, 118
Power Supply Input for internal core (1.8 +/- 0.09 Volt)

Internal Scan Test

Pin Name: SCAN_EN
Pin Number: 2
This pin, when active (high), will place all scan flip-flops into scan mode for chip testing. This pin must be left open or tied to ground for normal operation.

Flash Signals

Pin Name: FL_ADDR[00] / IDE_CFG
Pin Number: 42
When PCI_RST_N is deasserted, this pin is an output and represents flash memory address bit 0 During reset, it is sampled to configure Mass Storage class or RAID mode in the PCI Class Code register. A high on this pin sets Mass Storage class, a low sets RAID mode. The configuration state is latched internally when PCI_RST_N is deasserted. This pad is internally pulled high to enable Mass Storage class if left unconnected.

Pin Name: FL_ADDR[01] / BA5_EN
Pin Number: 43
When PCI_RST_N is deasserted, this pin is an output and represents flash memory address bit 1 During reset, it is sampled to configure Base address register 5. A high on this pin enables base address register 5, a low disables base address register 5. The configuration state is latched internally when PCI_RST_N is deasserted. This pin is internally pulled high to enable Base address register 5 when left unconnected.

Pin Name: FL_ADDR[02-18]
Pin Numbers: 44, 49~55, 58~66
Flash Memory address bits; 19 total for 512K address space. Flash address pins 15 to 18 are used to select internal test modes in conjunction with the TEST_MODE pin; they have internal pull-downs and must be unconnected or pulled down.

Pin Name: FL_DATA[00-07]
Pin Numbers: 68~71, 74~77
8-bit Flash memory data bus.

Pin Name: FL_RD_N
Pin Number: 48
Flash read enable signal, active low

Pin Name: FL_WR_N
Pin Number: 45
Flash write enable signal, active low

Memory Chip Select

Pin Name: MEM_CS_N
Pin Number: 143
This pin is used to select and enable the external memory. It is active low.

Serial Interface Signals

Pin Name: EEPROM_SDAT
Pin Number: 40
Serial Interface data line

Pin Name: EEPROM_SCLK
Pin Number: 41
Serial Interface clock

3.3.3 Serial ATA Signals

Power Supply & Ground

Pin Name: VDDD
Pin Numbers: 6, 12, 19, 25, and 32
SerDes 1.8 V Power supply Pins

Pin Name: GNDD
Pin Numbers: 5, 7, 13, 18, 20, 26, and 31
SerDes Digital Ground

Pin Name: GNDA
Pin Numbers: 8, 11, 14, 17, 21, 24, 27, 30, and 34
SerDes Analog Ground

High Speed Serial Signals

Pin Name: RxN1
Pin Number: 28
Channel 1 high-speed differential receive negative side.

Pin Name: RxP1
Pin Number: 29
Channel 1 high-speed differential receive positive side. Loading an internal register through the flash or EEPROM during the initialization sequence could reverse RxP1 and RxN1 pinouts.

Pin Name: TxN1
Pin Number: 23
Channel 1 high speed differential transmit negative side

Pin Name: TxP1
Pin Number: 22
Channel 1 high speed differential transmit positive side

Pin Name: RxN2
Pin Number: 10
Channel 2 high-speed differential receive negative side.

Pin Name: RxP2
Pin Number: 9
Channel 2 high-speed differential receive positive side. Loading an internal register through the flash or EEPROM during the initialization sequence could reverse RxP2 and RxN2 pinouts.

Pin Name: TxN2
Pin Number: 15
Channel 2 high speed differential transmit negative side

Pin Name: TxP2
Pin Number: 16
Channel 2 high speed differential transmit positive side

Other SerDes Signals

Pin Name: XTALO
Pin Number: 36
Crystal oscillator pin for SerDes reference clock. A 25MHz crystal must be used.

Pin Name: XTALI/CLKI
Pin Number: 35
Crystal oscillator pin for SerDes reference clock. When external clock source is selected, the external clock (either 25MHz or 100 MHz) will come in through this pin. The clock precision requirement is ±100ppm.

Pin Name: REXT
Pin Number: 33
External reference resistor pin for termination calibration. This pin provides the addition function of selecting frequency of the clock source . For 25MHz crystal/external clock, a 1K, 1% resistor is connected to ground. To use 100MHz external clock, a 4.99K, 1% resistor is connected to ground.

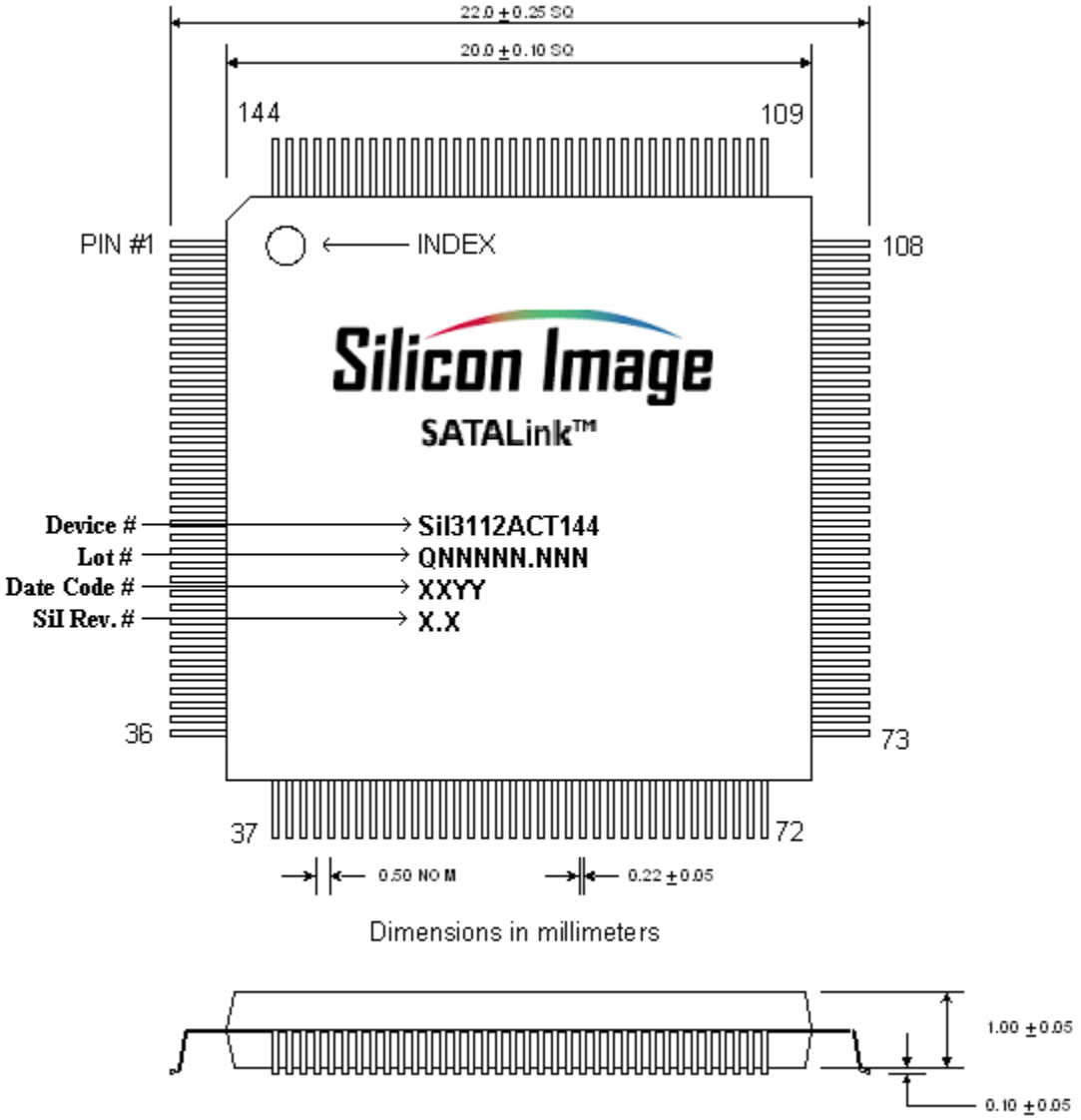

Figure 3-2: Package Drawing – 144 TQFP

4 Block Diagram

The SiI3112A contains the major logic modules shown below.

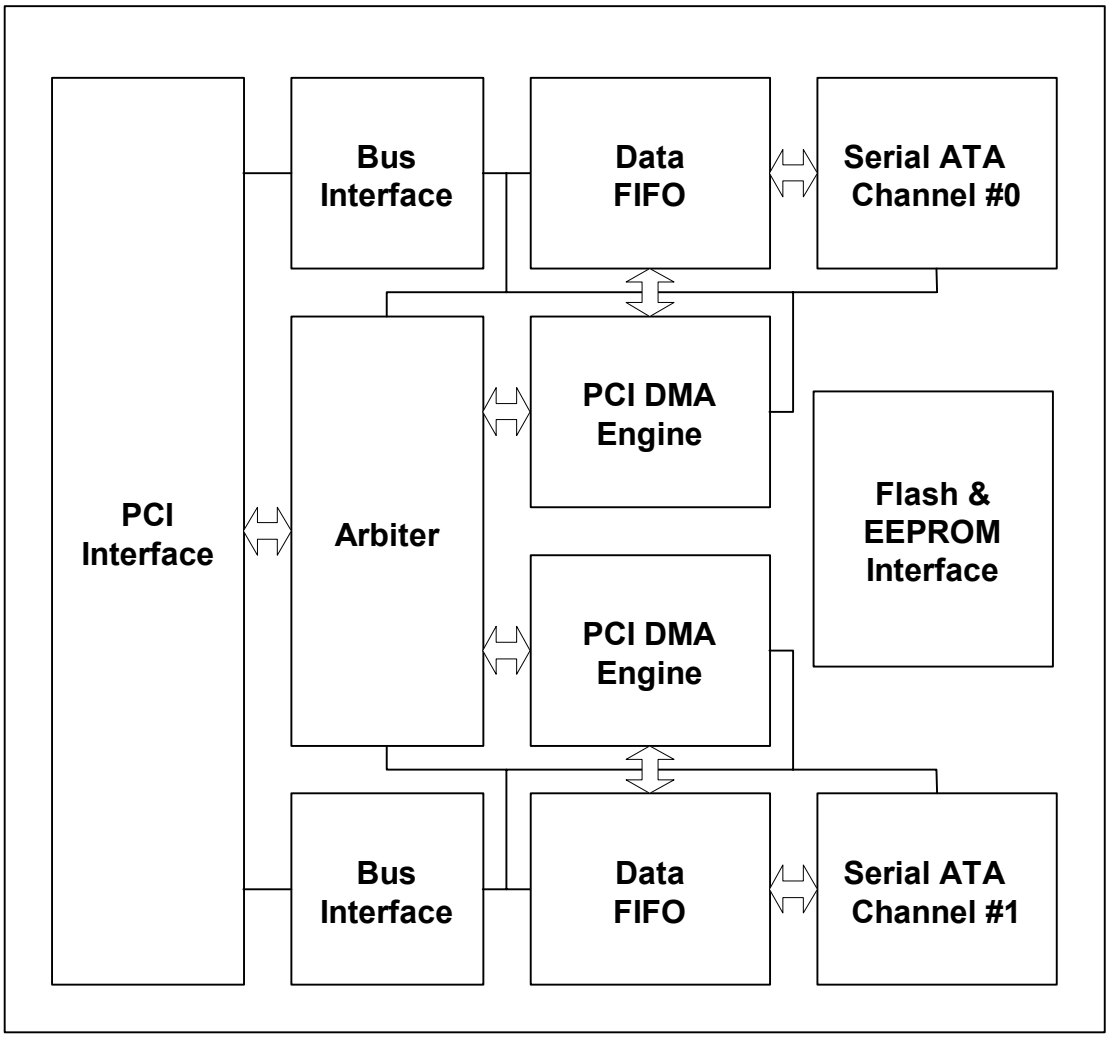

Figure 4-1: SiI3112A Block Diagram

5 Auto-Initialization

The SiI3112A supports an external FLASH and/or EEPROM device for BIOS extensions and user-defined PCI configuration header data.

5.1 Auto-Initialization from FLASH

The SiI3112A initiates the FLASH detection and configuration space loading sequence upon the release of PCI_RST_N. It begins by reading the highest two addresses ($7FFFF_H$ and $7FFFE_H$), checking for the correct data signature pattern – AA_H and 55_H, respectively. If the data signature pattern is correct, the SiI3112A continues to sequence the address downward, reading a total of sixteen bytes. If the Data Signature is correct (55_H at $7FFFC_H$), the last twelve bytes are loaded into the PCI Configuration Space registers.

Note: If both Flash and EEPROM are installed, the PCI Configuration Space registers will be loaded with EEPROM's data. While the sequence is active, the SiI3112A responds to all PCI bus accesses with a Target Retry.

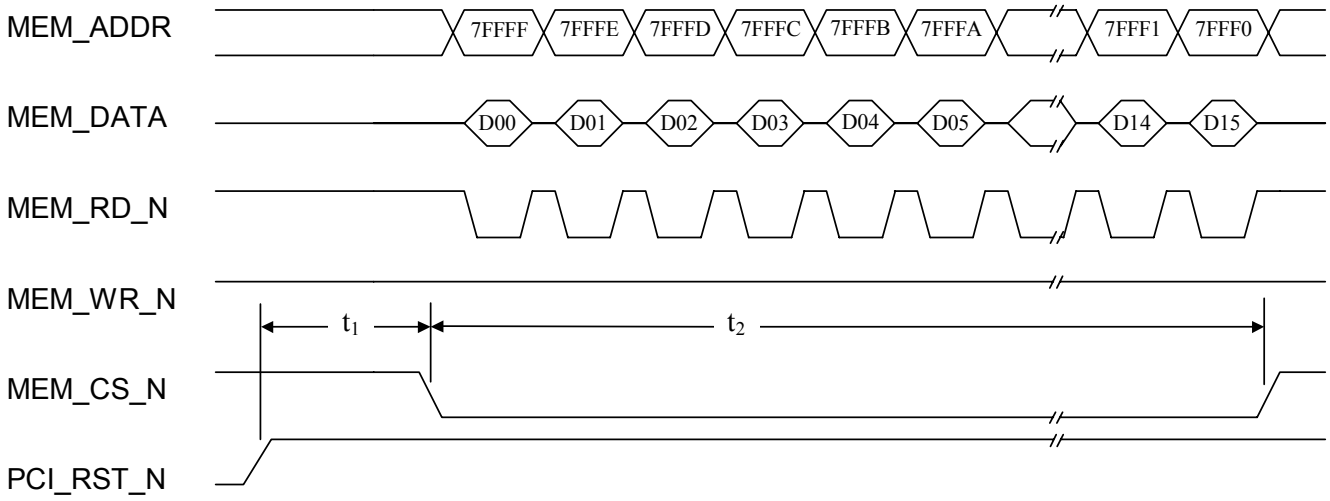

Figure 5-1 Auto-Initialization from Flash Timing

Parameter	Value	Description
t_1	660 ns	PCI reset to Flash Auto-Initialization cycle begin
t_2	9600 ns	Flash Auto-Initialization cycle time

Table 5-1 Auto-Initialization from Flash Timing

Address	Data Byte	Description
$7FFFF_H$	D00	Data Signature = AA_H
$7FFFE_H$	D01	Data Signature = 55_H
$7FFFD_H$	D02	AA = 120 ns FLASH device / Else, 240 ns FLASH device
$7FFFC_H$	D03	Data Signature = 55_H
$7FFFB_H$	D04	PCI Device ID [23:16]
$7FFFA_H$	D05	PCI Device ID [31:24]
$7FFF9_H$	D06	PCI Class Code [15:08]
$7FFF8_H$	D07	PCI Class Code [23:16]
$7FFF7_H$	D08	PCI Sub-System Vendor ID [07:00]
$7FFF6_H$	D09	PCI Sub-System Vendor ID [15:08]
$7FFF5_H$	D10	PCI Sub-System ID [23:16]
$7FFF4_H$	D11	PCI Sub-System ID [31:24]
$7FFF3_H$	D12	SerialATA PHY Config [07:00] (default: 0xF1)
$7FFF2_H$	D13	SerialATA PHY Config [15:08] (default: 0x80)
$7FFF1_H$	D14	SerialATA PHY Config [23:16] (default: 0x00)
$7FFF0_H$	D15	SerialATA PHY Config [31:24] (default: 0x00)

Table 5-2 Flash Data Description

5.2 Auto-Initialization from EEPROM

The SiI3112A initiates the EEPROM detection and configuration space loading sequence after the FLASH read sequence. The SiI3112A supports up to 256 byte EEPROM with a 2-wire serial interface. The sequence of operations consists of the following.

1) START condition defined as a high-to-low transition on SDAT while SCLK is high.
2) Control byte = 1010 (Control Code) + 000 (Chip Select) + 0 (Write Address)
3) Acknowledge
4) Starting address field = 00000000.
5) Acknowledge
6) Sequential data bytes separated by Acknowledges.
7) STOP condition.

While the sequence is active, the SiI3112A responds to all PCI bus accesses with a Target Retry.

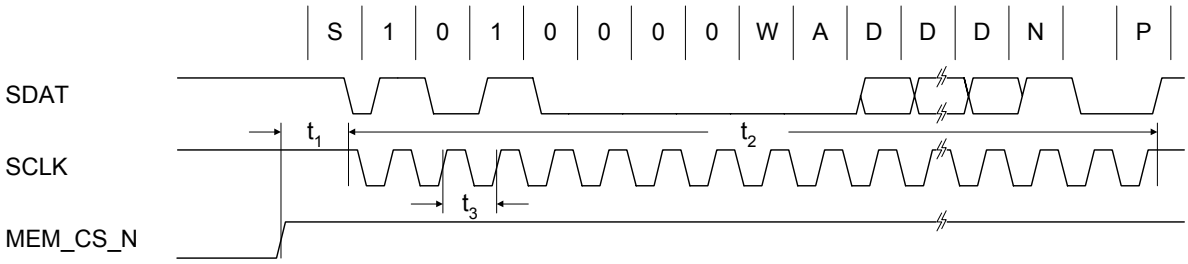

Figure 5-2: Auto-Initialization from EEPROM Timing

Parameter	Value	Description
t_1	26.00 µs	End of Auto-Initialization from FLASH to start of Auto-Initialization from EEPROM
t_2	2.66 ms	Auto-Initialization from EEPROM cycle time
t_3	19.26 µs	EEPROM serial clock period

Table 5-3 Auto-Initialization from EEPROM Timing

Parameter	Description
S	START condition
W	R/W 0 = Write Command, 1 = Read Command
A	Acknowledge
D	Serial data
N	No-Acknowledge
P	STOP condition

Table 5-4 Auto-Initialization from EEPROM Timing Symbols

Address	Data Byte	Description
00_H	D00	Memory Present Pattern = AA_H
01_H	D01	Memory Present Pattern = 55_H
02_H	D02	Data Signature = AA_H
03_H	D03	Data Signature = 55_H
04_H	D04	PCI Device ID [23:16]
05_H	D05	PCI Device ID [31:24]
06_H	D06	PCI Class Code [15:08]
07_H	D07	PCI Class Code [23:16]
08_H	D08	PCI Sub-System Vendor ID [07:00]
09_H	D09	PCI Sub-System Vendor ID [15:08]
$0A_H$	D10	PCI Sub-System ID [23:16]
$0B_H$	D11	PCI Sub-System ID [31:24]
$0C_H$	D12	SerialATA PHY Config [07:00] (default: 0xF1)
$0D_H$	D13	SerialATA PHY Config [15:08] (default: 0x80)
$0E_H$	D14	SerialATA PHY Config [23:16] (default: 0x00)
$0F_H$	D15	SerialATA PHY Config [31:24] (default: 0x00)

Table 5-5 EEPROM Data Description

6 ATA Command Supported

6.1 Data Modes

The SiI3112A PCI to Serial ATA Controller has an internal datapath interface between the PCI block and the Serial ATA controller block. The data modes (Register mode, PIO mode and DMA mode) are of no significance inside the SiI3112A.

6.2 ATA Commands

The SiI3112A PCI to Serial ATA Controller decodes ATA commands in hardware. The commands supported include ATA/ATAPI-5 and ATA/ATAPI-6 commands, including the 48-bit LBA extended commands. Certain obsolesced commands are also supported. The supported commands are listed below:

Table 10-1 Supported ATA Commands

Command	Command/ Features Codes	Comment
CFA Erase Sectors	C0h	
CFA Request Extended Error Code	03h	
CFA Translate Sector	87h	
CFA Write Multiple without Erase	CDh	
CFA Write Sectors without Erase	38h	
Check Media Card Type	D1h	
Check Power Mode	E5h	
Configure Stream	51h	
Device Configuration Freeze Lock	B1h/C1h	
Device Configuration Identify	B1h/C2h	
Device Configuration Restore	B1h/C0h	
Device Configuration Set	B1h/C3h	
Device Reset	08h	
Download Microcode	92h	
Execute Device Diagnostics	90h	The two Serial ATA ports for SiI3112A PCI to Serial ATA Controller are both "single masters".
Flush Cache	E7h	
Flush Cache Ext	EAh	48-bit LBA Command
Format Track	50h	Obsolesced vendor specific command, needs to be programmed as vendor specific commands
Get Media Status	DAh	
Identify Device	ECh	

Command	Command/ Features Codes	Comment
Identify Packet Device	A1h	
Idle	E3h	
Idle Immediate	E1h	
Initialize Device Parameters	91h	Obsolesced in ATA/ATAPI-6.
Media Eject	EDh	
Media Lock	DEh	
Media Unlock	DFh	
Nop	00h	
Packet	A0h	
Read Buffer	E4h	
Read DMA	C8h	
	C9h	Obsolesced Command code supported, decoded as Command Code C8h
Read DMA Ext	25h	48-bit LBA Command
Read DMA Queued	C7h	
Read DMA Queued Ext	26h	48-bit LBA Command
Read Log Ext	2Fh	
Read Long	22h	Obsolesced command
	23h	
Read Multiple	C4h	
Read Multiple Ext	29h	48-bit LBA Command
Read Native Max Address	F8h	
Read Native Max Address Ext	27h	48-bit LBA Command
Read Sector(s)	20h	
	21h	Obsolesced Command code supported, decoded as Command Code 20h
Read Sector(s) Ext	24h	48-bit LBA Command
Read Stream DMA	2A	
Read Stream PIO	2B	
Read Verify Sector(s)	40h	
	41h	Obsolesced Command code supported, decoded as Command Code 40h
Read Verify Sector(s) Ext	42h	48-bit LBA Command
Recalibrate	10h	Obsolesced command supported.
Security Disable Password	F6h	
Security Erase Prepare	F3h	
Security Erase Unit	F4h	
Security Freeze Lock	F5h	

Command	Command/ Features Codes	Comment
Security Set Password	F1h	
Security Unlock	F2h	
Seek	70h	
Service	A2h	
Set Features	EFh	
Set Max Address	F9h/00h	
Set Max Address Ext	37h	48-bit LBA Command
Set Max Freeze Lock	F9h/04h	
Set Max Lock	F9h/02h	
Set Max Unlock	F9h/03h	Obsolesced command supported.
Set Max Set Password	F9h/01h	
Set Multiple Mode	C6h	The SiI3112A PCI to Serial ATA Controller intercepts the command to set up the number of sectors for a DRQ block upon this command.
Sleep	E6h	
Smart Disable Operations	B0h/D9h	
Smart Enable Operations	B0h/D8h	
Smart Enable/Disable Attributes Autosave	B0h/D2h	
Smart Execute Off-Line Immediate	B0h/D4h	
Smart Read Attribute Thresholds	B0h/D1h	Obsolesced command supported.
Smart Read Data	B0h/D0h	
Smart Read Log	B0h/D5h	
Smart Return Status	B0h/DAh	
Smart Save Attribute Values	B0h/D3h	Obsolesced command supported.
Smart Write Log	B0h/D6h	
Standby	E2h	
Standby Immediate	E0h	
Write Buffer	E8h	
Write DMA	CAh	
	CBh	Obsolesced Command code supported, decoded as Command Code CAh
Write DMA Ext	35h	48-bit LBA Command
Write DMA Queued	CCh	
Write DMA Queued Ext	36h	48-bit LBA Command
Write Log Ext	3Fh	
Write Long	32h	Obsolesced command supported
	33h	
Write Multiple	C5h	

Command	Command/ Features Codes	Comment
Write Multiple Ext	39h	48-bit LBA Command
Write Sector(s)	30h	
	31h	Obsolesced Command code supported, decoded as Command Code 30h
Write Sector(s) Ext	34h	48-bit LBA Command
Write Stream DMA	3Ah	
Write Stream PIO	3Bh	

7 Power Sequencing 1.8V and 3.3V Supplies

The SiI3112A operates with 1.8V for the digital logic (VDDI) and the analog circuitry (VDDD), and 3.3V (VDDO) supplies for the I/O's. The voltage difference between the 1.8V supply and the 3.3V supplies must never be greater than 2.0V. It is possible for the 1.8V supply to rise faster than the 3.3V supply on power up without violating this rule, as long as the difference never exceeds 2.0V.