FDS9926A

Dual N-Channel 2.5V Specified PowerTrench® MOSFET

General Description

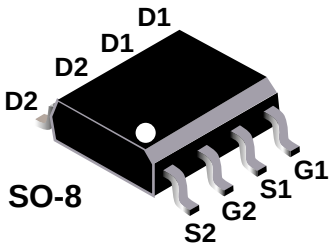
These N-Channel 2.5V specified MOSFETs use Fairchild Semiconductor's advanced PowerTrench process. It has been optimized for power management applications with a wide range of gate drive voltage (2.5V – 10V).

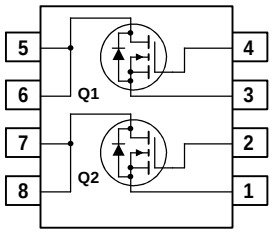
Applications

- Battery protection
- Load switch
- Power management

Features

- 6.5 A, 20 V. $R_{DS(ON)}$ = 0.030 Ω @ V_{GS} = 4.5 V
  $R_{DS(ON)}$ = 0.043 Ω @ V_{GS} = 2.5 V.
- Optimized for use in battery protection circuits
- ±10 V_{GSS} allows for wide operating voltage range
- Low gate charge





Absolute Maximum Ratings

T_A=25°C unless otherwise noted

Symbol	Parameter		Ratings	Units
V_{DSS}	Drain-Source Voltage		20	V
V_{GSS}	Gate-Source Voltage		±10	V
I_D	Drain Current – Continuous	(Note 1a)	6.5	A
	– Pulsed		20	
P_D	Power Dissipation for Dual Operation		2	W
	Power Dissipation for Single Operation	(Note 1a)	1.6	
		(Note 1b)	1	
		(Note 1c)	0.9	
T_J, T_{STG}	Operating and Storage Junction Temperature Range		-55 to +150	°C

Thermal Characteristics

$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient	(Note 1a)	78	°C/W
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case	(Note 1)	40	°C/W

Package Marking and Ordering Information

Device Marking	Device	Reel Size	Tape width	Quantity
FDS9926A	FDS9926A	13''	12mm	2500 units

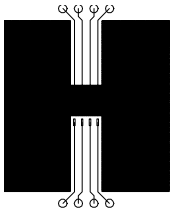
Electrical Characteristics

T_A = 25°C unless otherwise noted

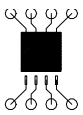
Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
Off Characteristics						
BV_{DSS}	Drain–Source Breakdown Voltage	V_{GS} = 0 V, I_D = 250 µA	20			V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	I_D = 250 µA, Referenced to 25°C		14		mV/°C
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = 16 V, V_{GS} = 0 V			1	µA
I_{GSSF}	Gate–Body Leakage, Forward	V_{GS} = 8 V, V_{DS} = 0 V			100	nA
I_{GSSR}	Gate–Body Leakage, Reverse	V_{GS} = –8 V V_{DS} = 0 V			–100	nA
On Characteristics (Note 2)						
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS} = V_{GS}, I_D = 250 µA	0.5	1	1.5	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate Threshold Voltage Temperature Coefficient	I_D = 250 µA, Referenced to 25°C		-3		mV/°C
$R_{DS(on)}$	Static Drain–Source On–Resistance	V_{GS} = 4.5 V, I_D = 6.5 A V_{GS} = 2.5 V, I_D = 5.4 A V_{GS}= 4.5 V, I_D =6.5A, T_J=125°C		0.025 0.036 0.035	0.030 0.043 0.050	Ω
$I_{D(on)}$	On–State Drain Current	V_{GS} = 4.5 V, V_{DS} = 5 V	15			A
g_{FS}	Forward Transconductance	V_{DS} = 5 V, I_D = 3 A		11		S
Dynamic Characteristics						
C_{iss}	Input Capacitance	V_{DS} = 10 V, V_{GS} = 0 V, f = 1.0 MHz		700		pF
C_{oss}	Output Capacitance			175		pF
C_{rss}	Reverse Transfer Capacitance			85		pF
Switching Characteristics (Note 2)						
$t_{d(on)}$	Turn–On Delay Time	V_{DD} = 10 V, I_D = 1 A, V_{GS} = 4.5 V, R_{GEN} = 6 Ω		8	16	ns
t_r	Turn–On Rise Time			10	18	ns
$t_{d(off)}$	Turn–Off Delay Time			18	29	ns
t_f	Turn–Off Fall Time			5	10	ns
Q_g	Total Gate Charge	V_{DS} = 10 V, I_D = 3A, V_{GS} = 4.5 V		7	10	nC
Q_{gs}	Gate–Source Charge			1.2		nC
Q_{gd}	Gate–Drain Charge			1.9		nC
Drain–Source Diode Characteristics and Maximum Ratings						
I_S	Maximum Continuous Drain–Source Diode Forward Current				1.3	A
V_{SD}	Drain–Source Diode Forward Voltage	V_{GS} = 0 V, I_S = 1.3 A (Note 2)		0.65	1.2	V

Notes:

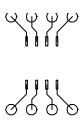
1. $R_{\theta JA}$ is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. $R_{\theta JC}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design.



a) 78°/W when mounted on a 0.5in^2 pad of 2 oz copper



b) 125°/W when mounted on a 0.02 in^2 pad of 2 oz copper



c) 135°/W when mounted on a minimum pad.

Scale 1 : 1 on letter size paper

2. Pulse Test: Pulse Width < 300µs, Duty Cycle < 2.0%