L7C185

8K x 8 Static RAM (Low Power)

FEATURES

- 8K x 8 Static RAM with Chip Select Powerdown, Output Enable
- Auto-Powerdown™ Design
- Advanced CMOS Technology
- High Speed — to 12 ns maximum
- Low Power Operation
  Active:
  425 mW typical at 25 ns
  Standby (typical):
  400µW (L7C185)
  200 µW (L7C185-L)
- Data Retention at 2 V for Battery Backup Operation
- DESC SMD No. 5962-38294
- Available 100% Screened to MIL-STD-883, Class B
- Plug Compatible with IDT7164, Cypress CY7C185/186
- Package Styles Available:
  - 28-pin Plastic DIP
  - 28-pin Ceramic DIP
  - 28-pin Plastic SOJ
  - 28-pin Ceramic Flatpack
  - 28-pin Ceramic LCC
  - 32-pin Ceramic LCC

DESCRIPTION

The **L7C185** is a high-performance, low-power CMOS static RAM. The storage circuitry is organized as 8,192 words by 8 bits per word. The 8 Data In and Data Out signals share I/O pins. These devices are available in four speeds with maximum access times from 12 ns to 25 ns.

Inputs and outputs are TTL compatible. Operation is from a single +5 V power supply. Power consumption for the L7C185 is 425 mW (typical) at 25 ns. Dissipation drops to 60 mW (typical) for the L7C185 and 50 mW (typical) for the L7C185-L when the memory is deselected.

Two standby modes are available. Proprietary Auto-Powerdown™ circuitry reduces power consumption automatically during read or write accesses which are longer than the minimum access time, or when the memory is deselected. In addition, data may be retained in inactive storage with a supply voltage as low as 2 V. The L7C185 and L7CL185-L consume only 30 µW and 15 µW (typical) respectively at 3 V, allowing effective battery backup operation.

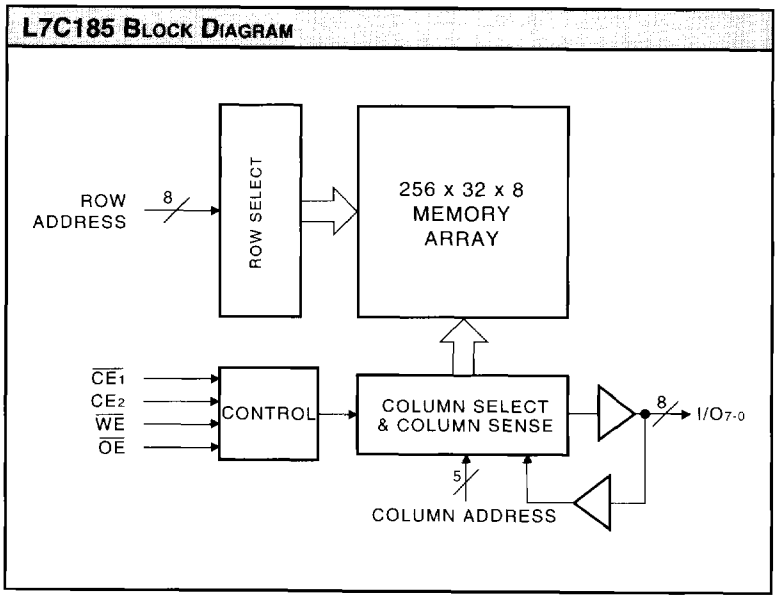
The L7C185 provides asynchronous (unclocked) operation with matching access and cycle times. Two Chip Enables (one active-low) and a three-state I/O bus with a separate Output Enable control simplify the connection of several chips for increased storage capacity.

Memory locations are specified on address pins A_0 through A_{12}. Reading from a designated location is accomplished by presenting an address and driving $\overline{CE_1}$ and $\overline{OE}$ LOW, and CE_2 and $\overline{WE}$ HIGH. The data in the addressed memory location will then appear on the Data Out pins within one access time. The output pins stay in a high-impedance state when $\overline{CE_1}$ or $\overline{OE}$ is HIGH, or CE_2 or $\overline{WE}$ is LOW.

Writing to an addressed location is accomplished when the active-low $\overline{CE_1}$ and $\overline{WE}$ inputs are both LOW, and CE_2 is HIGH. Any of these signals may be used to terminate the write operation. Data In and Data Out signals have the same polarity.

Latchup and static discharge protection are provided on-chip. The L7C185 can withstand an injection current of up to 200 mA on any pin without damage.

L7C185 Block Diagram



Maximum Ratings *Above which useful life may be impaired (Notes 1, 2)*

Storage temperature	–65°C to +150°C
Operating ambient temperature	–55°C to +125°C
V_{CC} supply voltage with respect to ground	–0.5 V to +7.0 V
Input signal with respect to ground	–3.0 V to +7.0 V
Signal applied to high impedance output	–3.0 V to +7.0 V
Output current into low outputs	25 mA
Latchup current	> 200 mA

Operating Conditions *To meet specified electrical and switching characteristics*

Mode	Temperature Range (Ambient)	Supply Voltage
Active Operation, Commercial	0°C to +70°C	4.5 V ≤ V_{CC} ≤ 5.5 V
Active Operation, Industrial	–40°C to +85°C	4.5 V ≤ V_{CC} ≤ 5.5 V
Active Operation, Military	–55°C to +125°C	4.5 V ≤ V_{CC} ≤ 5.5 V
Data Retention, Commercial	0°C to +70°C	2.0 V ≤ V_{CC} ≤ 5.5 V
Data Retention, Industrial	–40°C to +85°C	2.0 V ≤ V_{CC} ≤ 5.5 V
Data Retention, Military	–55°C to +125°C	2.0 V ≤ V_{CC} ≤ 5.5 V

Electrical Characteristics *Over Operating Conditions (Note 5)*

			L7C185			L7C185-L			
Symbol	Parameter	Test Condition	Min	Typ	Max	Min	Typ	Max	Unit
V_{OH}	Output High Voltage	V_{CC} = 4.5 V, I_{OH} = –4.0 mA	2.4			2.4			V
V_{OL}	Output Low Voltage	I_{OL} = 8.0 mA			0.4			0.4	V
V_{IH}	Input High Voltage		2.2		V_{CC} +0.3	2.2		V_{CC} +0.3	V
V_{IL}	Input Low Voltage	(Note 3)	–3.0		0.8	–3.0		0.8	V
I_{IX}	Input Leakage Current	Ground ≤ V_{IN} ≤ V_{CC}	–10		+10	–10		+10	µA
I_{OZ}	Output Leakage Current	(Note 4)	–10		+10	–10		+10	µA
I_{CC2}	V_{CC} Current, TTL Inactive	(Note 7)		12	25		10	15	mA
I_{CC3}	V_{CC} Current, CMOS Standby	(Note 8)		80	300		40	150	µA
I_{CC4}	V_{CC} Current, Data Retention	V_{CC} = 3.0 V (Note 9)		10	150		5	50	µA
C_{IN}	Input Capacitance	Ambient Temp = 25°C, V_{CC} = 5.0 V			5			5	pF
C_{OUT}	Output Capacitance	Test Frequency = 1 MHz (Note 10)			7			7	pF

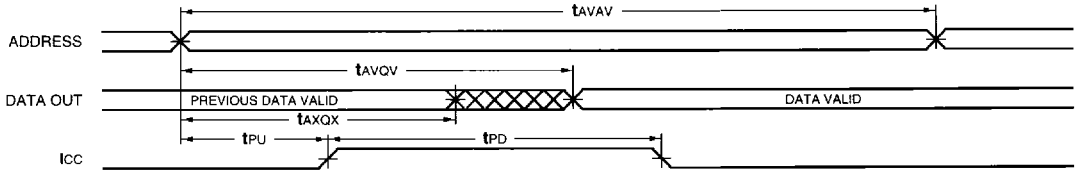
			L7C185-				
Symbol	Parameter	Test Condition	25	20	15	12	Unit
I_{CC1}	V_{CC} Current, Active	(Note 6)	115	135	160	195	mA

SWITCHING CHARACTERISTICS *Over Operating Range*

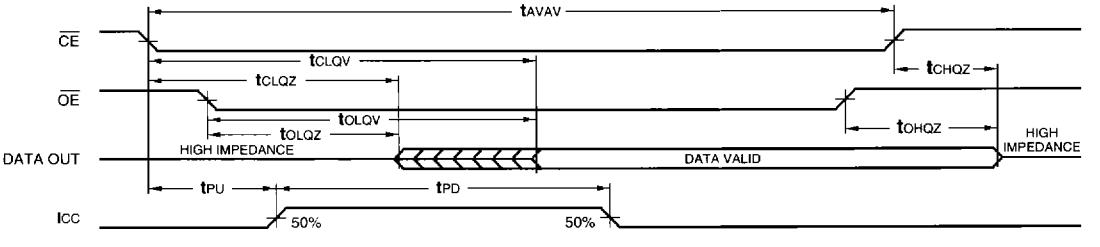
READ CYCLE *Notes 5, 11, 12, 22, 23, 24 (ns)*

		L7C185–							
		25		20		15		12	
Symbol	Parameter	Min	Max	Min	Max	Min	Max	Min	Max
t_{AVAV}	Read Cycle Time	25		20		15		12	
t_{AVQV}	Address Valid to Output Valid (Notes 13, 14)		25		20		15		12
t_{AXQX}	Address Change to Output Change	3		3		3		3	
t_{CLQV}	Chip Enable Low to Output Valid (Notes 13, 15)		25		20		15		12
t_{CLQZ}	Chip Enable Low to Output Low Z (Notes 20, 21)	3		3		3		3	
t_{CHQZ}	Chip Enable High to Output High Z (Notes 20, 21)		10		8		8		5
t_{OLQV}	Output Enable Low to Output Valid		12		10		8		6
t_{OLQZ}	Output Enable Low to Output Low Z (Notes 20, 21)	0		0		0		0	
t_{OHQZ}	Output Enable High to Output High Z (Notes 20, 21)		10		8		5		5
t_{PU}	Input Transition to Power Up (Notes 10, 19)	0		0		0		0	
t_{PD}	Power Up to Power Down (Notes 10, 19)		25		20		20		20
t_{CHVL}	Chip Enable High to Data Retention (Note 10)	0		0		0		0	

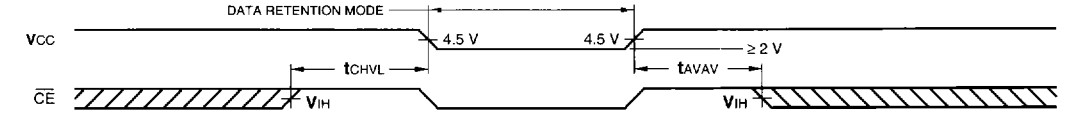
READ CYCLE — ADDRESS CONTROLLED *Notes 13, 14*



READ CYCLE — $\overline{CE}/\overline{OE}$ CONTROLLED *Notes 13, 15*



DATA RETENTION *Note 9*

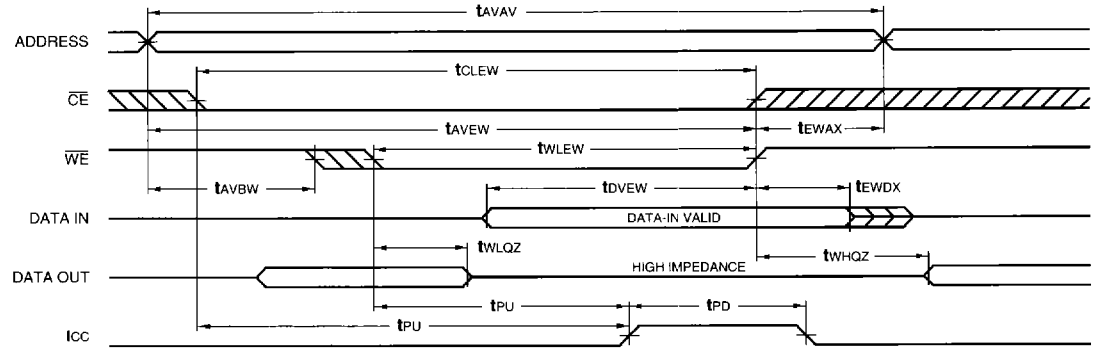


SWITCHING CHARACTERISTICS *Over Operating Range*

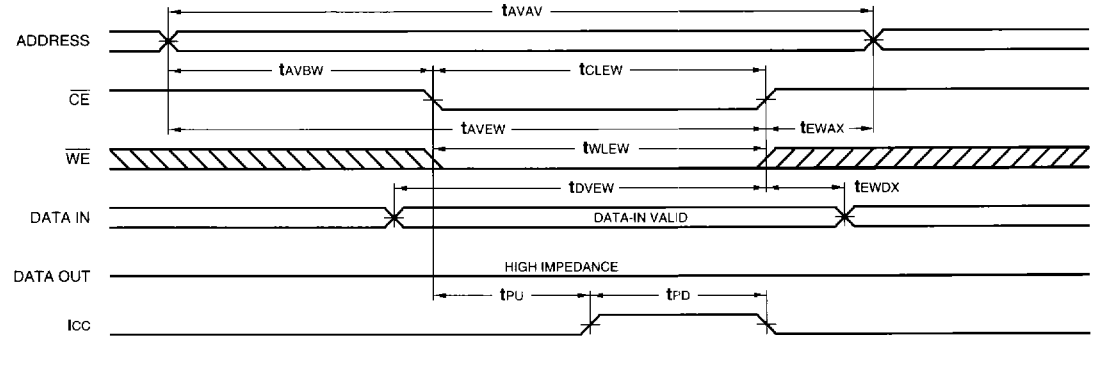
WRITE CYCLE *Notes 5, 11, 12, 22, 23, 24 (ns)*

		L7C185–							
		25		20		15		12	
Symbol	Parameter	Min	Max	Min	Max	Min	Max	Min	Max
t_{AVAV}	Write Cycle Time	20		20		15		12	
t_{CLEW}	Chip Enable Low to End of Write Cycle	15		15		12		10	
t_{AVBW}	Address Valid to Beginning of Write Cycle	0		0		0		0	
t_{AVEW}	Address Valid to End of Write Cycle	15		15		12		10	
t_{EWAX}	End of Write Cycle to Address Change	0		0		0		0	
t_{WLEW}	Write Enable Low to End of Write Cycle	15		15		12		10	
t_{DVEW}	Data Valid to End of Write Cycle	10		10		7		6	
t_{EWDX}	End of Write Cycle to Data Change	0		0		0		0	
t_{WHQZ}	Write Enable High to Output Low Z (Notes 20, 21)	0		0		0		0	
t_{WLQZ}	Write Enable Low to Output High Z (Notes 20, 21)		7		7		5		4

WRITE CYCLE — $\overline{WE}$ CONTROLLED *Notes 16, 17, 18, 19*



WRITE CYCLE — $\overline{CE}$ CONTROLLED *Notes 16, 17, 18, 19*



NOTES

1. Maximum Ratings indicate stress specifications only. Functional operation of these products at values beyond those indicated in the Operating Conditions table is not implied. Exposure to maximum rating conditions for extended periods may affect reliability of the tested device.

2. The products described by this specification include internal circuitry designed to protect the chip from damaging substrate injection currents and accumulations of static charge. Nevertheless, conventional precautions should be observed during storage, handling, and use of these circuits in order to avoid exposure to excessive electrical stress values.

3. This product provides hard clamping of transient undershoot. Input levels below ground will be clamped beginning at –0.6 V. A current in excess of 100 mA is required to reach –2.0 V. The device can withstand indefinite operation with inputs as low as –3 V subject only to power dissipation and bond wire fusing constraints.

4. Tested with GND ≤ V_{OUT} ≤ V_{CC}. The device is disabled, i.e., $\overline{CE_1}$ = V_{CC}, CE_2 = GND.

5. A series of normalized curves is available to supply the designer with typical DC and AC parametric information for Logic Devices Static RAMs. These curves may be used to determine device characteristics at various temperatures and voltage levels.

6. Tested with all address and data inputs changing at the maximum cycle rate. The device is continuously enabled for writing, i.e., $\overline{CE_1}$ ≤ V_{IL}, CE_2 ≥ V_{IH}, $\overline{WE}$ ≤ V_{IL}. Input pulse levels are 0 to 3.0 V.

7. Tested with outputs open and all address and data inputs changing at the maximum read cycle rate. The device is continuously disabled, i.e., $\overline{CE_1}$ ≥ V_{IH}, CE_2 ≤ V_{IL}.

8. Tested with outputs open and all address and data inputs stable. The device is continuously disabled, i.e., $\overline{CE_1}$ = V_{CC}, CE_2 = GND. Input levels are within 0.2 V of V_{CC} or GND.

9. Data retention operation requires that V_{CC} never drop below 2.0 V. $\overline{CE_1}$ must be ≥ V_{CC} – 0.2 V or CE_2 must be ≤ 0.2 V. All other inputs must meet V_{IN} ≥ V_{CC} – 0.2 V or V_{IN} ≤ 0.2 V to ensure full powerdown. For low power version (if applicable), this requirement applies only to $\overline{CE_1}$, CE_2, and $\overline{WE}$; there are no restrictions on data and address.

10. These parameters are guaranteed but not 100% tested.

11. Test conditions assume input transition times of less than 3 ns, reference levels of 1.5 V, output loading for specified I_{OL} and I_{OH} plus 30 pF (Fig. 1a), and input pulse levels of 0 to 3.0 V (Fig. 2).

12. Each parameter is shown as a minimum or maximum value. Input requirements are specified from the point of view of the external system driving the chip. For example, t_{AVEW} is specified as a minimum since the external system must supply at least that much time to meet the worst-case requirements of all parts. Responses from the internal circuitry are specified from the point of view of the device. Access time, for example, is specified as a maximum since worst-case operation of any device always provides data within that time.

13. $\overline{WE}$ is high for the read cycle.

14. The chip is continuously selected ($\overline{CE_1}$ low, CE_2 high).

15. All address lines are valid prior-to or coincident-with the $\overline{CE_1}$ and CE_2 transition to active.

16. The internal write cycle of the memory is defined by the overlap of $\overline{CE_1}$ and CE_2 active and $\overline{WE}$ low. All three signals must be active to initiate a write. Any signal can terminate a write by going inactive. The address, data, and control input setup and hold times should be referenced to the signal that becomes active last or becomes inactive first.

17. If $\overline{WE}$ goes low before or concurrent with the latter of $\overline{CE_1}$ and CE_2 going active, the output remains in a high impedance state.

18. If $\overline{CE_1}$ and CE_2 goes inactive before or concurrent with $\overline{WE}$ going high, the output remains in a high impedance state.

19. Powerup from I_{CC2} to I_{CC1} occurs as a result of any of the following conditions:

a. Rising edge of CE_2 ($\overline{CE_1}$ active) or the falling edge of $\overline{CE_1}$ (CE_2 active).

b. Falling edge of $\overline{WE}$ ($\overline{CE_1}$, CE_2 active).

c. Transition on any address line ($\overline{CE_1}$, CE_2 active).

d. Transition on any data line ($\overline{CE_1}$, CE_2, and $\overline{WE}$ active).

The device automatically powers down from I_{CC1} to I_{CC2} after t_{PD} has elapsed from any of the prior conditions. This means that power dissipation is dependent on only cycle rate, and is not on Chip Select pulse width.

20. At any given temperature and voltage condition, output disable time is less than output enable time for any given device.

21. Transition is measured ±200 mV from steady state voltage with specified loading in Fig. 1b. This parameter is sampled and not 100% tested.

22. All address timings are referenced from the last valid address line to the first transitioning address line.

23. $\overline{CE_1}$, CE_2, or $\overline{WE}$ must be inactive during address transitions.

24. This product is a very high speed device and care must be taken during testing in order to realize valid test information. Inadequate attention to setups and procedures can cause a good part to be rejected as faulty. Long high inductance leads that cause supply bounce must be avoided by bringing the V_{CC} and ground planes directly up to the contactor fingers. A 0.01 µF high frequency capacitor is also required between V_{CC} and ground. To avoid signal reflections, proper terminations must be used.

FIGURE 1a.

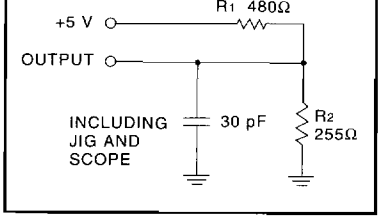


FIGURE 1b.

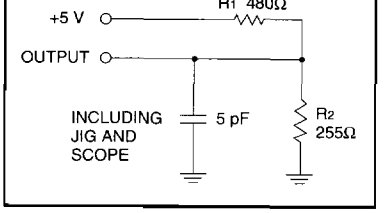
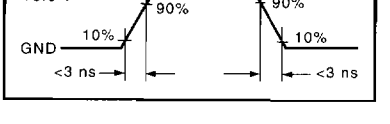
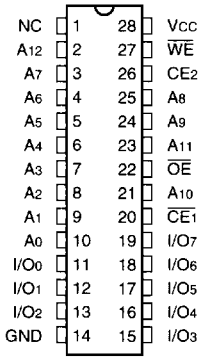


FIGURE 2.

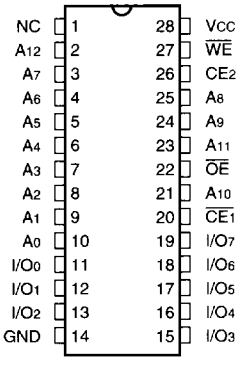


ORDERING INFORMATION

28-pin — 0.3" wide



28-pin — 0.6" wide

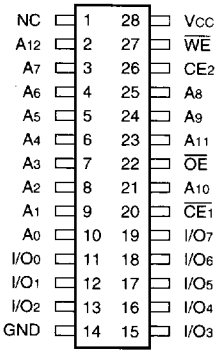


Speed	Plastic DIP (P10)	Ceramic DIP (C5)	Plastic DIP (P9)	Ceramic DIP (C6)
	0°C to +70°C — Commercial Screening			
20 ns	L7C185PC20*	L7C185CC20*	L7C185NC20*	L7C185IC20*
15 ns	L7C185PC15*	L7C185CC15*	L7C185NC15*	L7C185IC15*
12 ns	L7C185PC12*	L7C185CC12*	L7C185NC12*	L7C185IC12*
	–40°C to +85°C — Commercial Screening			
20 ns	L7C185PI20*		L7C185NI20*	
15 ns	L7C185PI15*		L7C185NI15*	
12 ns	L7C185PI12*		L7C185NI12*	
	–55°C to +125°C — Commercial Screening			
25 ns		L7C185CM25*		L7C185IM25*
20 ns		L7C185CM20*		L7C185IM20*
15 ns		L7C185CM15*		L7C185IM15*
	–55°C to +125°C — MIL-STD-883 Compliant			
25 ns		L7C185CMB25*		L7C185IMB25*
20 ns		L7C185CMB20*		L7C185IMB20*
15 ns		L7C185CMB15*		L7C185IMB15*

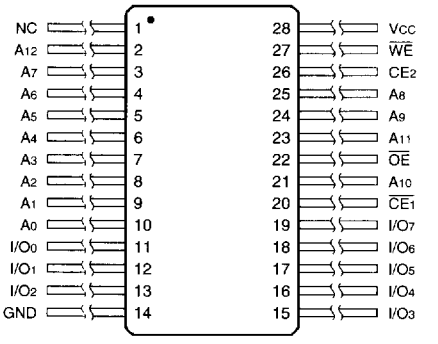
***The Low Power version is specified by adding the "L" suffix after the speed grade (e.g., L7C185CMB15L)**

ORDERING INFORMATION

28-pin — 0.3" wide



28-pin

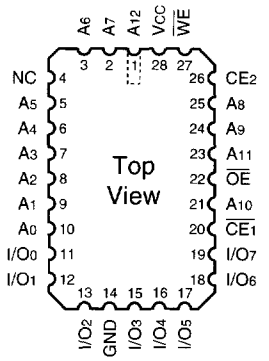


Speed	Plastic SOJ (W2)	Ceramic Flatpack (M2)
	0°C to +70°C — Commercial Screening	
20 ns	L7C185WC20*	L7C185MC20*
15 ns	L7C185WC15*	L7C185MC15*
12 ns	L7C185WC12*	L7C185MC12*
	–40°C to +85°C — Commercial Screening	
20 ns	L7C185WI20*	
15 ns	L7C185WI15*	
12 ns	L7C185WI12*	
	–55°C to +125°C — Commercial Screening	
25 ns		L7C185MM25*
20 ns		L7C185MM20*
15 ns		L7C185MM15*
	–55°C to +125°C — MIL-STD-883 Compliant	
25 ns		L7C185MMB25*
20 ns		L7C185MMB20*
15 ns		L7C185MMB15*

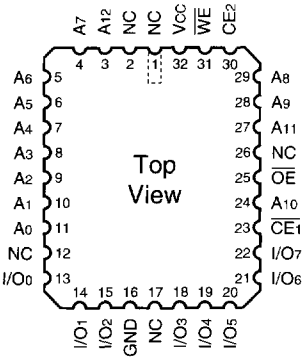
***The Low Power version is specified by adding the "L" suffix after the speed grade (e.g., L7C185MMB15L)**

ORDERING INFORMATION

28-pin



32-pin



Speed	Ceramic Leadless Chip Carrier (K5)	Ceramic Leadless Chip Carrier (K7)
	0°C to +70°C — Commercial Screening	
20 ns	L7C185KC20*	L7C185TC20*
15 ns	L7C185KC15*	L7C185TC15*
12 ns	L7C185KC12*	L7C185TC12*
	–40°C to +85°C — Commercial Screening	
20 ns		
15 ns		
12 ns		
	–55°C to +125°C — Commercial Screening	
25 ns	L7C185KM25*	L7C185TM25*
20 ns	L7C185KM20*	L7C185TM20*
15 ns	L7C185KM15*	L7C185TM15*
	–55°C to +125°C — MIL-STD-883 Compliant	
25 ns	L7C185KMB25*	L7C185TMB25*
20 ns	L7C185KMB20*	L7C185TMB20*
15 ns	L7C185KMB15*	L7C185TMB15*

***The Low Power version is specified by adding the "L" suffix after the speed grade (e.g., L7C185KMB15L)**