

# RQJ0304DQDQA

Silicon P Channel MOS FET  
Power Switching

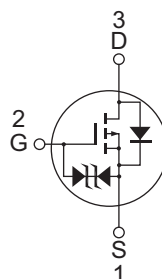
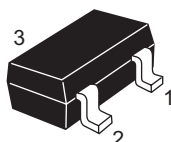
R07DS0296EJ0200  
(Previous: REJ03G1717-0100)  
Rev.2.00  
Mar 28, 2011

## Features

- Low gate drive  
     $V_{DSS}$  : -30 V and 2.5 V gate drive
- Low drive current
- High speed switching
- Small traditional package (MPAK)

## Outline

RENESAS Package code: PLSP0003ZB-A  
(Package name: MPAK)



1. Source
2. Gate
3. Drain

Notes: Marking is "DQ".

## Absolute Maximum Ratings

( $T_a = 25^\circ\text{C}$ )

Item	Symbol	Ratings	Unit
Drain to source voltage	$V_{DSS}$	-30	V
Gate to source voltage	$V_{GSS}$	+8 / -12	V
Drain current	$I_D$	-1.8	A
Drain peak current	$I_{D(pulse)}$ <sup>Note1</sup>	-8	A
Body - drain diode reverse drain current	$I_{DR}$	1.8	A
Channel dissipation	$P_{ch}$ <sup>Note2</sup>	0.8	W
Channel temperature	$T_{ch}$	150	$^\circ\text{C}$
Storage temperature	$T_{stg}$	-55 to +150	$^\circ\text{C}$

- Notes: 1.  $PW \leq 10 \mu\text{s}$ , Duty cycle  $\leq 1\%$   
 2. When using the glass epoxy board (FR-4 40 × 40 × 1 mm)

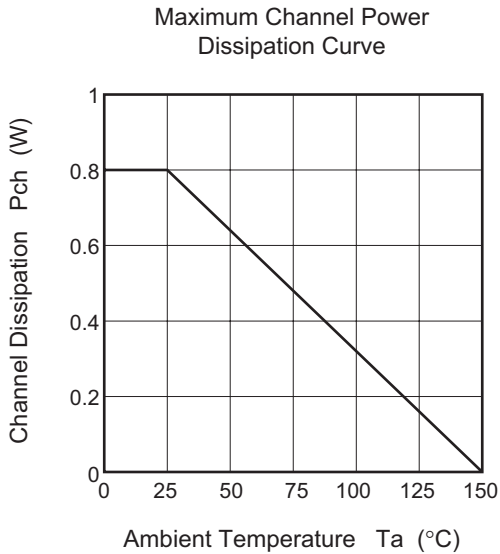
## Electrical Characteristics

(Ta = 25°C)

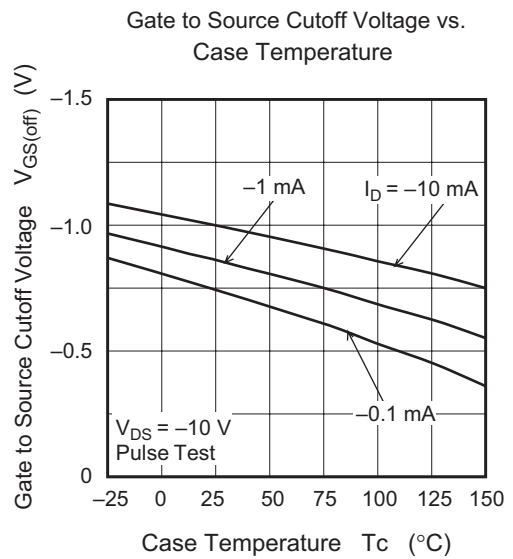
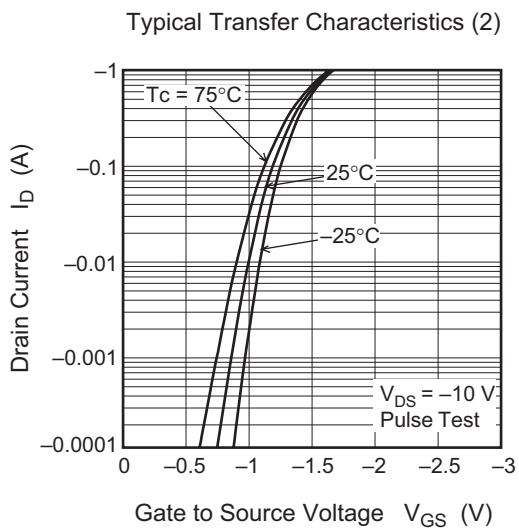
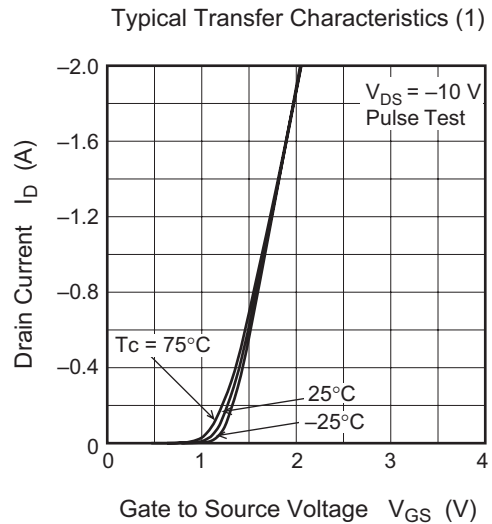
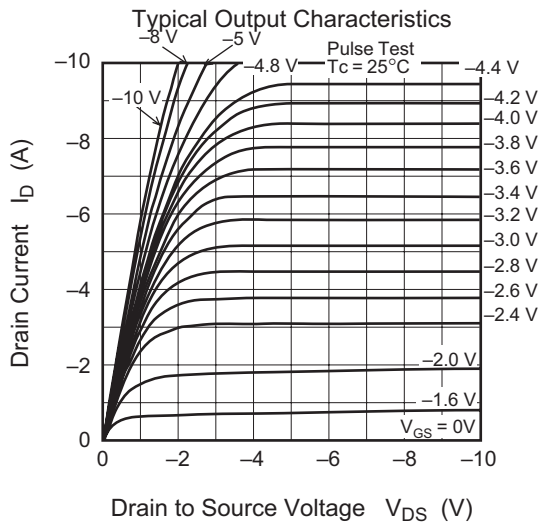
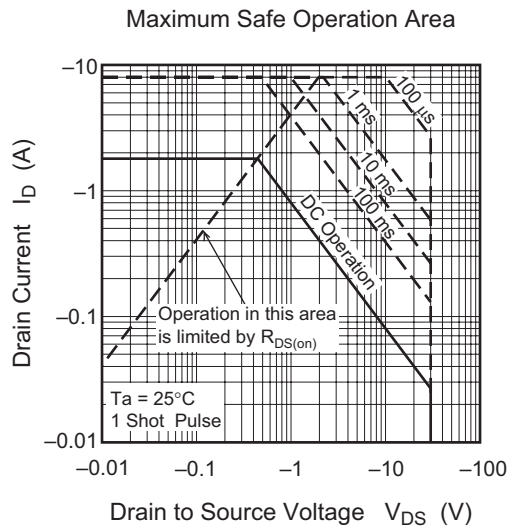
Item	Symbol	Min	Typ	Max	Unit	Test conditions
Drain to source breakdown voltage	$V_{(BR)DSS}$	-30	—	—	V	$I_D = -10 \text{ mA}$ , $V_{GS} = 0$
Gate to source breakdown voltage	$V_{(BR)GSS}$	+8	—	—	V	$I_G = +100 \text{ }\mu\text{A}$ , $V_{DS} = 0$
Gate to source breakdown voltage	$V_{(BR)GSS}$	-12	—	—	V	$I_G = -100 \text{ }\mu\text{A}$ , $V_{DS} = 0$
Gate to source leak current	$I_{GSS}$	—	—	+10	$\mu\text{A}$	$V_{GS} = +6 \text{ V}$ , $V_{DS} = 0$
Gate to source leak current	$I_{GSS}$	—	—	-10	$\mu\text{A}$	$V_{GS} = -10 \text{ V}$ , $V_{DS} = 0$
Drain to source leak current	$I_{DSS}$	—	—	-1	$\mu\text{A}$	$V_{DS} = -30 \text{ V}$ , $V_{GS} = 0$
Gate to source cutoff voltage	$V_{GS(off)}$	-0.4	—	-1.4	V	$V_{DS} = -10 \text{ V}$ , $I_D = -1 \text{ mA}$
Drain to source on state resistance	$R_{DS(on)}$	—	195	245	$\text{m}\Omega$	$I_D = -1.0 \text{ A}$ , $V_{GS} = -4.5 \text{ V}$ <sup>Note3</sup>
Drain to source on state resistance	$R_{DS(on)}$	—	300	420	$\text{m}\Omega$	$I_D = -1.0 \text{ A}$ , $V_{GS} = -2.5 \text{ V}$ <sup>Note3</sup>
Forward transfer admittance	$ y_{fs} $	1.8	2.5	—	S	$I_D = -1.0 \text{ A}$ , $V_{DS} = -10 \text{ V}$ <sup>Note3</sup>
Input capacitance	$C_{iss}$	—	185	—	pF	$V_{DS} = -10 \text{ V}$ , $V_{GS} = 0$ , $f = 1 \text{ MHz}$
Output capacitance	$C_{oss}$	—	45	—	pF	
Reverse transfer capacitance	$C_{rss}$	—	25	—	pF	
Turn - on delay time	$t_{d(on)}$	—	18	—	ns	$I_D = -1.0 \text{ A}$ $V_{GS} = -4.5 \text{ V}$ $R_L = 10 \text{ }\Omega$ $R_g = 4.7 \text{ }\Omega$
Rise time	$t_r$	—	33	—	ns	
Turn - off delay time	$t_{d(off)}$	—	22	—	ns	
Fall time	$t_f$	—	5	—	ns	
Total gate charge	$Q_g$	—	1.9	—	nC	$V_{DD} = -10 \text{ V}$
Gate to Source charge	$Q_{gs}$	—	0.4	—	nC	$V_{GS} = -4.5 \text{ V}$
Gate to drain charge	$Q_{gd}$	—	0.7	—	nC	$I_D = -2.0 \text{ A}$
Body - drain diode forward voltage	$V_{DF}$	—	-0.9	-1.3	V	$I_F = -2.0 \text{ A}$ , $V_{GS} = 0$ <sup>Note3</sup>

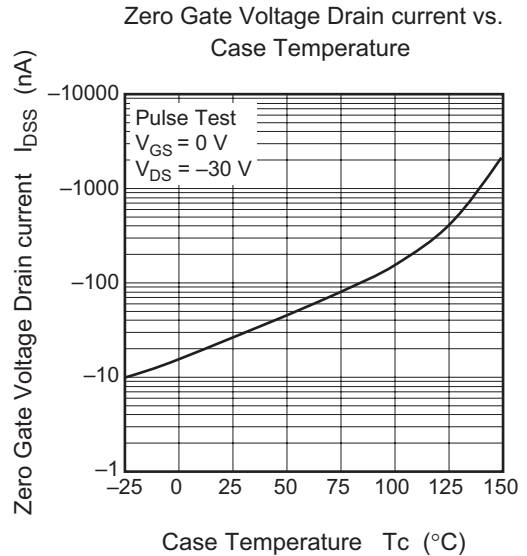
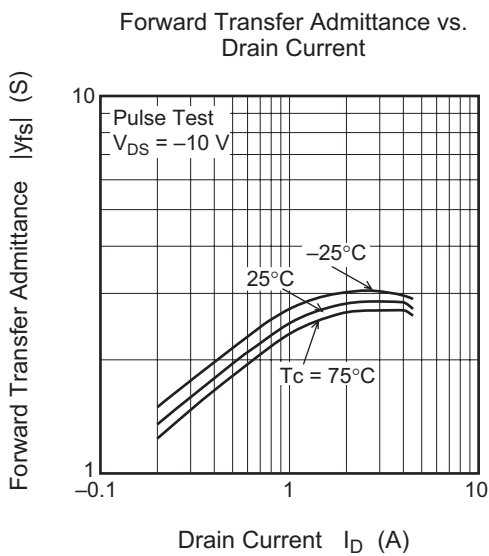
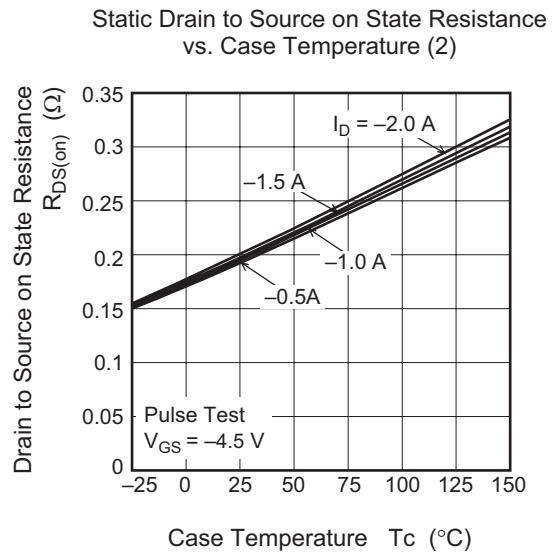
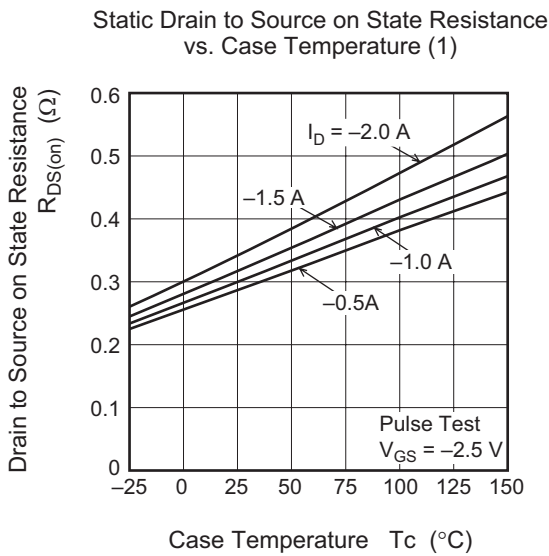
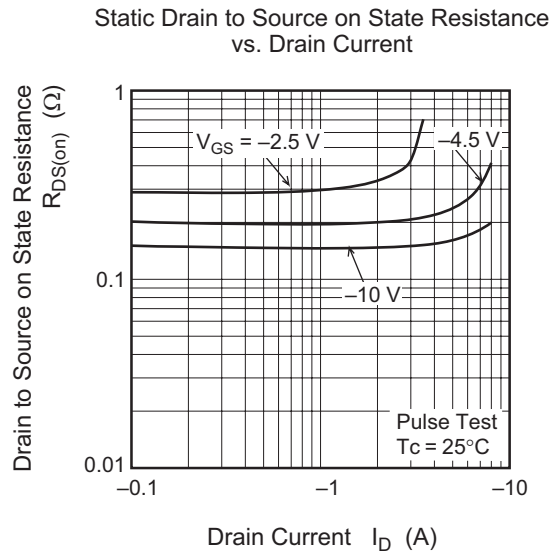
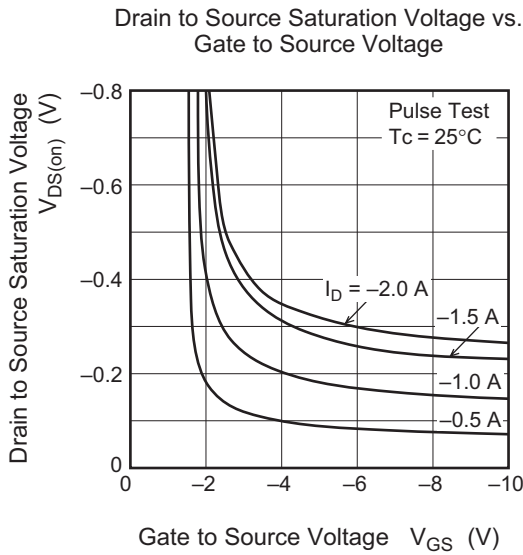
Notes: 3. Pulse test

Main Characteristics

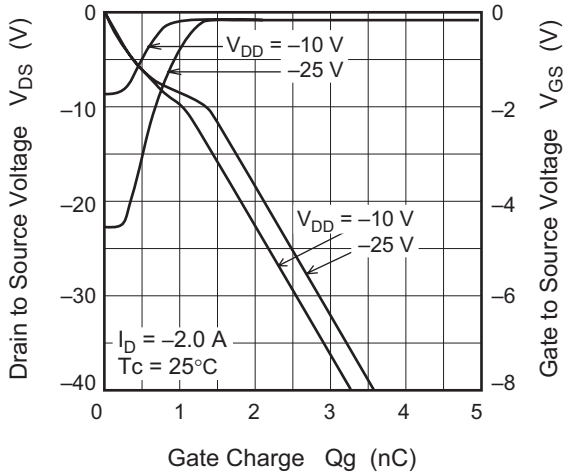


\*When using the glass epoxy board (FR-4 40 x 40 x 1 mm)

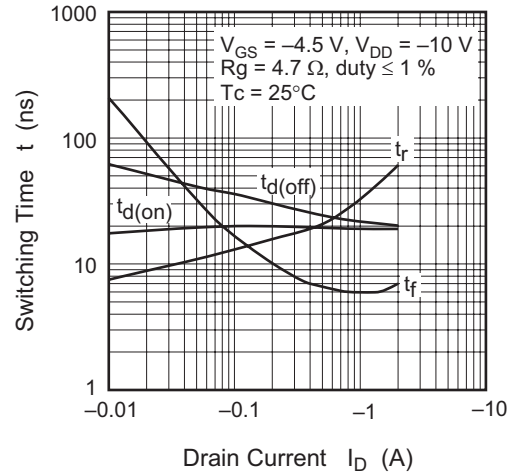




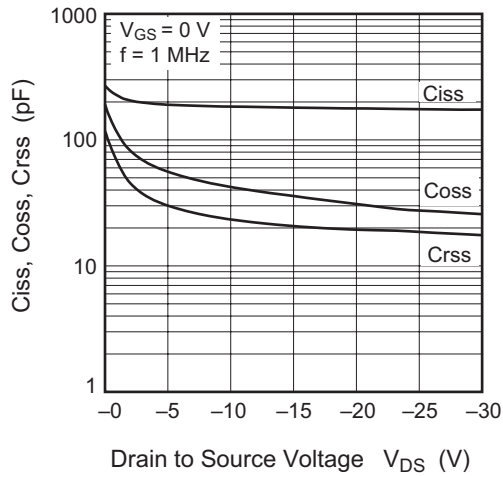
Dynamic Input Characteristics



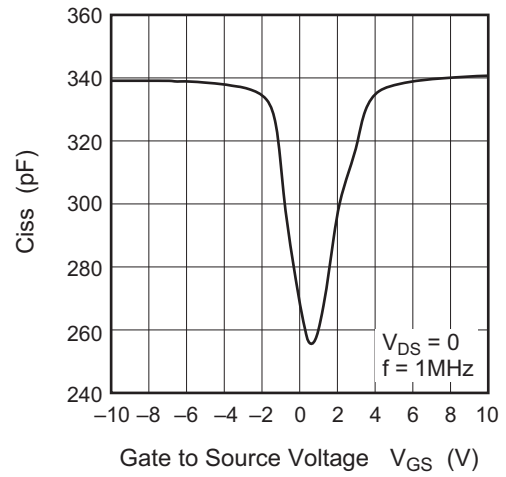
Switching Characteristics



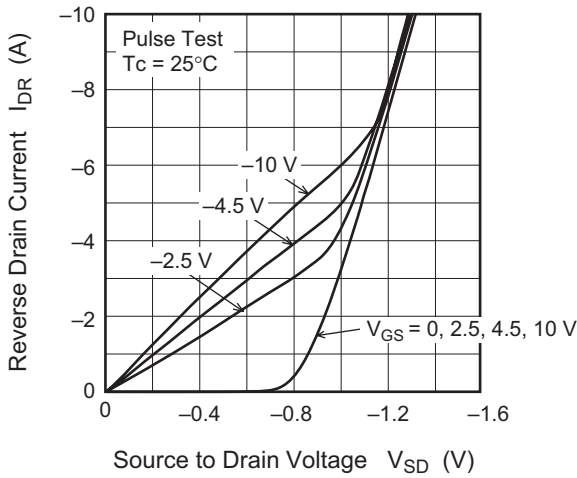
Typical Capacitance vs. Drain to Source Voltage



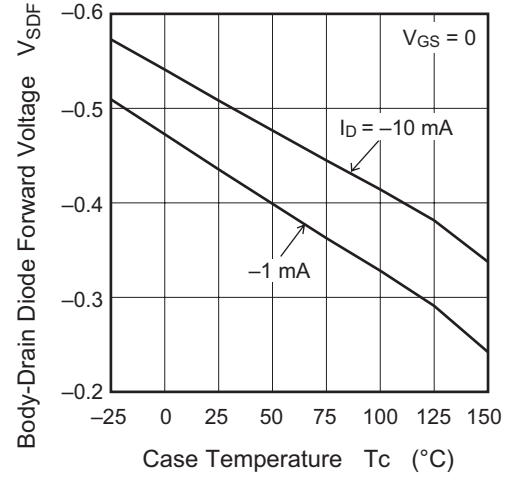
Input Capacitance vs. Gate to Source Voltage

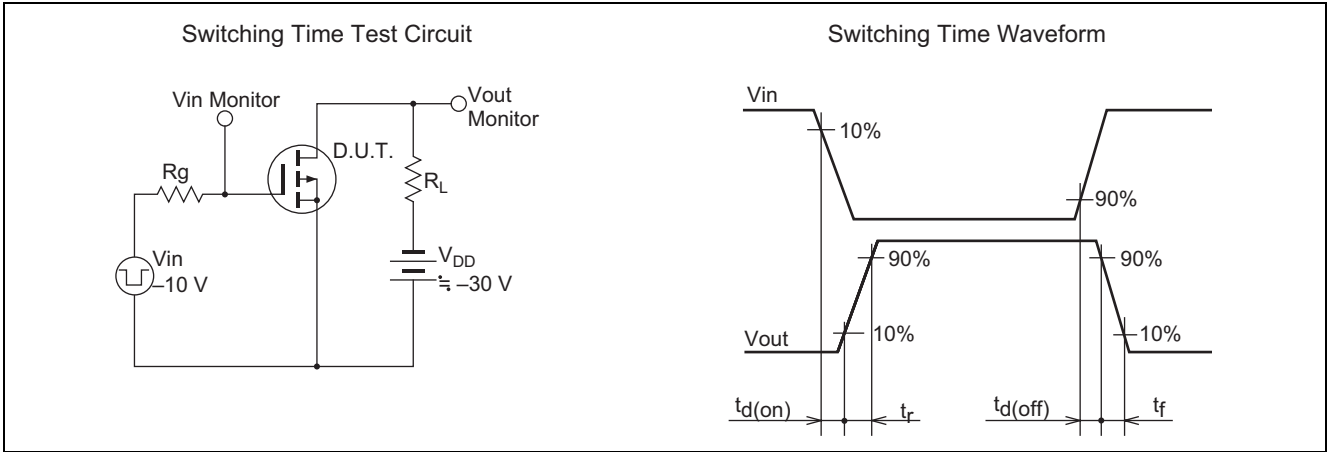


Reverse Drain Current vs. Source to Drain Voltage

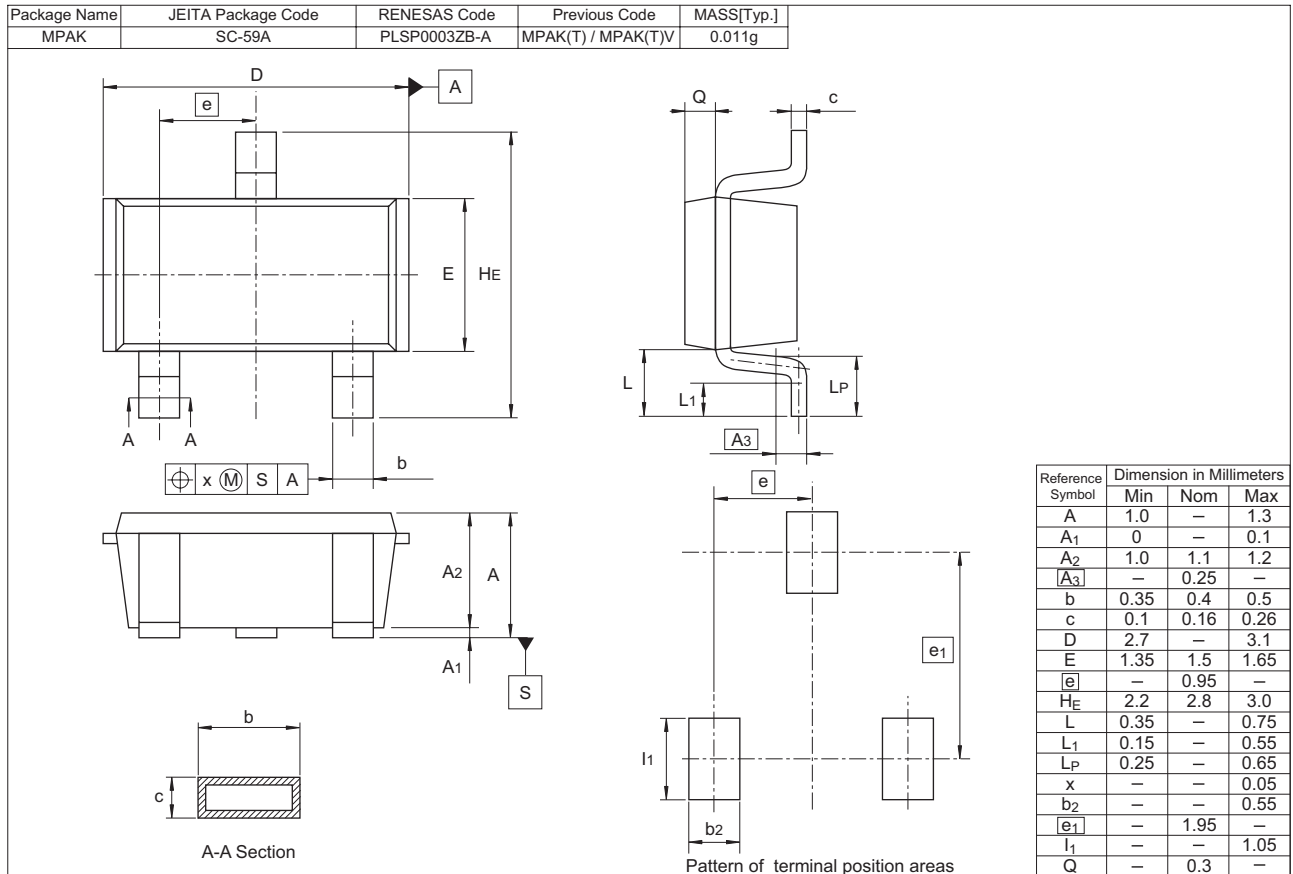


Body-Drain Diode Forward Voltage vs. Case Temperature





### Package Dimensions



### Ordering Information

Orderable Part Number	Quantity	Shipping Container
RQJ0304DQDQATL-H	3000 pcs.	φ178 mm reel, 8 mm Emboss taping

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2880 Scott Boulevard Santa Clara, CA 95050-2554, U.S.A.  
Tel: +1-408-586-6000, Fax: +1-408-586-6130

**Renesas Electronics Canada Limited**  
1101 Nicholson Road, Newmarket, Ontario L3Y 9C3, Canada  
Tel: +1-905-898-5441, Fax: +1-905-898-3220

**Renesas Electronics Europe Limited**  
Dukes Meadow, Millboard Road, Bourne End, Buckinghamshire, SL8 5FH, U.K.  
Tel: +44-1628-585-100, Fax: +44-1628-585-900

**Renesas Electronics Europe GmbH**  
Arcadiastrasse 10, 40472 Düsseldorf, Germany  
Tel: +49-211-65030, Fax: +49-211-6503-1327

**Renesas Electronics (China) Co., Ltd.**  
7th Floor, Quantum Plaza, No.27 ZhiChunLu Haidian District, Beijing 100083, P.R.China  
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Unit 204, 205, AZIA Center, No.1233 Lujiazui Ring Rd., Pudong District, Shanghai 200120, China  
Tel: +86-21-5877-1818, Fax: +86-21-6887-7858 / -7898

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Unit 1601-1613, 16/F., Tower 2, Grand Century Place, 193 Prince Edward Road West, Mongkok, Kowloon, Hong Kong  
Tel: +852-2886-9318, Fax: +852 2886-9022/9044

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Tel: +886-2-8175-9600, Fax: +886 2-8175-9670

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Tel: +65-6213-0200, Fax: +65-6276-8001

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Unit 906, Block B, Menara Amcorp, Amcorp Trade Centre, No. 18, Jin Persiaran Barat, 46050 Petaling Jaya, Selangor Darul Ehsan, Malaysia  
Tel: +60-3-7955-9390, Fax: +60-3-7955-9510

**Renesas Electronics Korea Co., Ltd.**  
11F., Samik Lavied' or Bldg., 720-2 Yeoksam-Dong, Kangnam-Ku, Seoul 135-080, Korea  
Tel: +82-2-558-3737, Fax: +82-2-558-5141