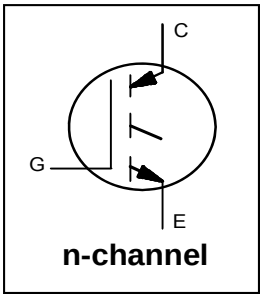
Features

- Advanced Trench IGBT Technology
- Optimized for Sustain and Energy Recovery circuits in PDP applications
- Low $V_{CE(on)}$ and Energy per Pulse (E_{PULSE}™) for improved panel efficiency
- High repetitive peak current capability
- Lead Free package

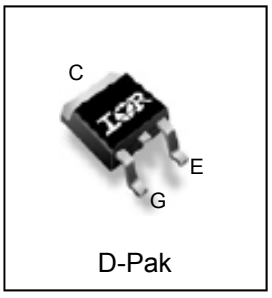
Description

This IGBT is specifically designed for applications in Plasma Display Panels. This device utilizes advanced trench IGBT technology to achieve low $V_{CE(on)}$ and low E_{PULSE}™ rating per silicon area which improve panel efficiency. Additional features are 150°C operating junction temperature and high repetitive peak current capability. These features combine to make this IGBT a highly efficient, robust and reliable device for PDP applications.

Key Parameters		
V_{CE} min	360	V
$V_{CE(ON)}$ typ. @ I_C = 20A	1.42	V
I_{RP} max @ T_C= 25°C	276	A
T_J max	150	°C



n-channel



D-Pak

G	C	E
Gate	Collector	Emitter

Ordering Information

Base part number	Package Type	Standard Pack		Complete Part Number
		Form	Quantity	
IRG7RA13UPbF	D-Pak	Tube	75	IRG7RA13UPbF
		Tape and Reel	2000	IRG7RA13UTRPbF
		Tape and Reel Left	3000	IRG7RA13UTRLPbF
		Tape and Reel Right	3000	IRG7RA13UTRRPbF

Absolute Maximum Ratings

	Parameter	Max.	Units
V_{GE}	Gate-to-Emitter Voltage	±30	V
I_C @ T_C = 25°C	Continuous Collector Current, V_{GE} @ 15V	40	A
I_C @ T_C = 100°C	Continuous Collector, V_{GE} @ 15V	20	
I_{RP} @ T_C = 25°C	Repetitive Peak Current ①	276	
P_D @T_C = 25°C	Power Dissipation	78	W
P_D @T_C = 100°C	Power Dissipation	31	
	Linear Derating Factor	0.63	W/°C
T_J T_{STG}	Operating Junction and Storage Temperature Range	-40 to + 150	°C
	Soldering Temperature for 10 seconds	300	

Thermal Resistance

	Parameter	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case ②	—	1.6	°C/W
$R_{\theta JA}$	Junction-to-Ambient (PCB Mount) ④	—	50	

Electrical Characteristics @ T_J = 25°C (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
BV_{CES}	Collector-to-Emitter Breakdown Voltage	360	—	—	V	V_{GE} = 0V, I_{CE} = 250µA
$\Delta BV_{CES}/\Delta T_J$	Breakdown Voltage Temp. Coefficient	—	0.4	—	V/°C	Reference to 25°C, I_{CE} = 1mA
$V_{CE(on)}$	Static Collector-to-Emitter Voltage	—	1.26	1.52	V	V_{GE} = 15V, I_{CE} = 12A ③
		—	1.42	—		V_{GE} = 15V, I_{CE} = 20A ③
			1.84	—		V_{GE} = 15V, I_{CE} = 40A ③
		—	2.25	—		V_{GE} = 15V, I_{CE} = 60A ③
		—	1.48	—		V_{GE} = 15V, I_{CE} = 20A, T_J = 150°C ③
$V_{GE(th)}$	Gate Threshold Voltage	2.2	—	4.7	V	V_{CE} = V_{GE}, I_{CE} = 1.0mA
$\Delta V_{GE(th)}/\Delta T_J$	Gate Threshold Voltage Coefficient	—	-10	—	mV/°C	
I_{CES}	Collector-to-Emitter Leakage Current	—	1.0	10	µA	V_{CE} = 360V, V_{GE} = 0V
		—	25	150		V_{CE} = 360V, V_{GE} = 0V, T_J = 125°C
		—	75	—		V_{CE} = 360V, V_{GE} = 0V, T_J = 150°C
I_{GES}	Gate-to-Emitter Forward Leakage	—	—	100	nA	V_{GE} = 30V
	Gate-to-Emitter Reverse Leakage	—	—	-100		V_{GE} = -30V
g_{fe}	Forward Transconductance	—	47	—	S	V_{CE} = 25V, I_{CE} = 12A
Q_g	Total Gate Charge	—	33	—	nC	V_{CE} = 240V, I_C = 12A, V_{GE} = 15V ③
Q_{gc}	Gate-to-Collector Charge	—	12	—		
$t_{d(on)}$	Turn-On delay time	—	11	—	ns	I_C = 12A, V_{CC} = 196V
t_r	Rise time	—	13	—		R_G = 10Ω, L=210µH
$t_{d(off)}$	Turn-Off delay time	—	75	—		T_J = 25°C
t_f	Fall time	—	120	—		
$t_{d(on)}$	Turn-On delay time	—	11	—	ns	I_C = 12A, V_{CC} = 196V
t_r	Rise time	—	14	—		R_G = 10Ω, L=200µH, L_S= 150nH
$t_{d(off)}$	Turn-Off delay time	—	86	—		T_J = 150°C
t_f	Fall time	—	190	—		
t_{st}	Shoot Through Blocking Time	100	—	—	ns	V_{CC} = 240V, V_{GE} = 15V, R_G= 5.1Ω
E_{PULSE}	Energy per Pulse	—	480	—	µJ	L = 220nH, C= 0.20µF, V_{GE} = 15V
						V_{CC} = 240V, R_G= 5.1Ω, T_J = 25°C
		—	570	—		L = 220nH, C= 0.20µF, V_{GE} = 15V
						V_{CC} = 240V, R_G= 5.1Ω, T_J = 100°C
ESD	Human Body Model	Class 1C (Per JEDEC standard JESD22-A114)				
	Machine Model	Class B (Per EIA/JEDEC standard EIA/JESD22-A115)				
C_{ies}	Input Capacitance	—	880	—	pF	V_{GE} = 0V
C_{oes}	Output Capacitance	—	47	—		V_{CE} = 30V
C_{res}	Reverse Transfer Capacitance	—	26	—		f = 1.0MHz
L_C	Internal Collector Inductance	—	4.5	—	nH	Between lead, 6mm (0.25in.)
L_E	Internal Emitter Inductance	—	7.5	—		from package and center of die contact

Notes:

① Half sine wave with duty cycle = 0.01, t_{on} = 1.0µsec.

② R_θ is measured at T_J approximately 90°C.

③ Pulse width ≤ 400µs; duty cycle ≤ 2%.

④ When mounted on 1" square PCB (FR-4 or G-10 Material). For recommended footprint and soldering techniques refer to application note #AN-994.

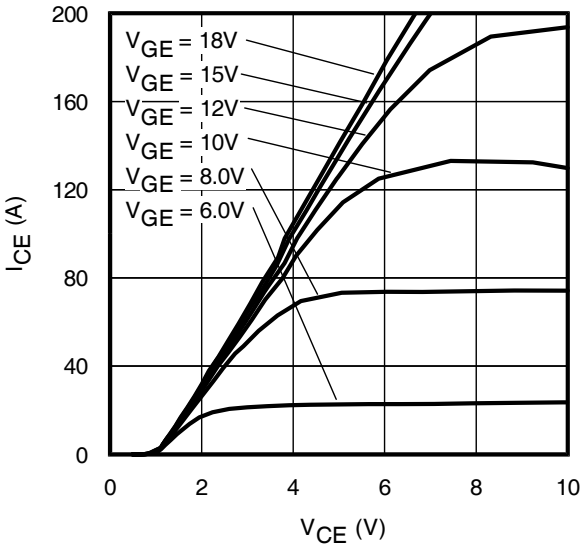


Fig 1. Typical Output Characteristics @ 25°C

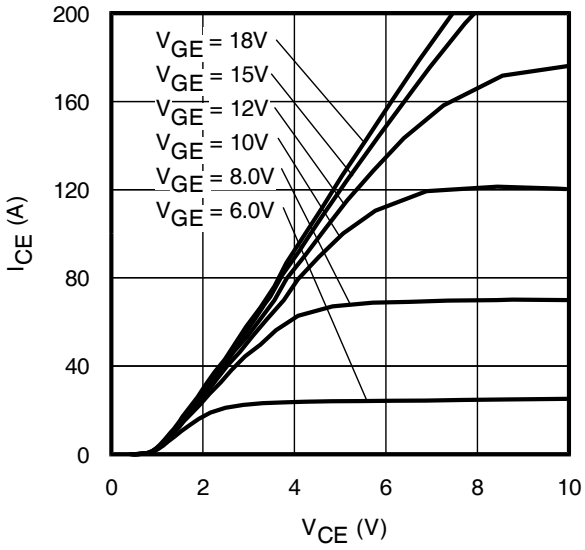


Fig 2. Typical Output Characteristics @ 75°C

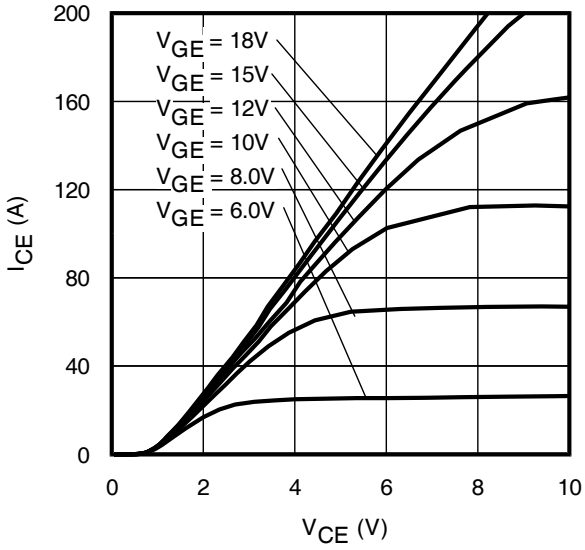


Fig 3. Typical Output Characteristics @ 125°C

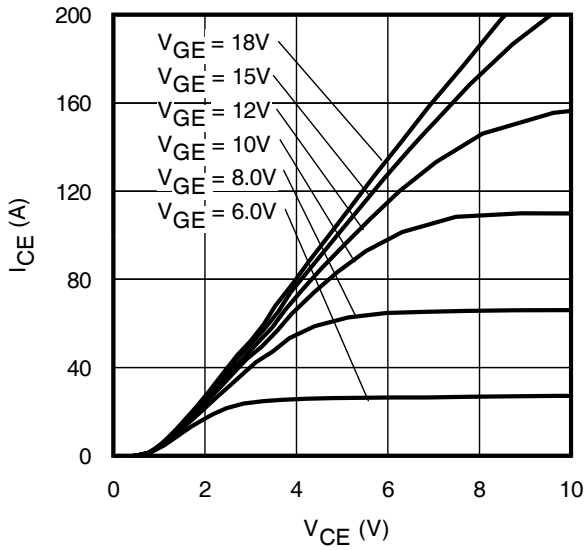


Fig 4. Typical Output Characteristics @ 150°C

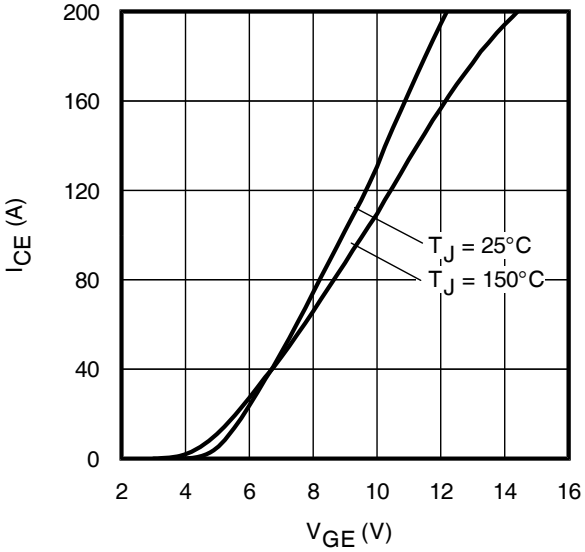


Fig 5. Typical Transfer Characteristics

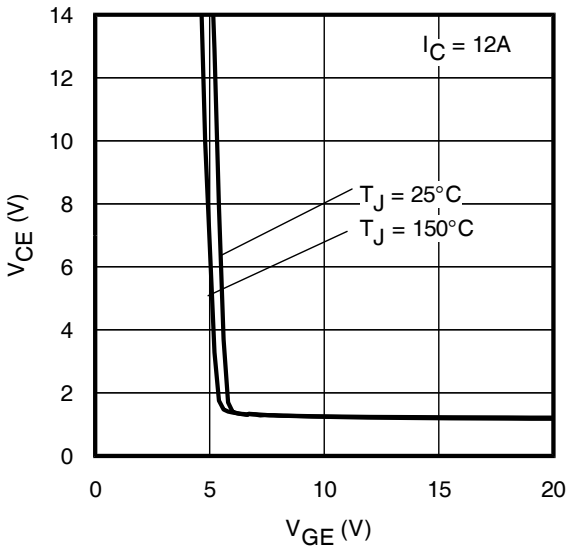


Fig 6. $V_{CE(ON)}$ vs. Gate Voltage

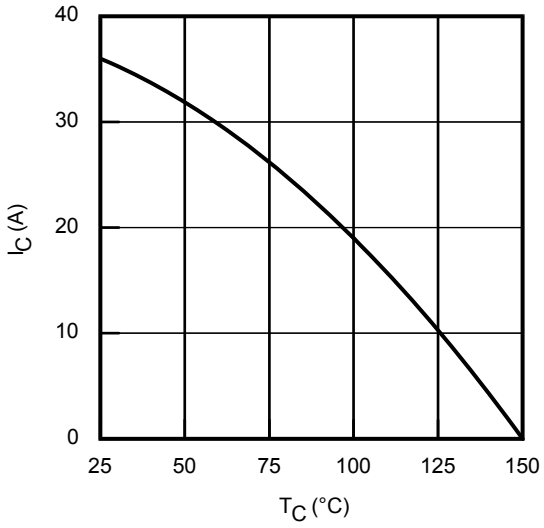


Fig 7. Maximum Collector Current vs. Case Temperature

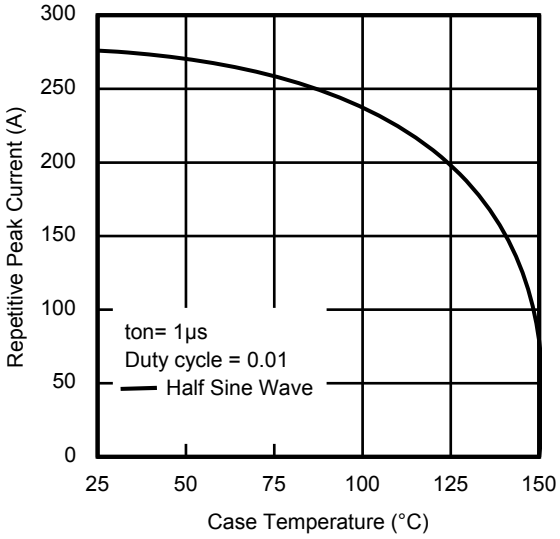


Fig 8. Typical Repetitive Peak Current vs. Case Temperature

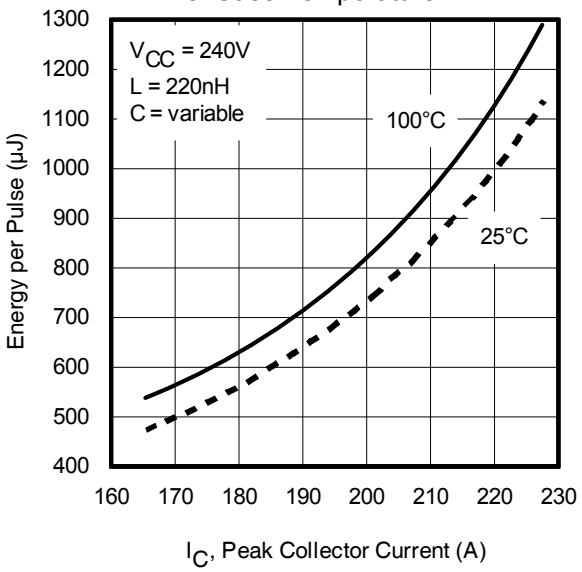


Fig 9. Typical E_{PULSE} vs. Collector Current

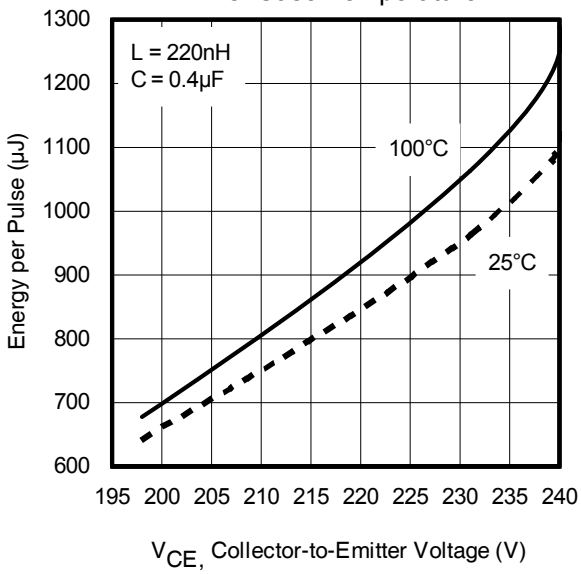


Fig 10. Typical E_{PULSE} vs. Collector-to-Emitter Voltage

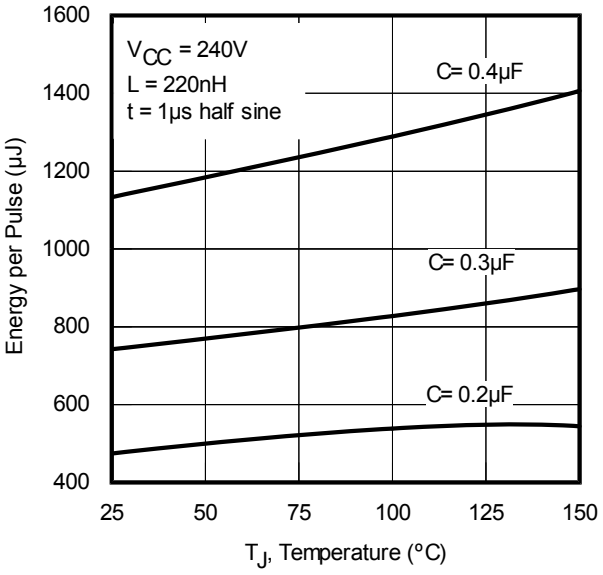


Fig 11. E_{PULSE} vs. Temperature

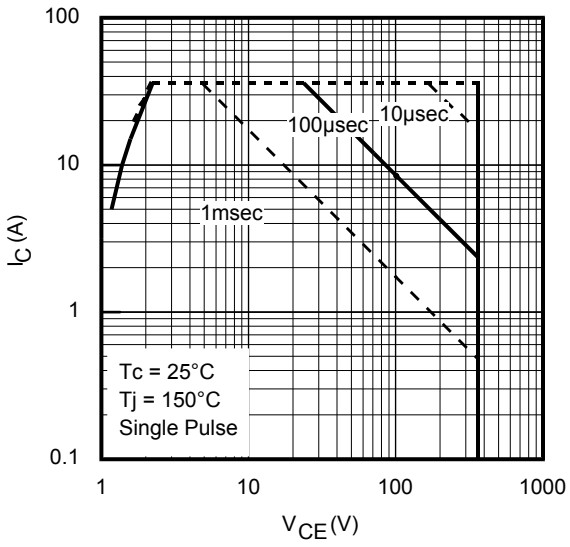


Fig 12. Forward Bias Safe Operating Area

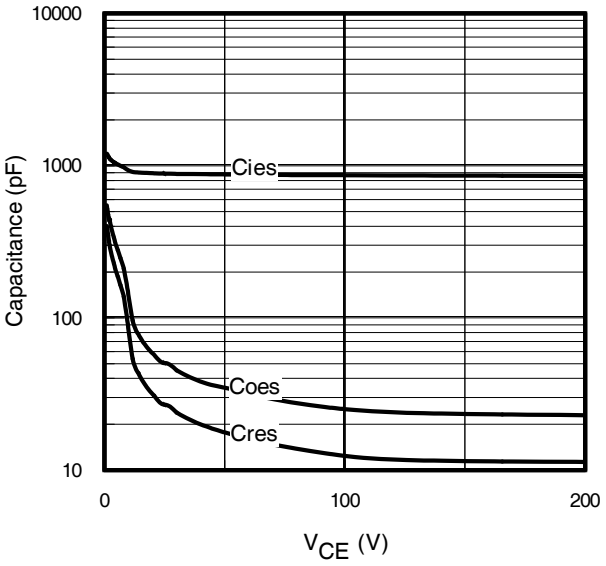


Fig 13. Typical Capacitance vs. Collector-to-Emitter Voltage

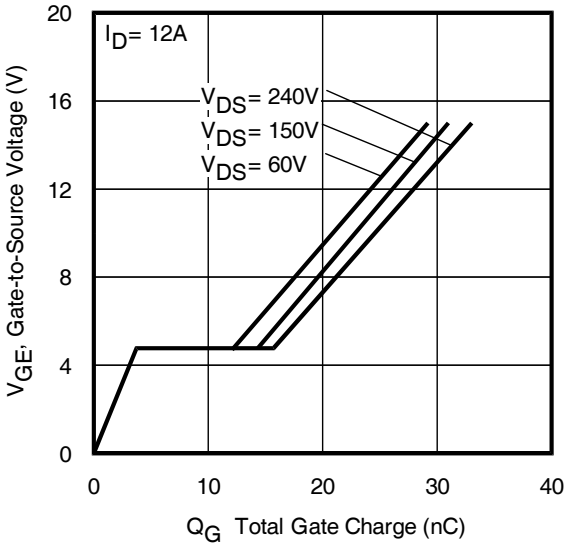


Fig 14. Typical Gate Charge vs. Gate-to-Emitter Voltage

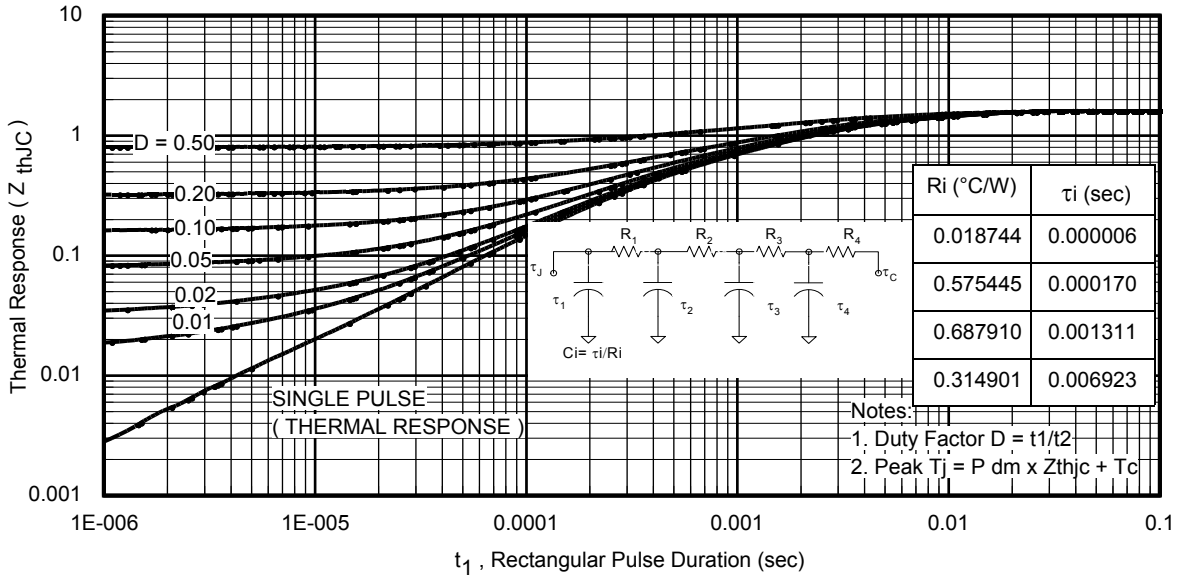


Fig 15. Maximum Effective Transient Thermal Impedance, Junction-to-Case

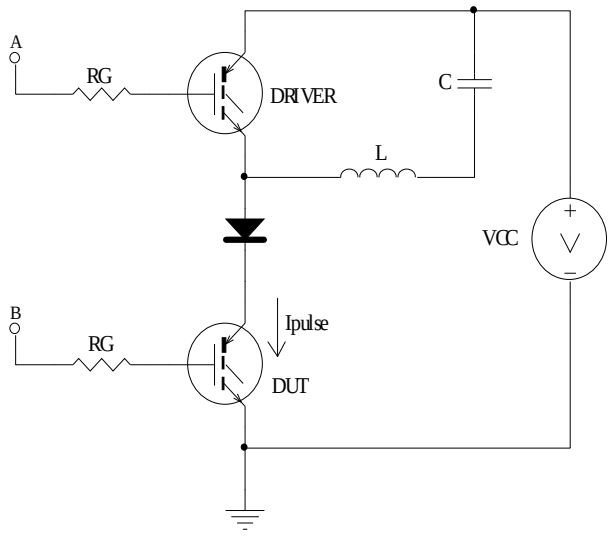


Fig 16a. t_{st} and E_{PULSE} Test Circuit

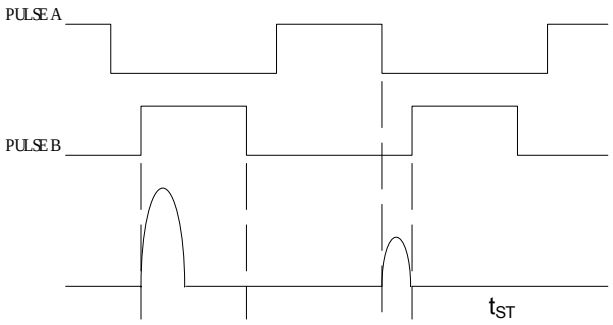


Fig 16b. t_{st} Test Waveforms

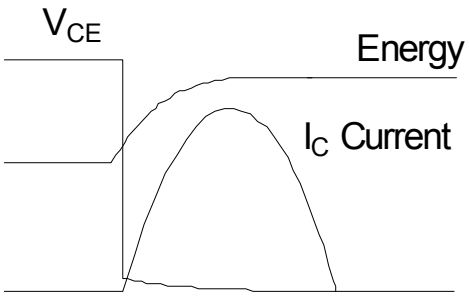


Fig 16c. E_{PULSE} Test Waveforms

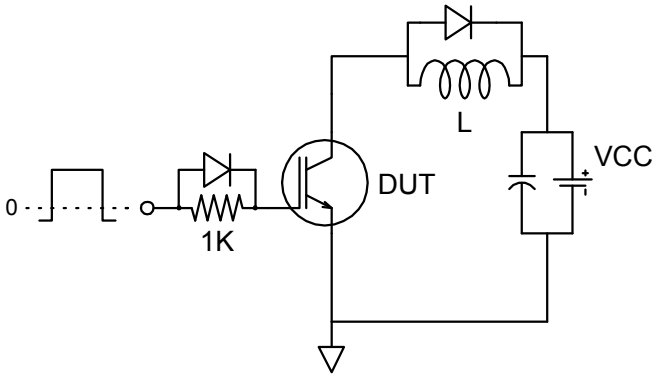
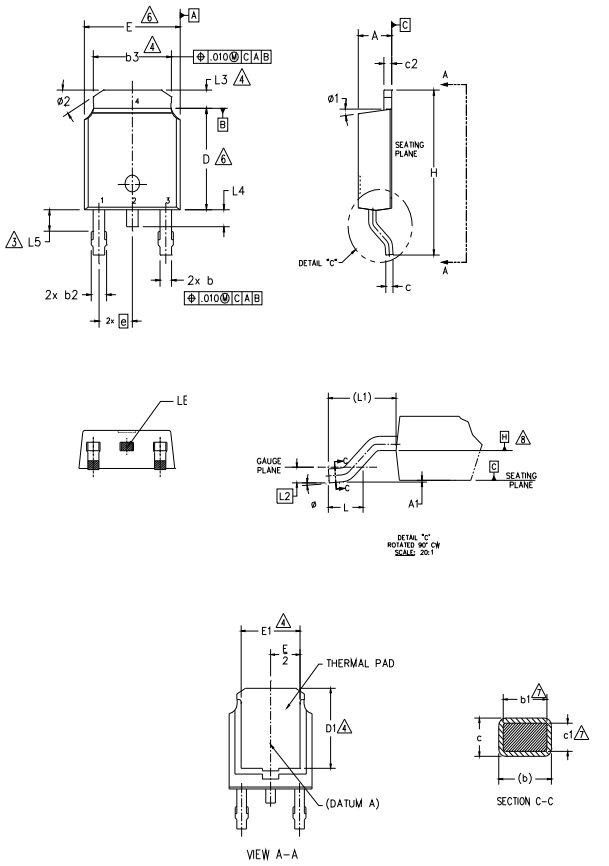


Fig 17. - Gate Charge Circuit (turn-off)

D-Pak (TO-252AA) Package Outline

Dimensions are shown in millimeters (inches)



NOTES:

1.– DIMENSIONING AND TOLERANCING PER ASME Y14.5M–1994

2.– DIMENSION ARE SHOWN IN INCHES [MILLIMETERS].

3.– LEAD DIMENSION UNCONTROLLED IN L5.

4.– DIMENSION D1, E1, L3 & b3 ESTABLISH A MINIMUM MOUNTING SURFACE FOR THERMAL PAD.

5.– SECTION C–C DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN .005 AND 0.10 [0.13 AND 0.25] FROM THE LEAD TIP.

6.– DIMENSION D & E DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED .005 [0.13] PER SIDE. THESE DIMENSIONS ARE MEASURED AT THE OUTMOST EXTREMES OF THE PLASTIC BODY.

7.– DIMENSION b1 & c1 APPLIED TO BASE METAL ONLY.

8.– DATUM A & B TO BE DETERMINED AT DATUM PLANE H.

9.– OUTLINE CONFORMS TO JEDEC OUTLINE TO–252AA.

SYMBOL	DIMENSIONS				NOTES
	MILLIMETERS		INCHES		
	MIN.	MAX.	MIN.	MAX.	
A	2.18	2.39	.086	.094	
A1	–	0.13	–	.005	
b	0.64	0.89	.025	.035	
b1	0.65	0.79	.025	.031	7
b2	0.76	1.14	.030	.045	
b3	4.95	5.46	.195	.215	4
c	0.46	0.61	.018	.024	
c1	0.41	0.56	.016	.022	7
c2	0.46	0.89	.018	.035	
D	5.97	6.22	.235	.245	6
D1	5.21	–	.205	–	4
E	6.35	6.73	.250	.265	6
E1	4.32	–	.170	–	4
e	2.29 BSC		.090 BSC		
H	9.40	10.41	.370	.410	
L	1.40	1.78	.055	.070	
L1	2.74 BSC		.108 REF.		
L2	0.51 BSC		.020 BSC		
L3	0.89	1.27	.035	.050	4
L4	–	1.02	–	.040	
L5	1.14	1.52	.045	.060	3
ø	0°	10°	0°	10°	
ø1	0°	15°	0°	15°	
ø2	25°	35°	25°	35°	

LEAD ASSIGNMENTS

HEXFET

1.– GATE
2.– DRAIN
3.– SOURCE
4.– DRAIN

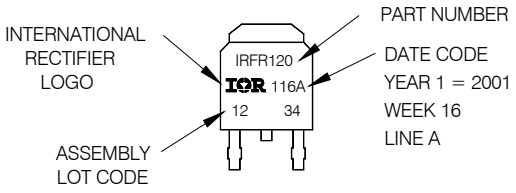
IGBT & CoPAK

1.– GATE
2.– COLLECTOR
3.– EMITTER
4.– COLLECTOR

D-Pak (TO-252AA) Part Marking Information

Notes: This part marking information applies to devices produced after 02/26/2001

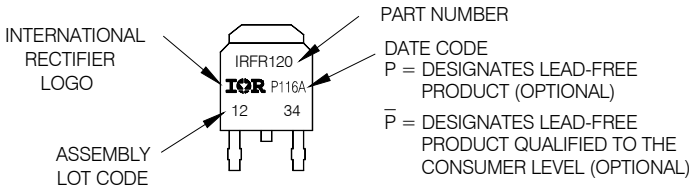
EXAMPLE: THIS IS AN IRFR120
WITH ASSEMBLY
LOT CODE 1234
ASSEMBLED ON WW 16, 2001
IN THE ASSEMBLY LINE "A"



Note: "P" in assembly line position indicates "Lead-Free"

"$\bar{P}$" in assembly line position indicates "Lead-Free" qualification to the consumer-level

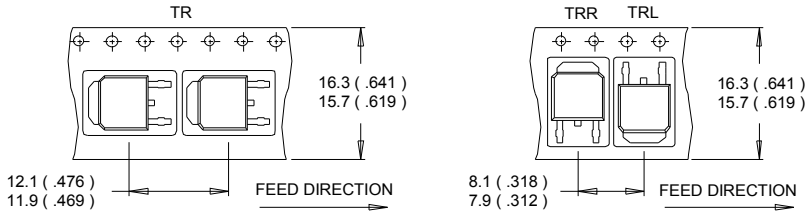
OR



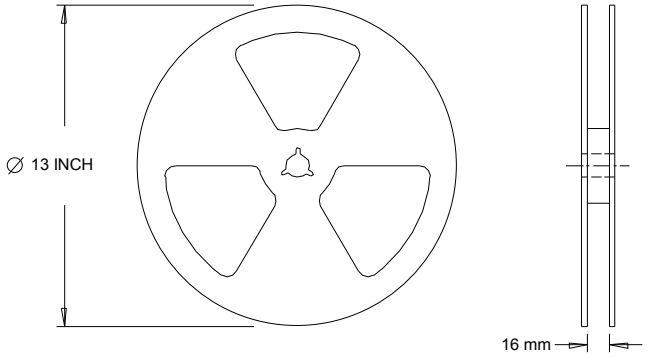
Note: For the most current drawing please refer to IR website at http://www.irf.com/package/

D-Pak (TO-252AA) Tape & Reel Information

Dimensions are shown in millimeters (inches)



NOTES :
1. CONTROLLING DIMENSION : MILLIMETER.
2. ALL DIMENSIONS ARE SHOWN IN MILLIMETERS (INCHES).
3. OUTLINE CONFORMS TO EIA-481 & EIA-541.



NOTES :
1. OUTLINE CONFORMS TO EIA-481.

Qualification information†

Qualification level	Industrial†† (per JEDEC JESD47F ††† guidelines)	
Moisture Sensitivity Level	D-Pak	MSL1 (per JEDEC J-STD-020D†††)
RoHS compliant	Yes	

† Qualification standards can be found at International Rectifier's web site: http://www.irf.com/product-info/reliability/

†† Higher qualification ratings may be available should the user have such requirements. Please contact your International Rectifier sales representative for further information: http:www.irf.com/whoto-call/salesrep/

††† Applicable version of JEDEC standard at the time of product release.

International
IOR Rectifier

IR WORLD HEADQUARTERS: 101 N. Sepulveda Blvd., El Segundo, California 90245
To contact International Rectifier, please visit http://www.irf.com/whoto-call/
Visit us at www.irf.com for sales contact information.

