PAS6180 CMOS QVGA DIGITAL IMAGE SENSOR

General Description

The PAS6180 is a highly integrated CMOS active-pixel image sensor that has output of 240 x 320 pixels. It embedded the new FinePixel™ sensor technology to perform the excellent image quality. PAS6180 outputs YUV/YCrCb 4:2:2 or RGB565/555/444 data through the serial data bus. It is available in CSP-16L package.

The PAS6180 can be programmed to set the exposure time for different luminance condition via I2C™ serial control bus. By programming the internal register set, it performs on-chip frame rate adjustment, offset correction DAC and programmable gain control.

Features

- **Resolution: 240 x 320 pixels, 1/13" Lens**
- **Bayer-RGB color filter array**
- **Output format:**
  - **YUV/YCrCb 4:2:2**
  - **RGB565/555/444**
- **I2C™ Interface**
- **Power dissipation: operating typical TBD @ 2.8V (QVGA YUV 30fps output, without loading), power-down typical TBD @ 2.8V**
- **Automatic Background Compensation**
- **DSP function:**
  - **AEC & AGC**
  - **AWB**
  - **Gamma**
  - **Color matrix**
  - **Sharpness**
  - **De-noise**
  - **Color saturation**
  - **Defect compensation**
  - **Lens shading compensation**
  - **Decimation and Scaler**
- **WOI & Sub-sampling**
- **Module size : 5.0mm * 5.0mm**

Key Specification

Resolution	240 (H) x 320 (V)
Pixel Size	3.15um * 3.15um
Array diagonal	1/13" Lens
Lens Chief Ray Angle	23 degree
Color filter	RGB Bayer Pattern
Power	2.8V typical
Input clock	52MHz
Output clock	52MHz
Max. Frame rate	30fps
Scan Mode	Progressive
Exposure Time	~ Frame time to Line time
Sensitivity	1500mV/Lux-Sec
S/N Ratio	41dB
Dynamic range	60dB
Package	CSP-16L

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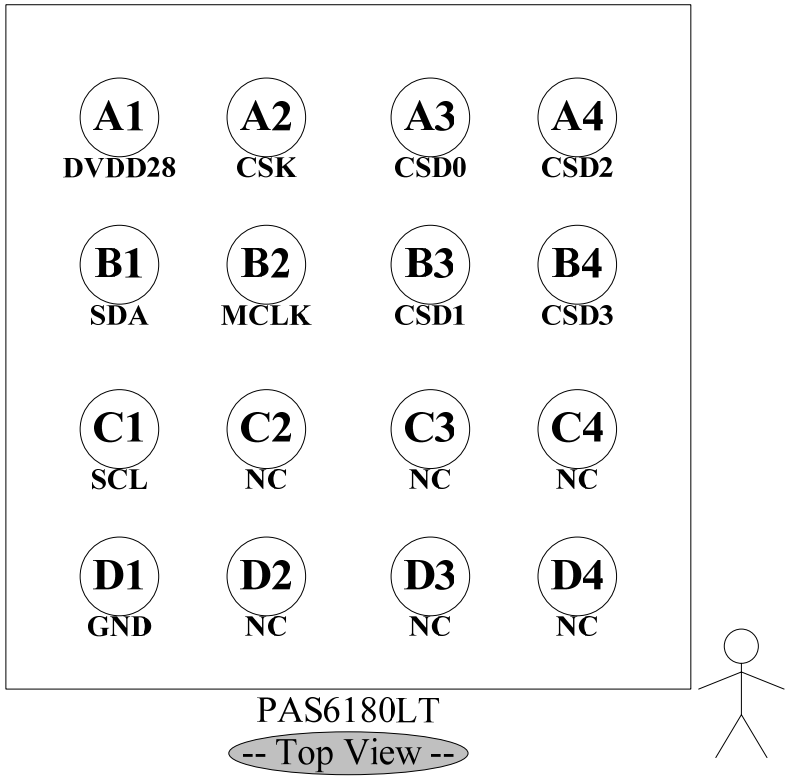
1. Pin Assignment



Pin No.	Name	Type	Description
A1	DVDD28	PWR	Main power, 2.8V typical,
A2	CSK	OUT	Pixel clock output,
A3	CSD0	OUT	Digital pixel data [0],
A4	CSD2	OUT	Digital pixel data [2], optional,
B1	SDA	I/O	I2C data,
B2	MCLK	IN	External clock input,
B3	CSD1	OUT	Digital pixel data [1], optional,
B4	CSD3	OUT	Digital pixel data [3], optional,
C1	SCL	IN	I2C clock input,
C2	NC	--	NC,
C3	NC	--	NC,
C4	NC	--	NC,
D1	GND	GND	Ground
D2	NC	--	NC,
D3	NC	--	NC,
D4	NC	--	NC,

2. Specifications

Absolute Maximum Ratings

Operating Temperature		-30˚C ~ 85˚C
Stable Image Temperature		0˚C ~ 50˚C
Ambient Storage Temperature		-40˚C ~ 125˚C
Supply Voltage (with respect to ground)	V_{DD}	4.5V
All Input / Output Voltage (with respect to ground)		-0.3V to V_{DD} + 0.5V
Lead-free temperature, Surface-mount process		245˚C
ESD rating, Human Body model		2000V

DC Electrical Characteristics (Ta = 0℃ ~ 70℃)

Symbol	Parameter	Min.	Typ.	Max.	Unit
Type : POWER					
V_{DD}	DC supply voltage – Main		2.8		V
I_{DD}	Operating Current (QVGA YUV 30fps / 2.8v)		12		mA
I_{PWDN}	Power Down Current (QVGA YUV 30fps / 2.8v)		10		μA
Type : IN & I/O					
V_{IH}	Input Voltage HIGH	V_{DD} * 0.7			V
V_{IL}	Input Voltage LOW			V_{DD} * 0.3	V
Type : OUT & I/O					
V_{OH}	Output Voltage HIGH	V_{DD} * 0.9			V
V_{OL}	Output Voltage LOW			V_{DD} * 0.1	V

AC Operating Condition

Symbol	Parameter	Min.	Typ.	Max.	Unit
f_{sysclk}	System clock frequency		52		MHz
t_{sysclk_dc}	System clock duty cycle	45		55	%

Sensor Characteristics

Parameter	Typ.	Unit
Sensitivity	1500	mV/Lux-Sec
Signal to Noise Ratio	41	dB
Dynamic Range	60	dB

3. I2C™ Bus

PAS6180 supports I2C bus transfer protocol and acts as slave device. The 7-bits unique slave address is "0111000" and supports receiving / transmitting speed as maximum 400KHz.

I2C Bus Overview

- Only two wires SDA (serial data) and SCL (serial clock) carry information between the devices connected to the I2C bus. Normally both SDA and SCL lines are open collector structure and pulled high by external pull-up resistors.
- Only the master can initiates a transfer (start), generates clock signals, and terminates a transfer (stop).
- Start and stop condition : A high to low transition of the SDA line while SCL is high defines a start condition. A low to high transition of the SDA line while SCL is high defines a stop condition. Please refer to Figure 2.1.
- Valid data : The data on the SDA line must be stable during the high period of the SCL clock. Within each byte, MSB is always transferred first. Read / Write control bit is the LSB of the first byte. Please refer to Figure 2.2.
- Both the master and slave can transmit and receive data from the bus.
- Acknowledge : The receiving device should pull down the SDA line during high period of the SCL clock line when a complete byte was transferred by transmitter. In the case of a master received data from a slave, the master does not generate an acknowledgment on the last byte to indicate the end of a master read cycle.

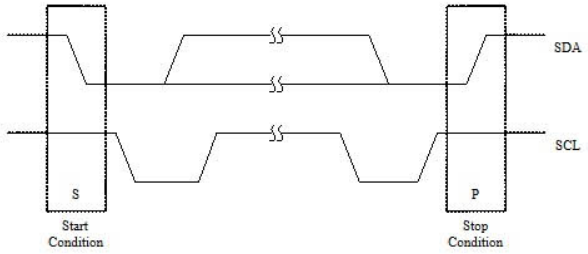


Figure 2.1 Start and Stop conditions

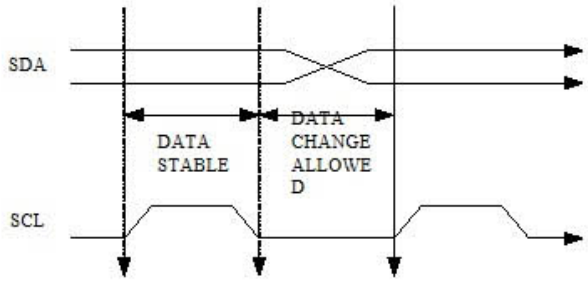
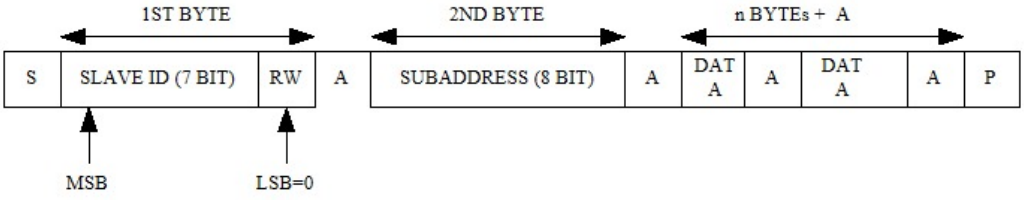


Figure 2.2 Valid Data

Data Transfer Format

Master transmits data to salve (write cycle)

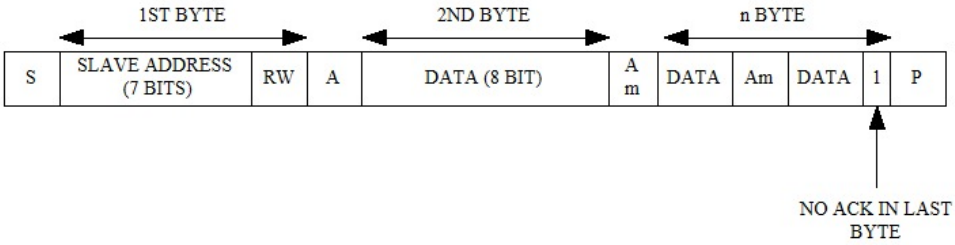
- S : Start.
- A : Acknowledge by salve.
- P : Stop.
- RW : The LSB of 1ST byte to decide whether current cycle is read or write cycle. RW = 1 – Read cycle, RW = 0 – Write cycle.
- SUBADDRESS : The address values of PAS6180 internal control registers. (Please refer to PAS6180 register description)



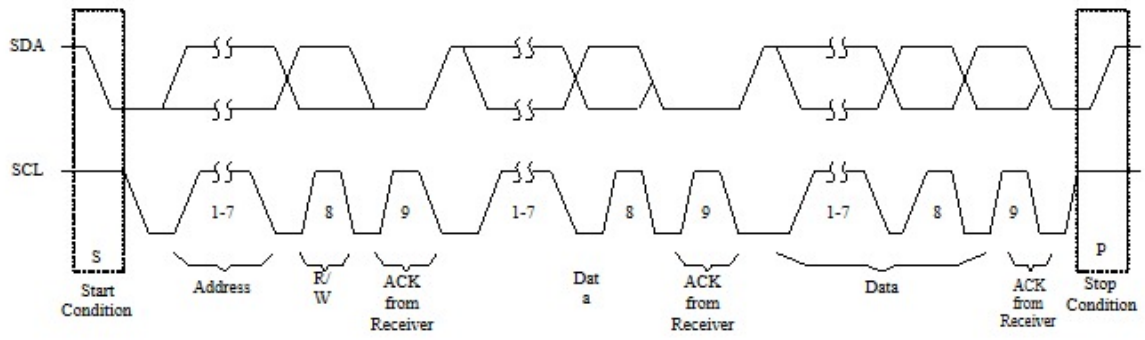
During write cycle, the master generates start condition and then places the 1st byte data that are combined slave address (7 bits) with a read / write control bit to SDA line. After slave (PAS6180) issues acknowledgment, the master places 2nd byte (Sub Address) data on SDA line. Again follow the PAS6180 acknowledgment, the master places the 8 bits data on SDA line and transmit to PAS6180 control register (address was assigned by 2nd byte). After PAS6180 issues acknowledgment, the master can generate a stop condition to end of this write cycle. In the condition of multi-byte write, the PAS6180 sub-address is automatically increment after each DATA byte transferred. The data and A cycles is repeat until last byte write. Every control registers value inside PAS6180 can be programming via this way.

Slave transmits data to master (read cycle)

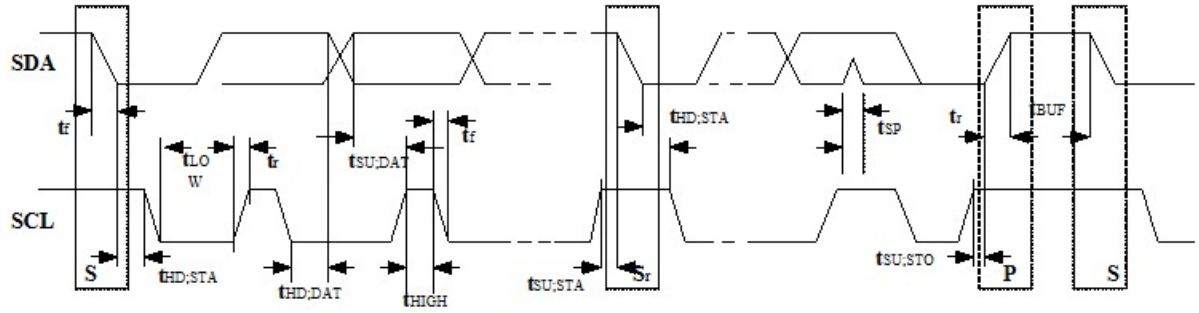
- The sub-address was taken from previous write cycle.
- The sub-address is automatically increment after each byte read.
- Am : Acknowledge by master.
- Note there is no acknowledgment from master after last byte read.



During read cycle, the master generates start condition and then place the 1st byte data that are combined slave address (7 bits) with a read / write control bit to SDA line. After issue acknowledgment, 8 bits DATA was also placed on SDA line by PAS6180. The 8 bits data was read from PAS6180 internal control register that address was assigned by previous write cycle. Follow the master acknowledgment, the PAS6180 place the next 8 bits data (address is increment automatically) on SDA line and then transmit to master serially. The DATA and Am cycles is repeat until the last byte read. After last byte read, Am is no longer generated by master but instead by keep SDA line high. The slave (PAS6180) must releases SDA line to master to generate STOP condition.



I2C™ Bus Timing



I2C™ Bus Timing Specification

Parameter	Symbol	Standard Mode		Unit
		Min.	Max	
SCL clock frequency.	f_{scl}	10	400	KHz
Hold time (repeated) Start condition. After this period, the first clock pulse is generated.	$t_{HD:STA}$	4.0	-	µs
Low period of the SCL clock.	t_{LOW}	4.7	-	µs
High period of the SCL clock.	t_{HIGH}	0.75	-	µs
Set-up time for a repeated START condition.	$t_{SU;STA}$	4.7	-	µs
Data hold time. For I2C-bus device.	$t_{HD;DAT}$	0	3.45	µs
Data set-up time.	$t_{SU;DAT}$	250	-	ns
Rise time of both SDA and SCL signals.	t_r	30	N.D.	ns (notel)
Fall time of both SDA and SCL signals.	t_f	30	N.D.	ns (notel)
Set-up time for STOP condition.	$t_{SU;STO}$	4.0	-	µs
Bus free time between a STOP and START.	t_{BUF}	4.7	-	µs
Capacitive load for each bus line.	C_b	1	15	pF
Noise margin at LOW level for each connected device. (Including hysteresis)	V_{nL}	0.1 VDD	-	V
Noise margin at HIGH level for each connected device. (including hysteresis)	V_{nH}	0.2 VDD	-	V

Note : It depends on the “high” period time of SCL.

4. Registers

Register Table

Bank	Address		Register Name	Bits	Default Value	Notes
	Hex	Dec				
0	0	0	PartID[15:8]	[7:0]	0x61	Part ID
0	1	1	PartID[7:0]	[7:0]	0x79	Part ID
0	2	2	VersionID[3:0]	[3:0]	0x00	VersionID
0	4	4	R_AE_stage_indoor_Sel	[0]	0x00	AE indoor stage select 0:11 , 1:12
0	F	15	R_AWB_Window_X[7:0]	[7:0]	0x90	AWB window width (by4)
0	11	17	R_AWB_Window_Y[7:0]	[7:0]	0x64	AWB window height (by4)
0	13	19	R_lpf_min[7:0]	[7:0]	0xf6	Lpf minimum value for AE
0	14	20	R_ny_min[3:0]	[7:4]	0x21	Ny minimum value for AE
0	14	20	R_lpf_min[10:8]	[2:0]		Lpf minimum value for AE
0	15	21	R_AE_Window_X[6:0]	[6:0]	0x80	AE window width (by4)
0	17	23	R_AE_Window_Y[6:0]	[6:0]	0x5f	AE window height (by4)
0	19	25	R_AWB_DGnR_LB_by2[7:0]	[7:0]	0x30	AWB digital gain lower bound for R
0	1A	26	R_AWB_DGnR_UB_by2[7:0]	[7:0]	0x49	AWB digital gain upper bound for B
0	1B	27	R_AWB_DGnB_LB_by2[7:0]	[7:0]	0x3a	AWB digital gain lower bound for B
0	1C	28	R_AWB_DGnB_UB_by2[7:0]	[7:0]	0x78	AWB digital gain upper bound for R
0	1F	31	R_DeNoiseEn	[4]	0x10	DeNoise Enable
0	29	41	R_ISP_Gamma_EnH	[0]	0x01	ISP gamma correction enable
0	2B	43	R_ISP_Y01	[7:0]	0x19	ISP Gamma Y1
0	2C	44	R_ISP_Y02	[7:0]	0x2f	ISP Gamma Y2
0	2D	45	R_ISP_Y03	[7:0]	0x53	ISP Gamma Y3
0	2E	46	R_ISP_Y04	[7:0]	0x62	ISP Gamma Y4
0	2F	47	R_ISP_Y05	[7:0]	0x6f	ISP Gamma Y5
0	30	48	R_ISP_Y06	[7:0]	0x7c	ISP Gamma Y6
0	31	49	R_ISP_Y07	[7:0]	0x87	ISP Gamma Y7
0	32	50	R_ISP_Y08	[7:0]	0x9a	ISP Gamma Y8
0	33	51	R_ISP_Y09	[7:0]	0xaa	ISP Gamma Y9
0	34	52	R_ISP_Y10	[7:0]	0xb8	ISP Gamma Y10
0	35	53	R_ISP_Y11	[7:0]	0xc5	ISP Gamma Y11
0	36	54	R_ISP_Y12	[7:0]	0xd8	ISP Gamma Y12
0	37	55	R_ISP_Y13	[7:0]	0xe8	ISP Gamma Y13
0	38	56	R_ISP_Y14	[7:0]	0xf5	ISP Gamma Y14
0	47	71	R_AWB_Speed	[1:0]	0x34	AWB adjust speed. The more, the slower 0: 1 x 1: 1/2 x 2: 1/4 x 3: 1/8 x
0	49	73	R_AWB_SumRatio_B	[7:0]	0x80	AWB B sum ratio = 128/X
0	4A	74	R_AWB_SumRatio_R	[7:0]	0x80	AWB R sum ratio = 128/X
0	4B	75	R_AWB_CThdL	[7:0]	0x37	AWB Chroma threshold low
0	4C	76	R_AWB_CThdH	[7:0]	0x0a	AWB Chroma threshold high
0	4D	77	R_AWB_CbThdL[7:0]	[7:0]	0x64	AWB region test Cb Low threshold -128 ~ +127 (2's complement)
0	4E	78	R_AWB_CrThdL[7:0]	[7:0]	0x87	AWB region test Cr Low threshold -128 ~ +127 (2's complement)
0	4F	79	R_AWB_CbCrThdL[7:0]	[7:0]	0x00	AWB region test Cb+Cr Low threshold

						-128 ~ +127 (2's complement)
0	50	80	R_AWB_CbThdH[7:0]	[7:0]	0x75	AWB region test Cb High threshold -128 ~ +127 (2's complement)
0	51	81	R_AWB_CrThdH[7:0]	[7:0]	0x96	AWB region test Cr High threshold -128 ~ +127 (2's complement)
0	52	82	R_AWB_CbCrThdH[7:0]	[7:0]	0xff	AWB region test Cb+Cr High threshold -128 ~ +127 (2's complement)
0	53	83	R_Ylow	[7:0]	0x1e	Low bound of "light-pixel"Y in AWB
0	54	84	R_Yhigh	[7:0]	0xff	High bound of "light-pixel"Y in AWB
0	57	87	R_AWB_LockRange__In[3:0]	[3:0]	0x02	AWB Lockrange In (NL)
0	58	88	R_AWB_LockRange_Out[5:0]	[5:0]	0x04	AWB Lockrange Out (NL)
0	5B	91	R_AWB_MinStep_th[2:0]	[2:0]	0x00	AWB mininum step size 0:1, 1:2, 2:4, 3:8, 4:16, 5:32, 6:64, 7:128
0	5F	95	R_AE_LockRange_Out_LB[7:0]	[7:0]	0x14	AE Lockrange Out LB
0	64	100	R_AE_LockRange_Out_UB[7:0]	[7:0]	0x14	AE Lockrange Out UB
0	65	101	R_AE_LockRange__In[3:0]	[7:4]	0x41	AE Lockrange In
0	66	102	R_AE_EnH	[4]	0x00	AE enable
0	66	102	R_freq_60	[0]	0x01	Set de-flicker frequency 0/1: 50/60Hz
0	67	103	R_SysClk_freq[7:0]	[7:0]	0x97	Input_frequency/256
0	68	104	R_SysClk_freq[14:8]	[6:0]	0x31	Input_frequency/256
0	6B	107	R_AE_minStage[4:0]	[4:0]	0x07	Minimum AE stage
0	6C	108	R_AE_maxStage[4:0]	[4:0]	0x1c	Maximum AE stage (AE_maxStage<=31) (ISP_UpdateFlag=1, update)
0	6D	109	R_AG_stage_UB	[7:0]	0x3f	AG_stage upper bound at max AE_stage (ISP_UpdateFlag=1, update)
0	6F	111	R_Ytar8bit	[7:0]	0x82	0~255, Target luminance of AE
0	72	114	R_AWB_EnH	[0]	0x00	Auto-white balance enable
0	72	114	R_AWB_Gain_rst	[4]	0x01	AWB gain gain reset
0	79	121	R_ISP_HOffset[4:0]	[4:0]	0x0E	ISP Hsize Offset
0	7B	123	R_ISP_VOffset[4:0]	[4:0]	0x04	ISP Vsize Offset
0	81	129	R_AE_Speed	[5:4]	0x00	AE speed, the more, the slower 0: 1 x 1: 1/2 x 2: 1/4 x 3: 1/8 x
0	8A	138	R_SenClk_Sel	[0]	0x00	Sensor Clk
0	8F	143	R_ImgEffect_c0	[7:0]	0x00	Image Effect parameter 0 (ISP_UpdateFlag=1, update)
0	90	144	R_ImgEffect_c1	[7:0]	0x00	Image Effect parameter 1 (ISP_UpdateFlag=1, update)
0	91	145	R_ImgEffect_c2	[7:0]	0x00	Image Effect parameter 2 (ISP_UpdateFlag=1, update)
0	93	147	R_ImgEffectMode	[3:0]	0x00	Image Effect mode 0: monochrome 1: negative 2: x-ray 3: Sepia/Cold/Warm/Sunset 6: Solarize 10: Pixelate (ISP_UpdateFlag=1, update)

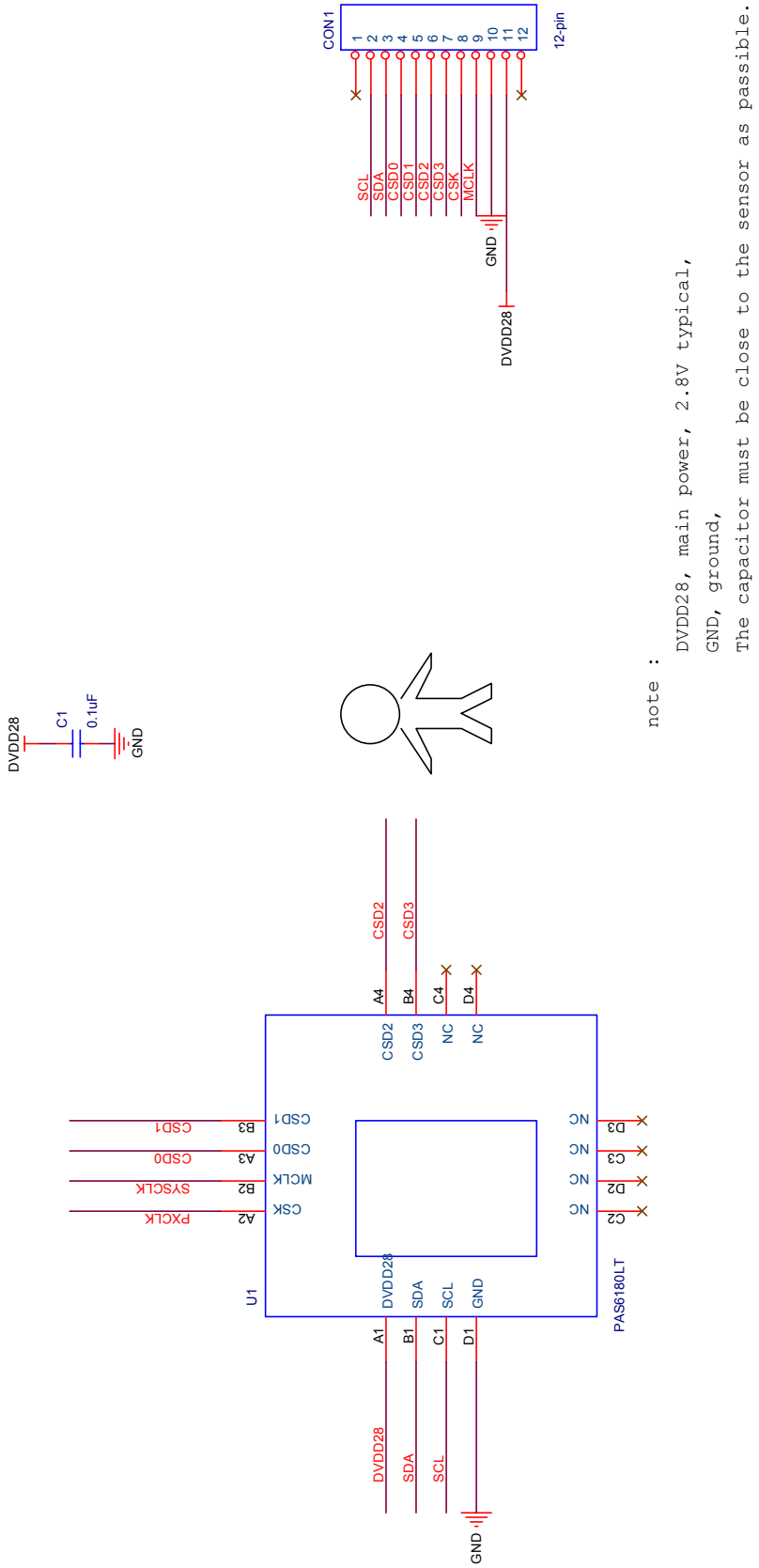
0	94	148	R_ISP_ImgEffect_En	[0]	0x00	(ISP_UpdateFlag=1, update)
0	97	151	R_Shading_EnH	[4]	0x01	Lens shading enable
0	98	152	R_VFLIP	[4]	0x00	Vertical flip
0	98	152	R_HFLIP	[5]	0x00	Horizontal flip
0	99	153	R_OffsetX_R[6:0]	[6:0]	0x00	Horizontal distances between shading center and sensor array center of R-channel, MSB:sign bit, -63~+63
0	9A	154	R_OffsetY_R[6:0]	[6:0]	0x00	Vertical distances between shading center and sensor array center of R-channel, MSB:sign bit, -63~+63
0	9B	155	R_OffsetX_G[6:0]	[6:0]	0x00	Horizontal distances between shading center and sensor array center of G-channel, MSB:sign bit, -63~+63
0	9C	156	R_OffsetY_G[6:0]	[6:0]	0x00	Vertical distances between shading center and sensor array center of G-channel, MSB:sign bit, -63~+63
0	9D	157	R_OffsetX_B[6:0]	[6:0]	0x00	Horizontal distances between shading center and sensor array center of B-channel, MSB:sign bit, -63~+63
0	9E	158	R_OffsetY_B[6:0]	[6:0]	0x00	Vertical distances between shading center and sensor array center of B-channel, MSB:sign bit, -63~+63
0	9F	159	R_LSC_R1[5:0]	[5:0]	0x00	Quartic parameter of R-channel
0	A0	160	R_LSC_G1[5:0]	[5:0]	0x00	Quartic parameter of G-channel
0	A1	161	R_LSC_B1[5:0]	[5:0]	0x00	Quartic parameter of B-channel
0	A2	162	R_LSC_R2[5:0]	[5:0]	0x38	Square parameter of R-channel
0	A3	163	R_LSC_G2[5:0]	[5:0]	0x38	Square parameter of G-channel
0	A4	164	R_LSC_B2[5:0]	[5:0]	0x38	Square parameter of B-channel
0	A5	165	R_LSFT_1[2:0]	[2:0]	0x05	Shading accuracy shift bit1
0	A6	166	R_LSFT_2[1:0]	[1:0]	0x00	Shading accuracy shift bit2
0	A7	167	R_LSFT_3[2:0]	[2:0]	0x02	Shading accuracy shift bit3
0	E0	224	R_ISP_HSize[7:0]	[7:0]	0x80	ISP output Horizontal size (before skip function)
0	E1	225	R_ISP_HSize[8]	[0]	0x02	ISP output Horizontal size (before skip function)
0	E2	226	R_ISP_VSize[7:0]	[7:0]	0xe0	ISP output Vertical size (before skip function)
0	E3	227	R_ISP_Vsize[8]	[0]	0x01	ISP output Vertical size (before skip function)
0	EB	235	R_SwTristate	[0]	0x00	Sw Tristate
0	EC	236	SW_CSB_suspend	[0]	0x00	1 : suspend
0	ED	237	ISP_Update	[0]	0x00	ISP_UpdateFlag
0	ED	237	ISP_FrameSkip	[4]	0x00	(ISP_UpdateFlag=1, update)
0	EF	239	R_RegBankSel	[2:0]	0x00	Register Bank Select 0: ISP1 Register Bank (default) 1: Sensor Register Bank 2: ISP2 Register Bank
2	0	0	ISP2_Update	[0]	0x00	ISP2_UpdateFlag

2	22	34	R_Defect_EnH	[3]	0x01	Defect Enable
2	26	38	R_DefectThd_NL[4:0]	[4:0]	0x0c	Defect Threshold @ normal light
2	27	39	R_DefectThd_LL[4:0]	[4:0]	0x0c	Defect Threshold @ low light
2	28	40	R_MTK_SPI_DataHeaderDelay [7:0]	[7:0]	0x1f	Cycle latency from previous data stream to next data header
2	2A	42	R_FlatRatio[3:0]	[3:0]	0x08	ISP edge enhancement flat ratio
2	2A	42	R_Flat_En	[6]	0x01	ISP edge enhancement flat enable
2	2A	42	R_ISP_Edge_En0	[7]	0x01	ISP edge enhancement enable
2	2C	44	R_Edge_UB[4:0]	[4:0]	0x20	ISP edge enhancement value upper bound
2	2D	45	R_Edge_LB[4:0]	[4:0]	0x19	ISP edge enhancement value lower bound
2	2F	47	R_AE_stage_LL[4:0]	[4:0]	0x13	AE_stage > R_AE_stage_LL => Low Light
2	30	48	R_AE_stage_NL[4:0]	[4:0]	0x11	AE_stage < R_AE_stage_NL => Normal Light
2	35	53	R_Gamma_Strength_NL[4:0]	[4:0]	0x10	Gamma strength @ normal light
2	37	55	R_Gamma_Strength_LL[4:0]	[4:0]	0x08	Gamma strength @ low light
2	38	56	R_AE_Middle_Stage[4:0]	[4:0]	0x0f	Apply Middle Gain when AE_stage >= R_AE_Middle_Stage
2	38	56	R_AE_Middle_Gain_En	[7]	0x01	AE Middle Gain Enable
2	39	57	R_AE_Middle_Gain[5:0]	[5:0]	0x10	AE Middle Gain code
2	3C	60	R_AG_FG_LB[5:0]	[5:0]	0x03	AE Front Gain Lowerbound
2	3E	62	R_CCMbSign[5:0]	[5:0]	0x33	CCM matrix coefficient
2	3F	63	R_CCMb0_0[6:0]	[6:0]	0x26	CCM matrix coefficient
2	40	64	R_CCMb0_1[6:0]	[6:0]	0x4b	CCM matrix coefficient
2	41	65	R_CCMb0_2[6:0]	[6:0]	0x0f	CCM matrix coefficient
2	42	66	R_CCMb1_0[6:0]	[6:0]	0x18	CCM matrix coefficient
2	43	67	R_CCMb1_1[6:0]	[6:0]	0x52	CCM matrix coefficient
2	44	68	R_CCMb1_2[6:0]	[6:0]	0x6a	CCM matrix coefficient
2	45	69	R_CCMb2_0[6:0]	[6:0]	0x6a	CCM matrix coefficient
2	46	70	R_CCMb2_1[6:0]	[6:0]	0x68	CCM matrix coefficient
2	47	71	R_CCMb2_2[6:0]	[6:0]	0x02	CCM matrix coefficient
2	48	72	R_AE_Middle_Gain2[2:0]	[7:5]	0x01	middle gain 2
2	48	72	R_AE_Middle_Stage2[4:0]	[4:0]	0x10	middle gain stage 2
2	49	73	R_AE_Middle_Gain3[2:0]	[7:5]	0x02	middle gain 3
2	49	73	R_AE_Middle_Stage3[4:0]	[4:0]	0x12	middle gain stage 3
2	57	87	R_EdgeRatio_LL[3:0]	[3:0]	0x04	Edge ratio @ Low Light
2	58	88	R_EdgeRatio_NL[3:0]	[3:0]	0x0a	Edge ratio @ Normal Light
2	5C	92	R_Edge_th_NL[4:0]	[4:0]	0x08	Edge threshold @ Normal Light
2	5F	95	R_Saturation_LL[4:0]	[4:0]	0x0b	Color Saturation @ Low Light
2	60	96	R_Saturation_NL[4:0]	[4:0]	0x16	Color Saturation @ Normal Light
2	63	99	R_Shading_CP__NL[3:0]	[3:0]	0x0f	Shading compensation percentage @ Normal Light
2	63	99	R_Shading_CP__LL[3:0]	[7:4]	0x00	Shading compensation percentage @ Low Light
2	64	100	R_Contrast_En	[0]	0x01	Contrast Enable
2	65	101	R_Contrast_Str[7:0]	[7:0]	0x40	Contrast Strength (ISP2_UpdateFlag=1, update)
2	66	102	R_Contrast_CP[7:0]	[7:0]	0x82	Contrast CP (ISP2_UpdateFlag=1, update)

2	67	103	R_MTK_SPI_OutEn	[0]	0x00	(ISP2_UpdateFlag=1, update)
2	69	105	R_Brightness_LL[7:0]	[7:0]	0x00	Brightness @ Low Light
2	6A	106	R_Brightness_NL[7:0]	[7:0]	0x00	Brightness @ Normal Light
2	6B	107	R_MTK_SPI_En	[0]	0x00	output data coded by mtk spi
2	6B	107	R_MTK_SPI_ClkInv	[2]	0x00	0=neg latch, 1=pos latch
2	6B	107	R_MTK_SPI_MSBfirst	[3]	0x00	Byte transmission from MSB
2	6B	107	R_MTK_SPI_DataParallelism [1:0]	[5:4]	0x00	0=1bit, 1=2bit
2	6C	108	R_MTK_SPI_SyncCode_Bit_ 07_00[7:0]	[7:0]	0xff	sync code; fix 0xff
2	6D	109	R_MTK_SPI_SyncCode_Bit_ 15_08[7:0]	[7:0]	0xff	sync code; fix 0xff
2	6E	110	R_MTK_SPI_SyncCode_Bit_ 23_16[7:0]	[7:0]	0xff	sync code; fix 0xff
2	6F	111	R_MTK_SPI_VSIZE[8]	[0]	0x01	image vsize to mtk spi
2	70	112	R_MTK_SPI_VSIZE[7:0]	[7:0]	0x40	image vsize to mtk spi
2	71	113	R_MTK_SPI_HSIZE[8]	[0]	0x00	image hsize to mtk spi
2	72	114	R_MTK_SPI_HSIZE[7:0]	[7:0]	0xf0	image hsize to mtk spi
2	73	115	R_MTK_SPI_Header_Delay [4:0]	[4:0]	0x04	Cycle Interval between any two header bytes
2	9B	155	R_ISP_WOI_HSize[8]	[0]	0x02	WOIa Hsize
2	9C	156	R_ISP_WOI_HSize[7:0]	[7:0]	0x80	WOIa Hsize
2	9D	157	R_ISP_WOI_VSize[8]	[0]	0x01	WOIa Vsize
2	9E	158	R_ISP_WOI_VSize[7:0]	[7:0]	0xe0	WOIa Vsize
2	9F	159	R_ISP_WOI_HOffset[8]	[0]	0x00	WOIa Hoffset
2	A0	160	R_ISP_WOI_HOffset[7:0]	[7:0]	0x00	WOIa Hoffset
2	A1	161	R_ISP_WOI_VOffset[8]	[0]	0x00	WOIa Voffset
2	A2	162	R_ISP_WOI_VOffset[7:0]	[7:0]	0x00	WOIa Voffset
2	A3	163	R_ScalingFIFO_En	[0]	0x01	(ISP2_UpdateFlag=1, update)
2	A4	164	R_ScalingFIFO_Out_NP[4:0]	[4:0]	0x02	(ISP2_UpdateFlag=1, update)
2	A5	165	R_Ptr_ScalingFIFO[8]	[0]	0x00	(ISP2_UpdateFlag=1, update)
2	A6	166	R_Ptr_ScalingFIFO[7:0]	[7:0]	0x02	(ISP2_UpdateFlag=1, update)
2	A8	168	R_FIFO_Hsync[8]	[0]	0x00	==(Hsize_sen+nov)*IN_NP*3/4 - Hsize_out*OUT_NP
2	A9	169	R_FIFO_Hsync[7:0]	[7:0]	0x20	==(Hsize_sen+nov)*IN_NP*3/4 - Hsize_out*OUT_NP
2	AA	170	R_FIFO_HSize[8]	[0]	0x02	FIFO output hsize (ISP2_UpdateFlag=1, update)
2	AB	171	R_FIFO_HSize[7:0]	[7:0]	0x80	FIFO output hsize (ISP2_UpdateFlag=1, update)
2	AD	173	R_DummyPix_End[4:0]	[4:0]	0x00	number of dummy pixel inserted in the end of line
2	AE	174	R_DummyPix_Front[4:0]	[4:0]	0x00	number of dummy pixel inserted in the front of line
2	B0	176	R_Scaler_X_En	[7]	0x00	Scaling Down X Enable (ISP2_UpdateFlag=1, update)
2	B0	176	R_ScaleDenr_X[5:0]	[5:0]	0x00	Scaling Down 16/x , 15<x<63 (ISP2_UpdateFlag=1, update)
2	B1	177	R_Scaler_Y_En	[7]	0x00	Scaling Down Y Enable (ISP2_UpdateFlag=1, update)
2	B1	177	R_ScaleDenr_Y[5:0]	[5:0]	0x00	Scaling Down 16/x , 15<x<63 (ISP2_UpdateFlag=1, update)
2	B2	178	R_EncDecimationNo_X[3:0]	[3:0]	0x00	ISP decimation no in X-direction (ISP_Zoom_UpdateFlag=1, update)
2	B2	178	R_EncDecimationNo_Y[3:0]	[7:4]	0x00	ISP decimation no in Y-direction (ISP_Zoom_UpdateFlag=1, update)
2	B4	180	R_ISP_WOIb_HSize[8]	[0]	0x02	WOIb Hsize
2	B5	181	R_ISP_WOIb_HSize[7:0]	[7:0]	0x80	WOIb Hsize

2	B6	182	R_ISP_WOIb_VSize[8]	[0]	0x01	WOIb Vsize
2	B7	183	R_ISP_WOIb_VSize[7:0]	[7:0]	0xe0	WOIb Vsize
2	B8	184	R_ISP_WOIb_HOffset[8]	[0]	0x00	WOIb Hoffset
2	B9	185	R_ISP_WOIb_HOffset[7:0]	[7:0]	0x00	WOIb Hoffset
2	BA	186	R_ISP_WOIb_VOffset[8]	[0]	0x00	WOIb Voffset
2	BB	187	R_ISP_WOIb_VOffset[7:0]	[7:0]	0x00	WOIb Voffset
2	BD	189	ISP_Out_En	[0]	0x01	1= ISP output enable
2	BD	189	R_ISP_Out_1frame	[1]	0x00	1= output 1 frame
2	BD	189	ISP_Out_1frame	[2]	0x00	Output 1 frame only if enable
2	BF	191	R_UV_Swap	[1]	0x00	U V Swap
2	BF	191	R_YC_Swap	[2]	0x01	Y C Swap
2	C0	192	R_RGB565_mode[3:0]	[3:0]	0x00	RGB565_mode
2	C0	192	R_Format_Sel	[5:4]	0x00	Output Data format select 0:YUV 1:RGB565 2:RGB555 3:RGB444 (ISP2_UpdateFlag=1, update)

5. Reference Circuit Schematic



6. Package Information

	Symbol	Nominal	Min.	Max.
		μm		
Package Body Dimension X	A	2004.6	1979.6	2029.6
Package Body Dimension Y	B	1997.8	1972.8	2022.8
Package Height	C	730	670	790
Ball Height	C1	110	80	140
Package Body Thickness	C2	620	575	665
Thickness of Glass surface to wafer	C3	445	425	465
Ball Diameter	D	230	200	260
Total Pin Count	N	16		
Pin Count X axis	N1	4		
Pin Count Y axis	N2	4		
Pins Pitch X axis	J1	430/480		
Pins Pitch Y axis	J2	430/480		
Edge to Pin Center Distance along X	S1	332.3	302	362
Edge to Pin Center Distance along Y	S2	328.9	299	359

∗ 1. The thickness of Bond-1 glass is 400 um (1pcs).

∗ 2. The material of solder ball is SAC305.

Mechanical Diagram

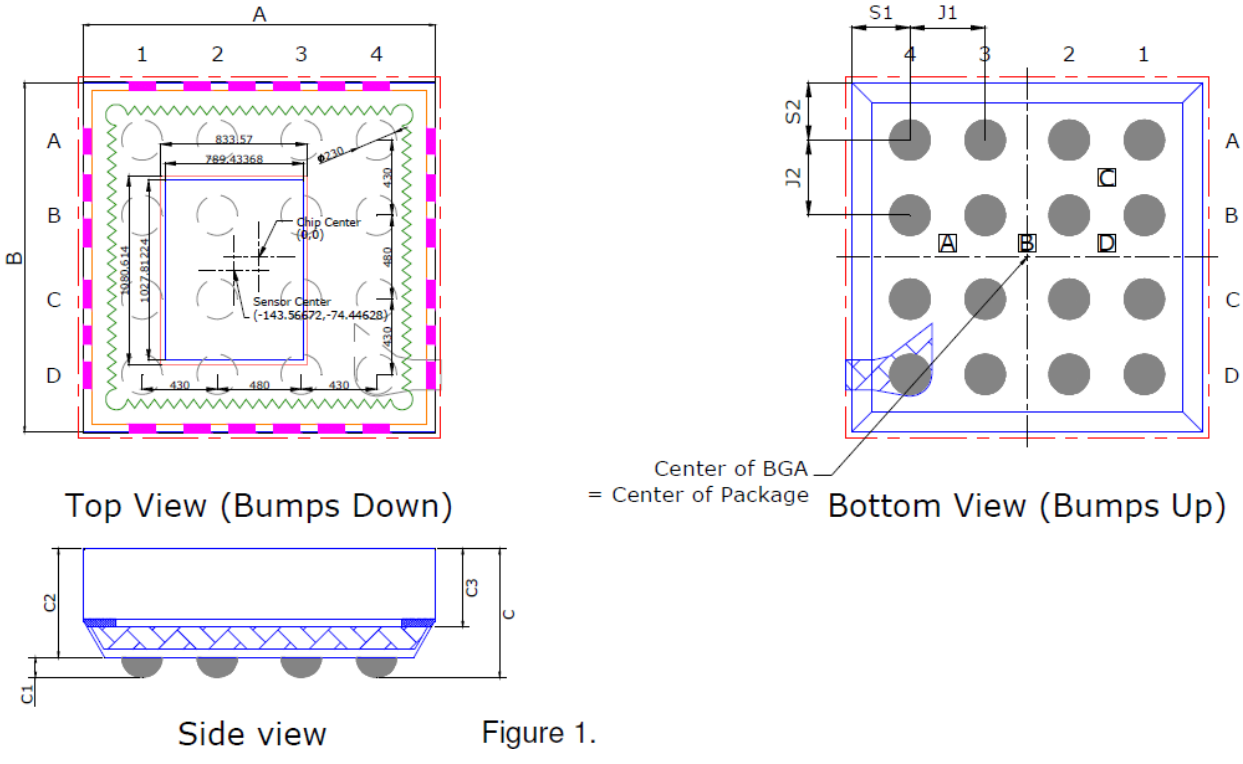
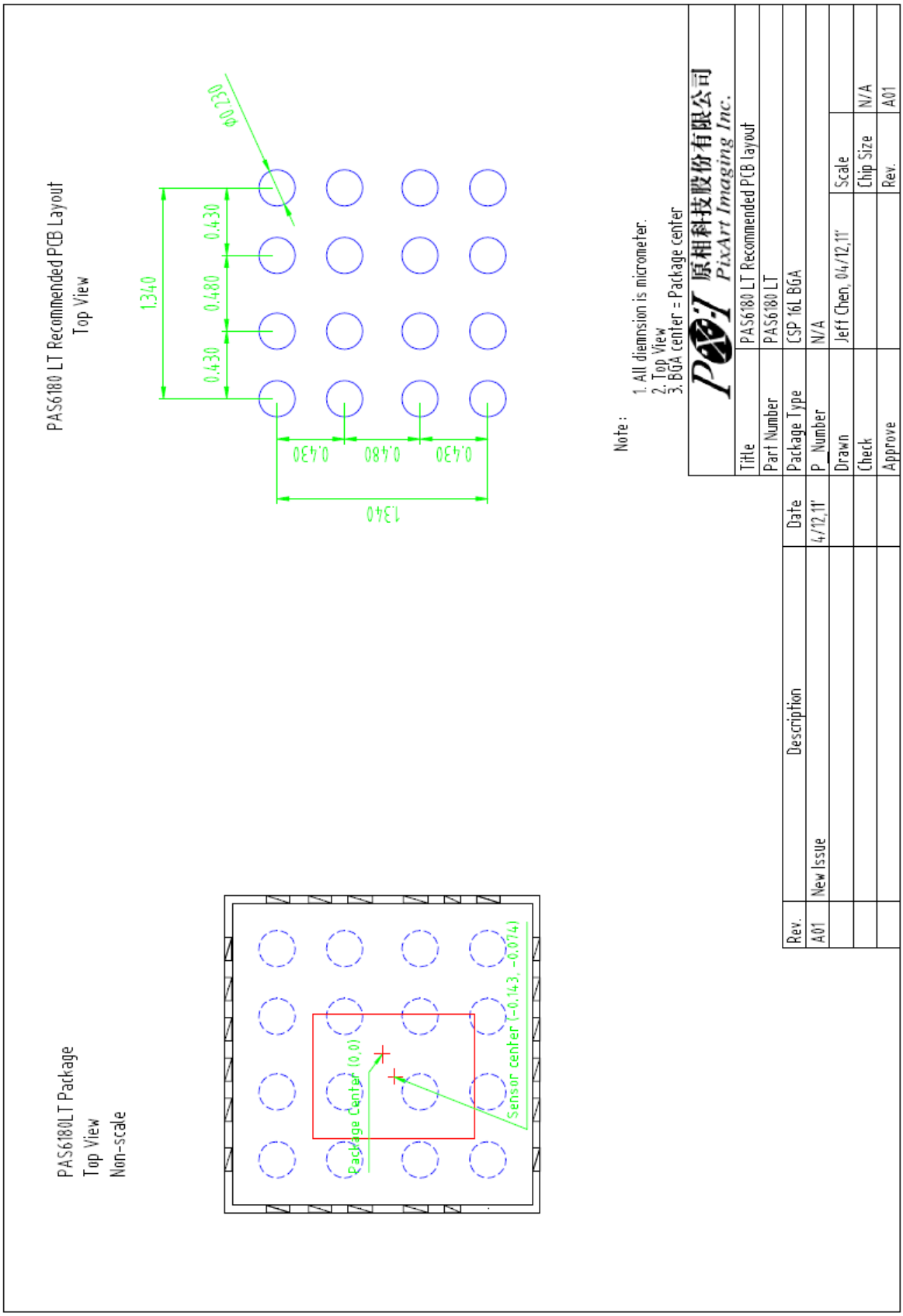


Figure 1.

*Note The formation of image is the result formed by package Top view(A1 : left-up) and general Lens(invert and mirror the image).

Recommended PCB Layout



Recommended Guideline for PCB Assembly

Recommended vender and type for Pb-free solder paste

1. Almit LFM-48W TM-HP
2. Senju M705-GRN360-K

IR Reflow Soldering Profile:

Temperature profile is the most important control in reflow soldering. It must be fine tuned to establish a robust process. The typical recommended IR reflow profile is showed in figure below.

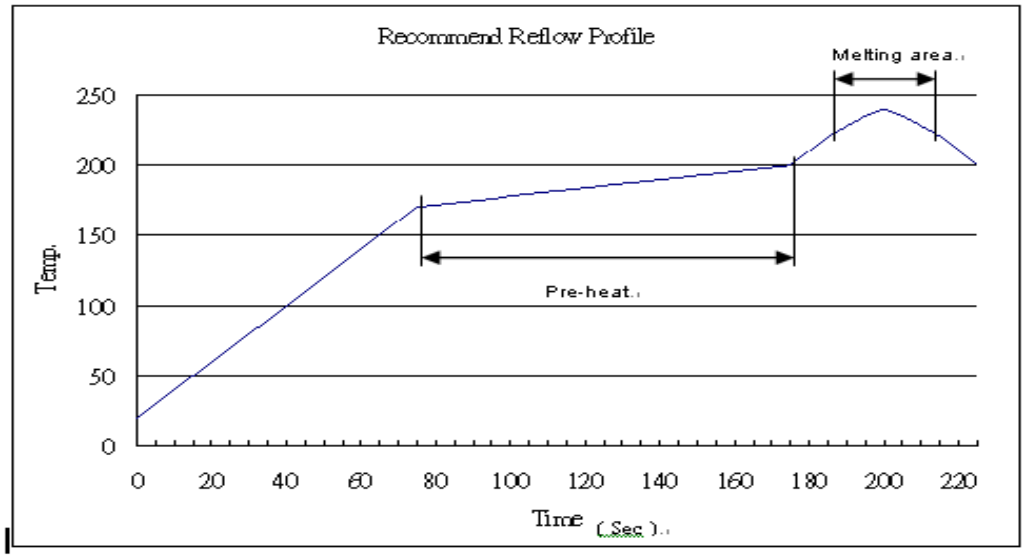


Fig. 8 IR Reflow Profile

Reflow Profile :

1. Average Ramp-up Rate (30°C to preheat zone): 1.5~ 2.5 Degree C/ Sec
2. Preheat zone:
   - 2.1 Temp ramp from 170~ 200 degree C
   - 2.2 Exposure time: 90 +/- 30 sec
3. Melting zone:
   - 3.1 Melting area temp > 220 degree C for at least 30 ~ 50 sec
   - 3.2 Peak temperature : 245 degree C.

Others:

Epoxy under-filled process is required post IC mounting process.

⊙ Dispense Epoxy

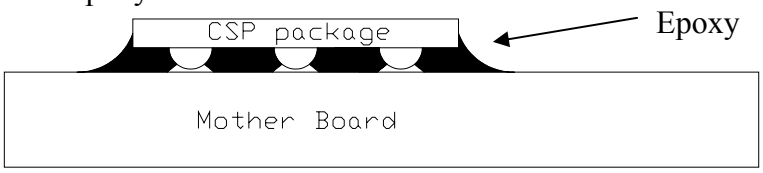


Fig. Epoxy Under-filled