CHA2001

6.4 - 8.6GHz LOW NOISE, GAIN CONTROL AMPLIFIER

GaAs MONOLITHIC MICROWAVE IC

FEATURES

- 3.3dB noise figure
- 20dB gain
- 24dB dynamic gain control
- Good input and output matching
- Available in chip form : CHA2001-99A/00 and T-PAK package :CHA2001-C1A/00
- Economic version : CHA2001-99A/01

APPLICATIONS

C-band radar and telecommunication receivers.

Automatic Gain control amplifiers

DESCRIPTION

The CHA2001 is a C-band monolithic three stage LNA including a dual gate MESFET as a control element. The gain can be varied continuously from +20 to -4dB by means of a control voltage V_C.

The circuit is manufactured with the LN05 standard process : 0,5µm implanted MESFET, via holes, air bridges and electron beam gate lithography.

Chip size 2 x 1 mm^2

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ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	MIN.	MAX.	UNIT
Drain to source voltage	V_{DS}		5	V
Drain current	I_{DS}		150	mA
Drain to gate voltage	V_{DG}		7	V
Gain control voltage	V_C	-2.5	+2.5	V
Input power (CW)	P_{in}		15	dBm
Operating temperature range	T_A	-40	+80	°C
Storage temperature range	T_{stg}	-55	+175	°C

ELECTRICAL CHARACTERISTICS (Tamb = + 25°C) (DIE FORM)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Operating frequency range	f_{op}		6.4		8.6	GHz
Small signal gain	G	(1) (2)	16	20 -4		dB
Gain flatness	ΔG	(1) (2)		± 1.5 ± 1.7	± 2.0 ± 2.5	dB
Noise figure CHA2001- 99A/00 99A/01	NF	(1)		 3.3 3.6	 3.5 3.8	dB
Output power at 1dB gain compression (3)	P_{01}	(1)		11		dBm
Gain Control range (3)	G_{CR}	(1,2)	19	24		dB
Input V.S.W.R.		(1,2)		2.2 : 1	2.5 : 1	
Output V.S.W.R.		(1,2)		1.4 : 1	2.0 : 1	
Reverse isolation		(1)	-42	-45		dB
Drain current	I_D	(1) (2)		60 45	80 60	mA
Drain to source voltage	V_{DS}			3	5	V
Gate to source voltage	V_{GS}		-2	-0.4	0	V
Gain control voltage	V_C	(1) (2)		+1.5 -1.2		V

(1) V_D = 3V V_G = -0.4V V_C = +1.5V for maximum gain
(2) V_D = 3V V_G = -0.4V V_C = -1.2V for maximum attenuation
(3) Measured on assembled die.

ELECTRICAL CHARACTERISTICS (Tamb = + 25°C) (T-PAK® FORM)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Operating frequency range	f_{op}		6.4		8.6	GHz
Small signal gain	G	(1) (2)	15	19 -4		dB
Gain flatness	ΔG	(1) (2)		± 1.5 ± 1.7	± 2.0 ± 2.5	dB
Noise figure CHA2001- 99A/00 99A/01	NF	(1)		 3.7 4	 3.9 4.2	dB
Output power at 1dB gain compression	P_{01}	(1)	9	11		dBm
Gain Control range	G_{CR}	(1,2)	19	24		dB
Input V.S.W.R.		(1,2)		1.8 : 1	2.2 : 1	
Output V.S.W.R.		(1,2)		2.2 : 1	2.5 : 1	
Reverse isolation		(1)	25	30		dB
Drain current	I_D	(1) (2)		60 45	80 60	mA
Drain to source voltage	V_{DS}			3	5	V
Gate to source voltage	V_{GS}		-2	-0.4	0	V
Gain control voltage	V_C	(1) (2)		+1.5 -1.2		V

(1) V_D = 3V V_G = -0.4V V_C = +1.5V for maximum gain
(2) V_D = 3V V_G = -0.4V V_C = -1.2V for maximum attenuation

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HANDLING AND BONDING PROCEDURES

◆ STORAGE

It is recommended that GaAs MMICs be stored in a dry nitrogen environment until die attached. Since Gallium Arsenide is a more brittle material than Silicon, special care must be taken when removing the chip from the carrier.

◆ DIE ATTACH

Stage temperature = 300°C (Minimize temperature and time whenever possible).
Preforms : Au/Sn (80/20)
Handling : grounded equipment and personnel.
Atmosphere : Dry nitrogen or forming gas flow over a clean die attach stage is recommended.

◆ BONDING

Thermal compression bonding is recommended using very pure gold wire of 25µm in diameter. The bonder should be properly grounded.

◆ PRECAUTIONS

Permanent damage to the device can result from inadequate protection against excessive voltages on the device due to static charge build up, test equipment transients and inductive pick up. Grounding of equipment and personnel during the handling and testing of GaAs MMICs and control of the device test conditions and environment should be standard procedures.

◆ DICE BONDING PAD LAYOUT
TO READ ATTENTIVELY

The ground pads must be connected to ground very close to the chip.

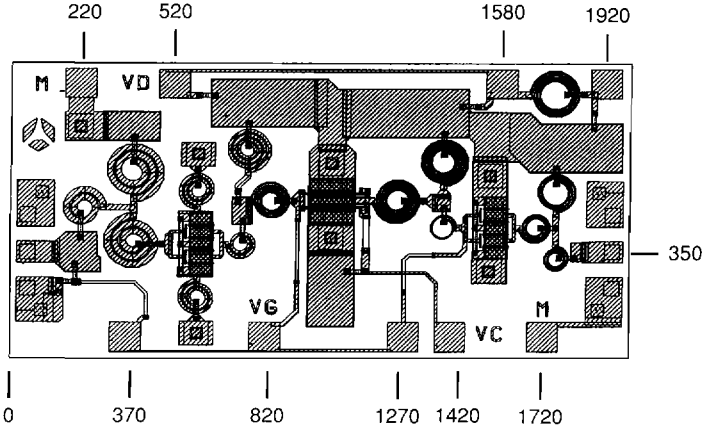
PIN ALLOCATIONS

1- RF input
2- Drain supply voltage
3- RF output
4- Gate supply voltage

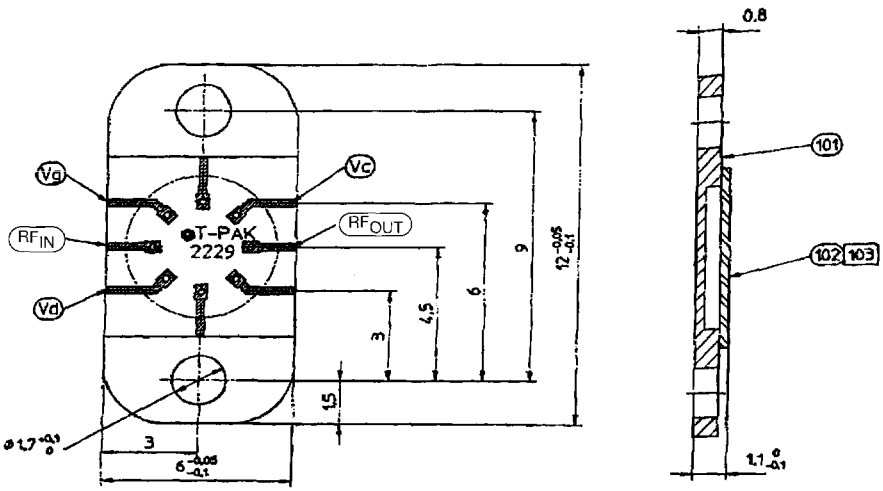
ORDERING INFORMATIONS

CHA2001-99A/00 Chip form
CHA2001-C1E/00 T-PAK® TPS1

CHIP LAYOUT



T-PAK® PACKAGE DRAWING



General tolerances = - 0.05

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