54F/74F675

16-Bit Serial-In, Serial/Parallel-Out Shift Register

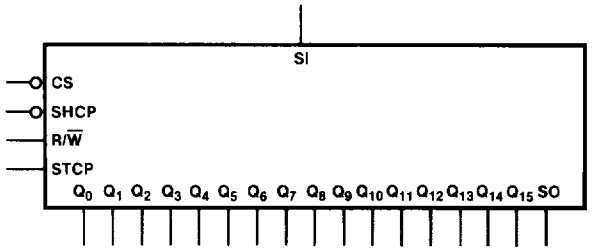
Description

The 'F675 contains a 16-bit serial-in, serial-out shift register and a 16-bit parallel-out storage register. Separate serial input and output pins are provided for expansion to longer words. By means of a separate clock, the contents of the shift register are transferred to the storage register. The contents of the storage register can also be loaded back into the shift register. A HIGH signal on the Chip Select input prevents both shifting and parallel loading.

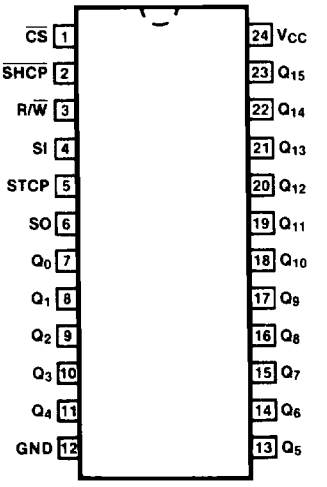
- **Serial-to-Parallel Converter**
- **16-Bit Serial I/O Shift Registerd**
- **16-Bit Parallel-Out Storage Register**
- **Recirculating Parallel Transfer**
- **Expandable for Longer Words**

Ordering Code: See Section 5

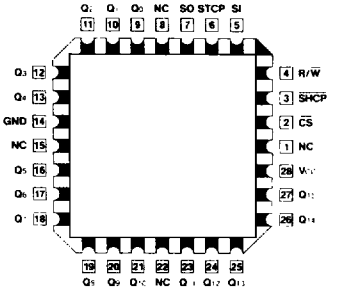
Logic Symbol



Connection Diagrams



Pin Assignment for DIP and SOIC



Pin Assignment for LCC and PCC

Input Loading/Fan-Out: See Section 3 for U.L. definitions

Pin Names	Description	54F/74F(U.L.) HIGH/LOW
SI	Serial Data Input	0.5/0.375
$\overline{CS}$	Chip Select Input (Active LOW)	0.5/0.375
$\overline{SHCP}$	Shift Clock Pulse Input (Active Falling Edge)	0.5/0.375
STCP	Store Clock Pulse Input (Active Rising Edge)	0.5/0.375
R/$\overline{W}$	Read/Write Input	0.5/0.375
SO	Serial Data Output	25/12.5
Q_0-Q_{15}	Parallel Data Outputs	25/12.5

Functional Description

The 16-bit shift register operates in one of four modes, as determined by the signals applied to the Chip Select ($\overline{CS}$), Read/Write (R/$\overline{W}$) and Store Clock Pulse (STCP) input. State changes are indicated by the falling edge of the Shift Clock Pulse ($\overline{SHCP}$). In the Shift Right mode, data enters D_0 from the Serial Input (SI) pin and exits from Q_{15} via the Serial Data Output (SO) pin. In the Parallel Load mode, data from the storage register outputs enter the shift register and serial shifting is inhibited.

The storage register is in the Hold mode when either $\overline{CS}$ or R/$\overline{W}$ is HIGH. With $\overline{CS}$ and R/$\overline{W}$ both LOW, the storage register is parallel loaded from the shift register on the rising edge of STCP.

To prevent false clocking of the shift register, $\overline{SHCP}$ should be in the LOW state during a LOW-to-HIGH transition of $\overline{CS}$. To prevent false clocking of the storage register, STCP should be LOW during a HIGH-to-LOW transition of $\overline{CS}$ if R/$\overline{W}$ is LOW, and should also be LOW during a HIGH-to-LOW transition of R/$\overline{W}$ if $\overline{CS}$ is LOW.

Shift Register Operations Table

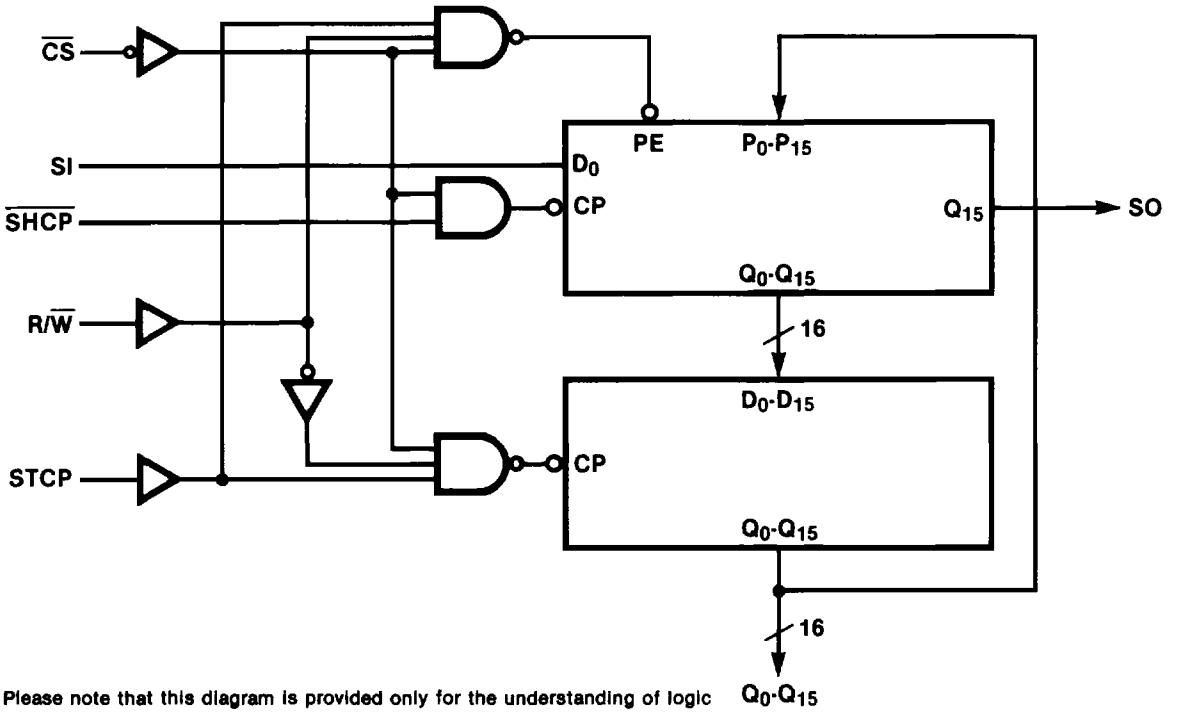
Control Inputs				Operating Mode
$\overline{CS}$	R/$\overline{W}$	$\overline{SHCP}$	STCP	
H	X	X	X	Hold
L	L	↓	X	Shift Right
L	H	↓	L	Shift Right
L	H	↓	H	Parallel Load; No Shifting

Storage Register Operations Table

Inputs			Operating Mode
$\overline{CS}$	R/$\overline{W}$	STCP	
H	X	X	Hold
L	H	X	Hold
L	L	↑	Parallel Load

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
↑ = LOW-to-HIGH Transition
↓ = HIGH-to-LOW Transition

Block Diagram



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

DC Characteristics over Operating Temperature Range (unless otherwise specified)

Symbol	Parameter	54F/74F			Units	Conditions
		Min	Typ	Max		
I_{CC}	Power Supply Current		106	160	mA	V_{CC} = Max

AC Characteristics: See Section 3 for waveforms and load configurations

Symbol	Parameter	54F/74F			54F		74F		Units	Fig. No.
		T_A = +25°C, V_{CC} = +5.0 V, C_L = 50 pF			T_A, V_{CC} = Mil, C_L = 50 pF		T_A, V_{CC} = Com, C_L = 50 pF			
		Min	Typ	Max	Min	Max	Min	Max		
f_{max}	Maximum Clock Frequency	100	130				80		MHz	3-1
t_{PLH}	Propagation Delay	6.5	11.0	14.0			6.5	15.0	ns	3-1
t_{PHL}	STCP to Q_n	6.5	11.0	14.0			6.5	15.0		3-7
t_{PLH}	Propagation Delay	5.5	9.0	11.5			5.5	12.5	ns	3-1
t_{PHL}	$\overline{SHCP}$ to SO	5.5	9.0	11.5			5.5	12.5		3-8

AC Operating Requirements: See Section 3 for waveforms

Symbol	Parameter	54F/74F	54F	74F	Units	Fig. No.
		$T_A = +25°C$ $V_{CC} = +5.0\ V$	T_A, V_{CC} = Mil	T_A, V_{CC} = Com		
		Min Typ Max	Min Max	Min Max		
$t_s(H)$	Setup Time, HIGH $\overline{CS}$ or R/$\overline{W}$ to STCP	0		0	ns	3-5
$t_h(L)$	Hold Time, LOW $\overline{CS}$ or R/$\overline{W}$ to STCP	7.0		7.0		
$t_s(H)$ $t_s(L)$	Setup Time, HIGH or LOW SI to $\overline{SHCP}$	3.0 3.0		3.0 3.0	ns	3-6
$t_h(H)$ $t_h(L)$	Hold Time, HIGH or LOW SI to $\overline{SHCP}$	3.0 3.0		3.0 3.0		
$t_s(H)$ $t_s(L)$	Setup Time, HIGH or LOW R/$\overline{W}$ to $\overline{SHCP}$	10.0 10.0		10.0 10.0	ns	3-6
$t_h(H)$ $t_h(L)$	Hold Time, HIGH or LOW R/$\overline{W}$ to $\overline{SHCP}$	0 0		0 0		
$t_s(H)$ $t_s(L)$	Setup Time, HIGH or LOW STCP to $\overline{SHCP}$	10.0 10.0		10.0 10.0	ns	3-6
$t_h(H)$ $t_h(L)$	Hold Time, HIGH or LOW STCP to $\overline{SHCP}$	0 0		0 0		
$t_s(L)$	Setup Time, LOW $\overline{CS}$ to $\overline{SHCP}$	7.0		7.0	ns	3-6
$t_h(H)$	Hold Time, HIGH $\overline{CS}$ to $\overline{SHCP}$	0		0		
$t_w(H)$ $t_w(L)$	$\overline{SHCP}$ Pulse Width, HIGH or LOW	5.0 5.0		6.0 6.0	ns	3-8
$t_w(H)$ $t_w(L)$	STCP Pulse Width, HIGH or LOW	6.0 5.0		7.0 6.0	ns	3-8