PROCESS CP714V

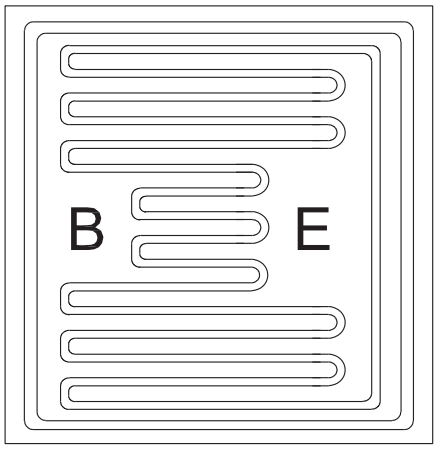
Small Signal Transistor

PNP - High Current Transistor Chip

PROCESS DETAILS

Process	EPITAXIAL PLANAR
Die Size	40 x 40 MILS
Die Thickness	7.0 MILS
Base Bonding Pad Area	7.9 x 8.7 MILS
Emitter Bonding Pad Area	9.0 x 14 MILS
Top Side Metalization	Al - 30,000Å
Back Side Metalization	Au - 18,000Å

GEOMETRY



BACKSIDE COLLECTOR R1

GROSS DIE PER 5 INCH WAFER

10,583

PRINCIPAL DEVICE TYPES

CBCP69
CBCX69
CZT751
MPS750
MPS751

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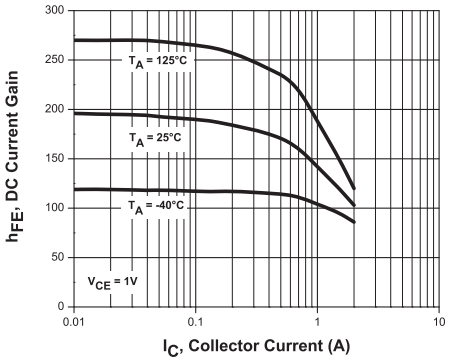
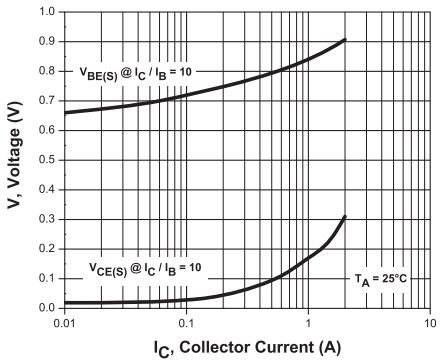
PROCESS CP714V

Typical Electrical Characteristics

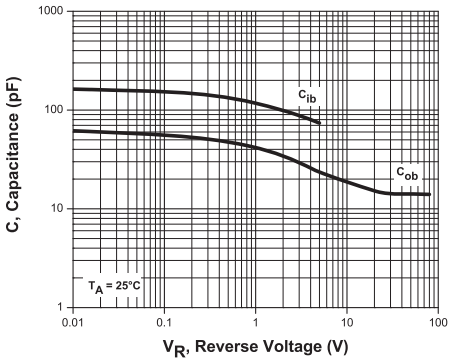
DC Current Gain



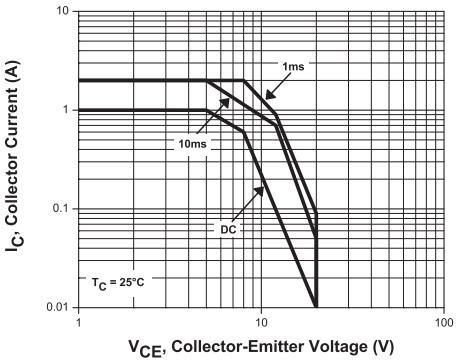
"ON" Voltage



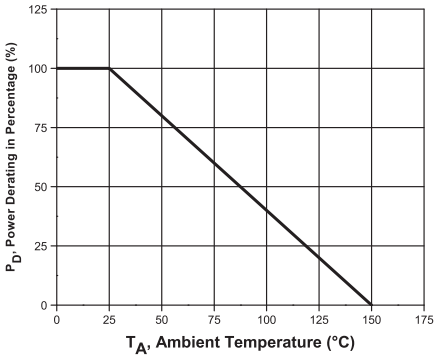
Capacitance



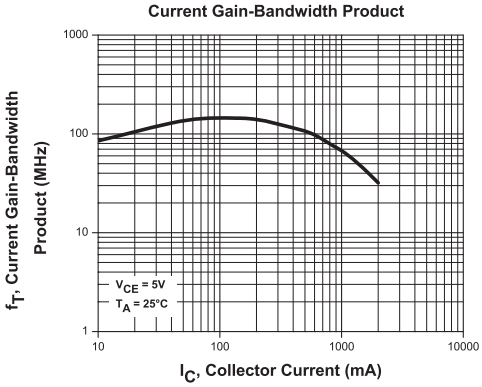
Safe Operating Area



Normalized Power Derating



Current Gain-Bandwidth Product



R0 (17-November 2010)