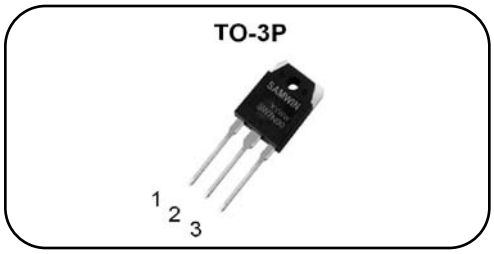
N-channel MOSFET

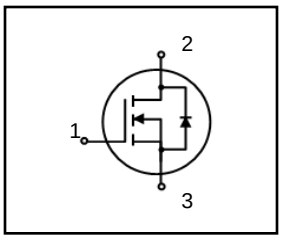
Features

- High ruggedness
- $R_{DS(ON)}$ (Max 1.8 **Ω**)@V_{GS}=10V
- Gate Charge (Typical 50nC)
- Improved dv/dt Capability
- 100% Avalanche Tested



1. Gate 2. Drain 3. Source

BV_{DSS} : 900V
I_D : 7.0A
$R_{DS(ON)}$: 1.8ohm



General Description

This power MOSFET is produced with advanced VDMOS technology of SAMWIN.
This technology enable power MOSFET to have better characteristics,
such as fast switching time, low on resistance, low gate charge and especially excellent avalanche characteristics. This power MOSFET is usually used at high efficient DC to DC converter block and switch mode power supply.

Order Codes

Item	Sales Type	Marking	Package	Packaging
1	SW W 7N90	SW7N90	TO-3P	TUBE

Absolute maximum ratings

Symbol	Parameter		Value	Unit
V_{DSS}	Drain to Source Voltage		900	V
I_D	Continuous Drain Current (@T_C=25ºC)		7.0*	A
	Continuous Drain Current (@T_C=100ºC)		4.4*	A
I_{DM}	Drain current pulsed	(note 1)	28	A
V_{GS}	Gate to Source Voltage		±30	V
E_{AS}	Single pulsed Avalanche Energy	(note 2)	580	mJ
E_{AR}	Repetitive Avalanche Energy	(note 1)	72	mJ
dv/dt	Peak diode Recovery dv/dt	(note 3)	2	V/ns
P_D	Total power dissipation (@T_C=25ºC)		390	W
	Derating Factor above 25ºC		3.1	W/ºC
T_{STG}, T_J	Operating Junction Temperature & Storage Temperature		-55 ~ + 150	ºC
T_L	Maximum Lead Temperature for soldering purpose, 1/8 from Case for 5 seconds.		300	ºC

*. Drain current is limited by junction temperature.

Thermal characteristics

Symbol	Parameter	Value	Unit
R_{thjc}	Thermal resistance, Junction to case	0.32	ºC/W
R_{thcs}	Thermal resistance, Case to Sink	0.5	ºC/W
R_{thja}	Thermal resistance, Junction to ambient	50	ºC/W

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Electrical characteristic (T_C = 25ºC unless otherwise specified)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
Off characteristics						
BV_{DSS}	Drain to source breakdown voltage	V_{GS}=0V, I_D=250uA	900	-	-	V
ΔBV_{DSS} / ΔT_J	Breakdown voltage temperature coefficient	I_D=250uA, referenced to 25ºC	-	0.85	-	V/ºC
I_{DSS}	Drain to source leakage current	V_{DS}=900V, V_{GS}=0V	-	-	10	uA
		V_{DS}=720V, T_C=125ºC	-	-	100	uA
I_{GSS}	Gate to source leakage current, forward	V_{GS}=30V, V_{DS}=0V	-	-	100	nA
	Gate to source leakage current, reverse	V_{GS}=-30V, V_{DS}=0V	-	-	-100	nA
On characteristics						
$V_{GS(TH)}$	Gate threshold voltage	V_{DS}=V_{GS}, I_D=250uA	3.0	-	5.0	V
$R_{DS(ON)}$	Drain to source on state resistance	V_{GS}=10V, I_D = 3.5A	-	1.1	1.8	Ω
Gfs	Forward Transconductance	VDS = 40 V, ID = 3.5A	2	-	-	S
Dynamic characteristics						
C_{iss}	Input capacitance	V_{GS}=0V, V_{DS}=25V, f=1MHz	-	1440	1880	pF
C_{oss}	Output capacitance		-	140	185	
C_{rss}	Reverse transfer capacitance		-	17	23	
$t_{d(on)}$	Turn on delay time	V_{DS}=450V, I_D=7A, R_G=25Ω (note 4、5)	-	33	80	ns
tr	Rising time		-	35	100	
$t_{d(off)}$	Turn off delay time		-	130	200	
t_f	Fall time		-	38	100	
Q_g	Total gate charge	VDS=720V, VGS=10V,ID=7A (note 4、5)	-	50	80	nC
Q_{gs}	Gate-source charge		-	11	-	
Q_{gd}	Gate-drain charge		-	23	-	

Source to drain diode ratings characteristics

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_S	Continuous source current	Integral reverse p-n Junction diode in the MOSFET	-	-	7	A
I_{SM}	Pulsed source current		-	-	25.6	A
V_{SD}	Diode forward voltage drop.	I_S=7A, V_{GS}=0V	-	-	1.5	V
T_{rr}	Reverse recovery time	I_S=7A, V_{GS}=0V, dI_F/dt=100A/us	-	400	-	ns
Q_{rr}	Breakdown voltage charge		-	3.8	-	uC

※. Notes
1. Repeatitive rating : pulse width limited by junction temperature.
2. L = 23.6mH, I_{AS} = 7A, V_{DD} = 50V, R_G=25Ω, Starting T_J = 25ºC
3. I_{SD} ≤ 7A, di/dt = 100A/us, V_{DD} ≤ BV_{DSS}, Staring T_J =25ºC
4. Pulse Test : Pulse Width≤ 300us, duty cycle ≤ 2%
5. Essentially independent of operating temperature.

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Fig. 1. On-state characteristics

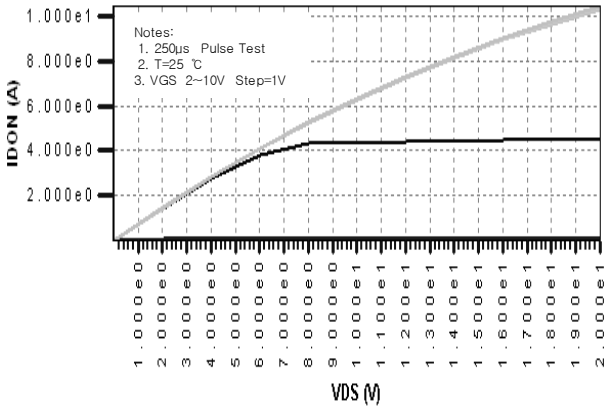

Fig. 2. On-resistance variation vs. drain current and gate voltage

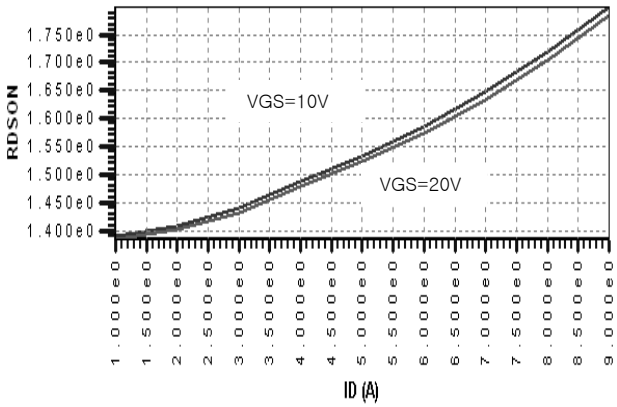

Fig. 3. Gate charge characteristics

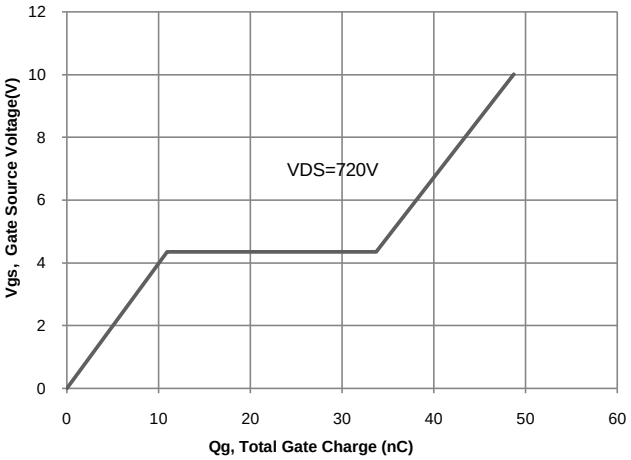

Fig. 4. On state current vs. diode forward voltage

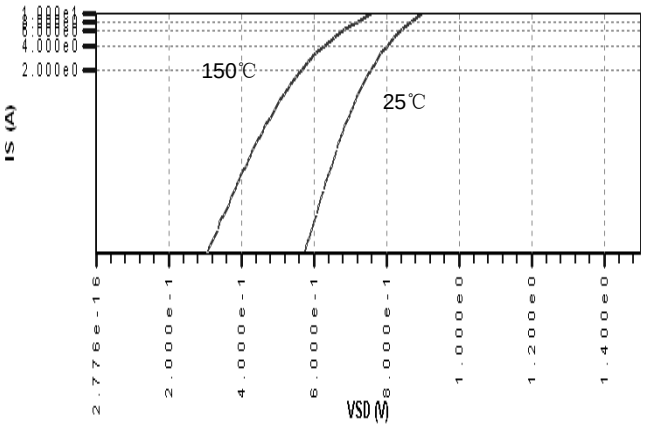

Fig 5. Breakdown Voltage Variation vs. Junction Temperature

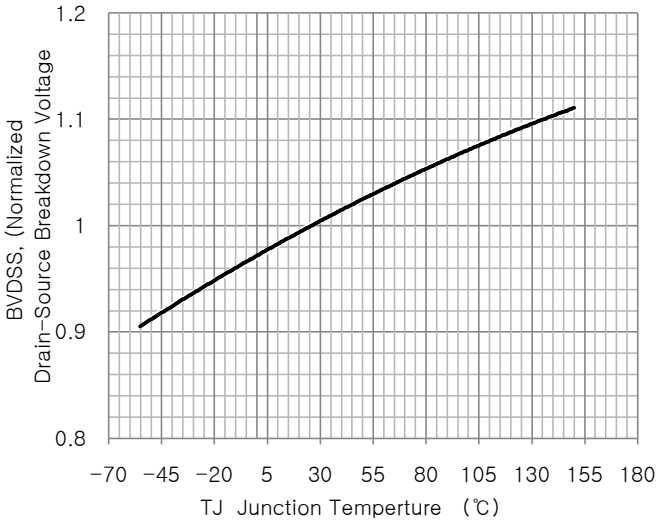

Fig. 6. On resistance variation vs. junction temperature

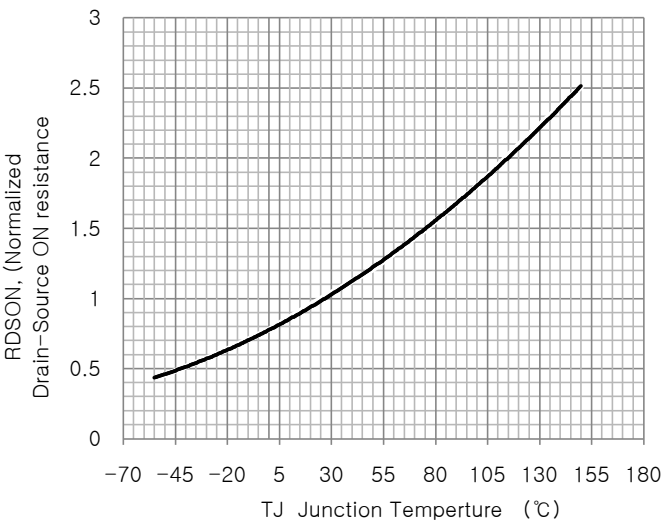

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Fig. 7. Maximum safe operating area

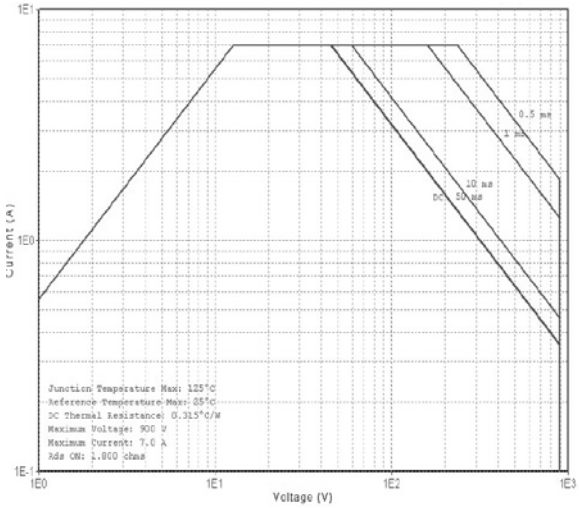

Fig. 8. Transient thermal response curve

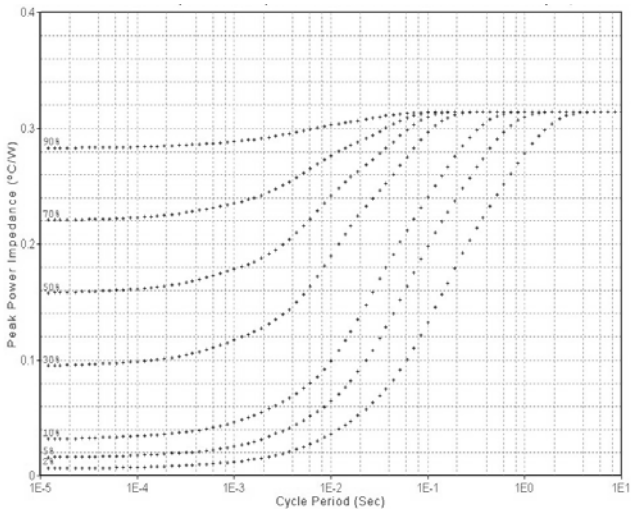

Fig. 9. Gate charge test circuit & waveform

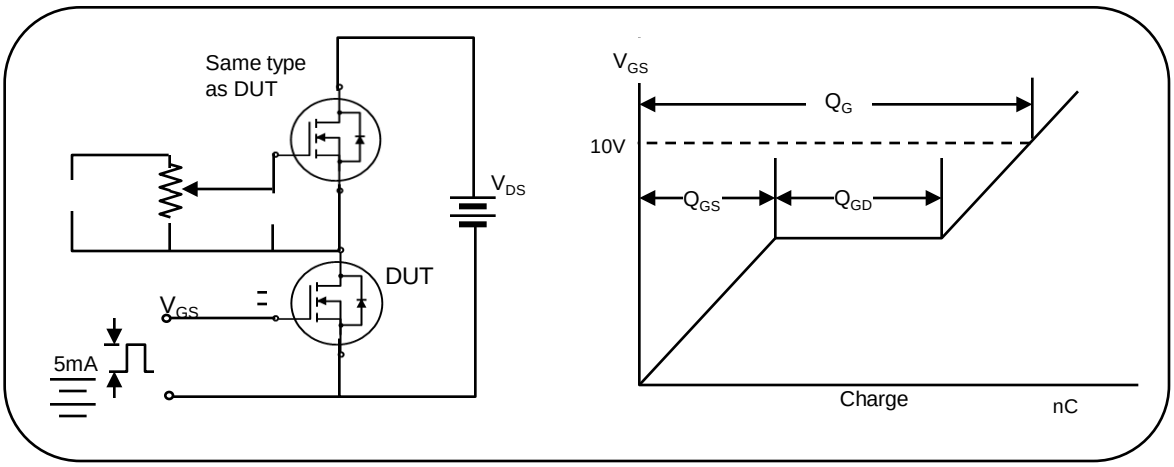

Fig. 10. Switching time test circuit & waveform

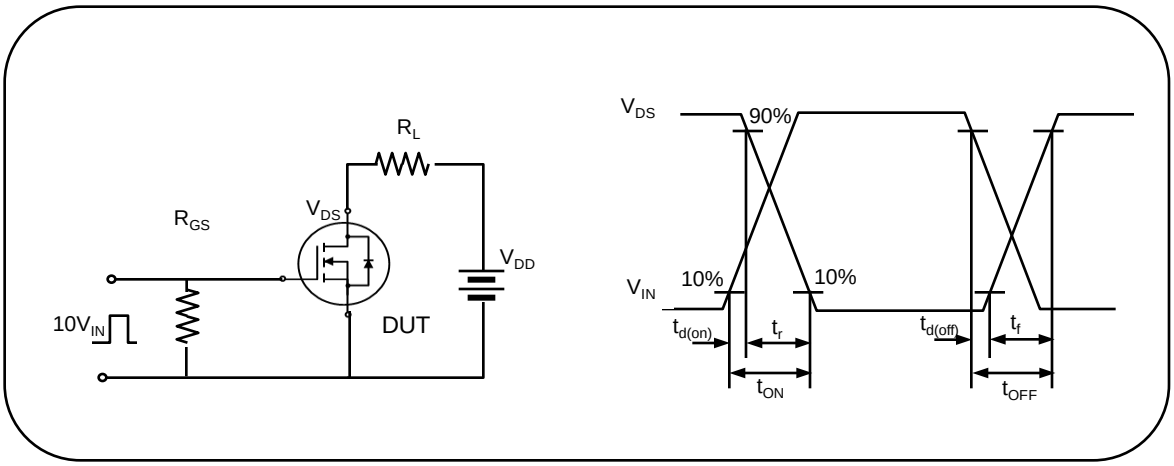

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Fig. 11. Unclamped Inductive switching test circuit & waveform

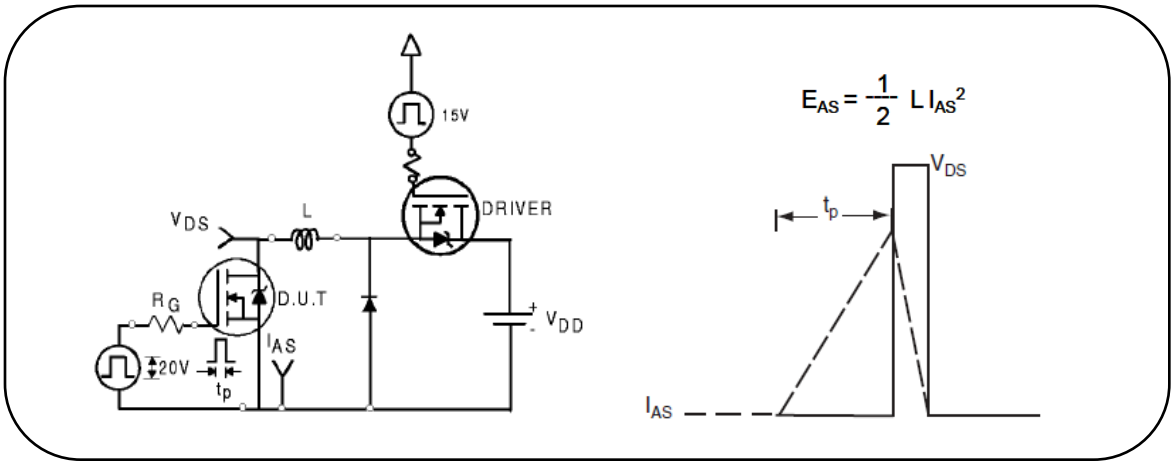

Fig. 12. Peak diode recovery dv/dt test circuit & waveform