Siliconix incorporated

SMP60N06/05, SMP50N06/05

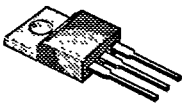
N-Channel Enhancement Mode Transistors

T-39-13

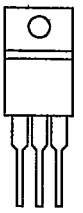
PRODUCT SUMMARY

PART NUMBER	$V_{(BR)DSS}$ (V)	$r_{DS(ON)}$ (Ω)	I_D (A)
SMP60N06	60	0.023	60
SMP60N05	50	0.023	60
SMP50N06	60	0.028	50
SMP50N05	50	0.028	50

TO-220AB



TOP VIEW



1 GATE
2 DRAIN (Connected to TAB)
3 SOURCE

1 2 3

ABSOLUTE MAXIMUM RATINGS (T_C = 25°C Unless Otherwise Noted)

PARAMETERS/TEST CONDITIONS		SYMBOL	SMP 60N06	SMP 60N05	SMP 50N06	SMP 50N05	UNITS
Gate-Source Voltage		V_{GS}	±20	±20	±20	±20	V
Continuous Drain Current	T_C = 25°C	I_D	60	60	50	50	A
	T_C = 100°C		38	38	31	31	
Pulsed Drain Current[1]		I_{DM}	240	240	200	200	
Avalanche Current (See Figure 9)		I_{AR}	60	60	50	50	
Avalanche Energy	L = 0.05 mH	E_A	90	90	62	62	mJ
Repetitive Avalanche Energy[2]	L = 0.01 mH	E_{AR}	18	18	18	18	
Power Dissipation	T_C = 25°C	P_D	125	125	125	125	W
	T_C = 100°C		50	50	50	50	
Operating Junction & Storage Temperature Range		T_J, T_{stg}	−55 to 150				°C
Lead Temperature ($^1/_{16}$" from case for 10 sec.)		T_L	300				

THERMAL RESISTANCE RATINGS

THERMAL RESISTANCE	SYMBOL	TYPICAL	MAXIMUM	UNITS
Junction-to-Case	R_{thJC}		1.0	K/W
Junction-to-Ambient	R_{thJA}		80	
Case-to-Sink	R_{thCS}	1.0		

[1]Pulse width limited by maximum junction temperature (refer to transient thermal impedance data, Figure 11.
[2]Duty cycle ≤ 1%.

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SMP60N06/05, SMP50N06/05

Siliconix incorporated

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ELECTRICAL CHARACTERISTICS (T_J = 25°C Unless Otherwise Noted)

PARAMETER		SYMBOL	TEST CONDITIONS	TYP	LIMITS MIN	LIMITS MAX	UNIT
STATIC							
Drain-Source Breakdown Voltage	SMP60N06, 50N06 SMP60N05, 50N05	$V_{(BR)DSS}$	V_{GS} = 0 V, I_D = 250 µA	65 55	60 50		V
Gate Threshold Voltage		$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 250 µA		2.0	4.0	
Gate-Body Leakage		I_{GSS}	V_{DS} = 0 V, V_{GS} = ±20 V	10		±100	nA
Zero Gate Voltage Drain Current		I_{DSS}	V_{DS} = $V_{(BR)DSS}$, V_{GS} = 0 V			250	µA
			V_{DS} = 0.8 x $V_{(BR)DSS}$, V_{GS} = 0 V, T_J = 125°C			1000	
On-State Drain Current[1]	SMP60N06, 60N05 SMP50N06, 50N05	$I_{D(ON)}$	V_{DS} = 25 V, V_{GS} = 10 V		60 50		A
Drain-Source On-State Resistance[1]	SMP60N06, 60N05 SMP50N06, 50N05	$r_{DS(ON)}$	V_{GS} = 10 V, I_D = 30 A	0.019 0.023		0.023 0.028	Ω
	SMP60N06, 60N05 SMP50N06, 50N05		V_{GS} = 10 V, I_D = 30 A T_J = 125°C	0.025 0.030		0.030 0.036	
Forward Transconductance[1]		g_{fs}	V_{DS} = 25 V, I_D = 30 A	18	15		S
DYNAMIC							
Input Capacitance		C_{iss}	V_{GS} = 0 V, V_{DS} = 25 V, f = 1 MHz	2900			pF
Output Capacitance		C_{oss}		1500			
Reverse Transfer Capacitance		C_{rss}		500			
Total Gate Charge[2]		Q_g	V_{DS} = 0.5 x $V_{(BR)DSS}$, V_{GS} = 10 V, I_D = 60 A	70		100	nC
Gate-Source Charge[2]		Q_{gs}		22		35	
Gate-Drain Charge[2]		Q_{gd}		35		50	
Turn-On Delay Time[2]		$t_{d(on)}$	V_{DD} = 30 V, R_L = 1 Ω I_D ≃ 130 A, V_{GEN} = 10 V, R_G = 2.5 Ω	20		40	ns
Rise Time[2]		t_r		25		50	
Turn-Off Delay Time[2]		$t_{d(off)}$		30		60	
Fall Time[2]		t_f		20		40	
SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS (T_C = 25°C)							
Continuous Current	SMP60N06, 60N05 SMP50N06, 50N05	I_S				60 50	A
Pulsed Current[3]		I_{SM}				190	
Forward Voltage[1]	SMP60N06, 60N05 SMP50N06, 50N05	V_{SD}	I_F = I_S, V_{GS} = 0 V			2.5 2.4	V
Reverse Recovery Time		t_{rr}	I_F = I_S, dI_F/dt = 100 A/µs	75		100	ns
Reverse Recovery Charge		Q_{rr}		0.19			µC

[1]Pulse test: Pulse Width ≤ 300 µsec, Duty Cycle ≤ 2%.
[2]Independent of operating temperature.
[3]Pulse width limited by maximum junction temperature (refer to transient thermal impedance data, Figure 11).

TYPICAL CHARACTERISTICS (25°C Unless Otherwise Specified)

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Figure 1. Output Characteristics

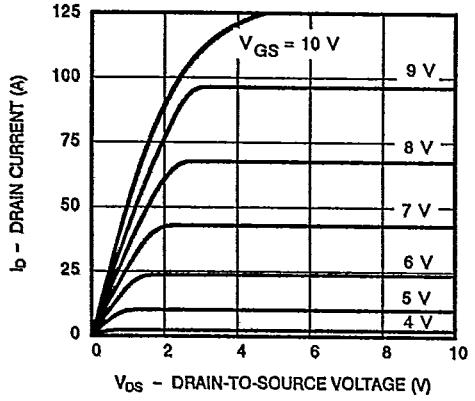


Figure 2. Transfer Characteristics

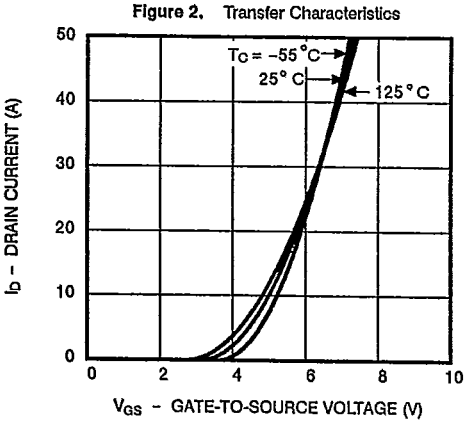


Figure 3. Transconductance

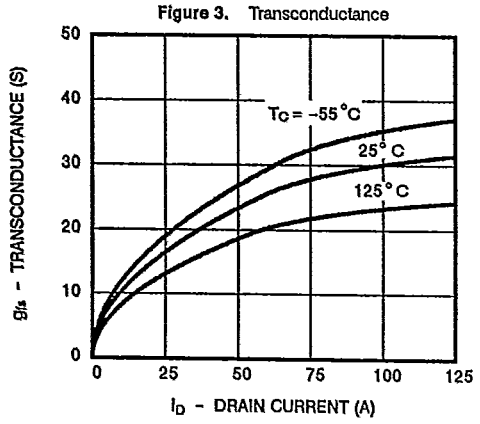


Figure 4. On-Resistance

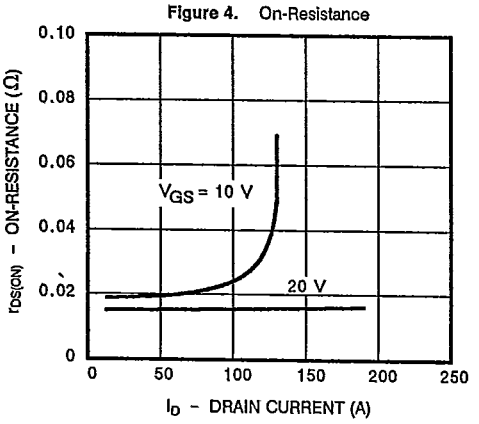


Figure 5. Capacitance

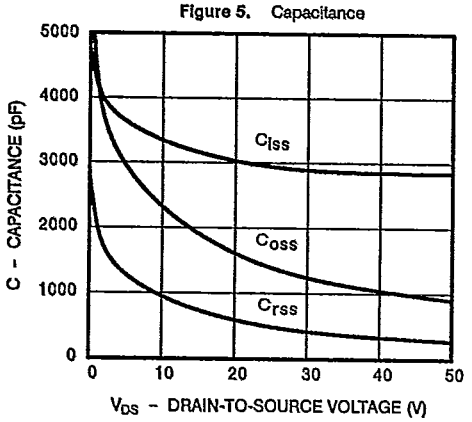
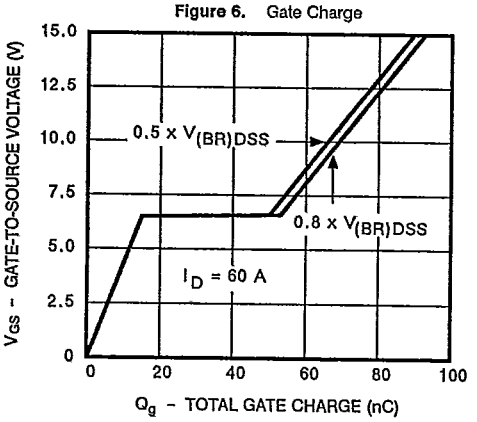


Figure 6. Gate Charge



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TYPICAL CHARACTERISTICS (Cont'd)

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Figure 7. On-Resistance vs. Junction Temperature

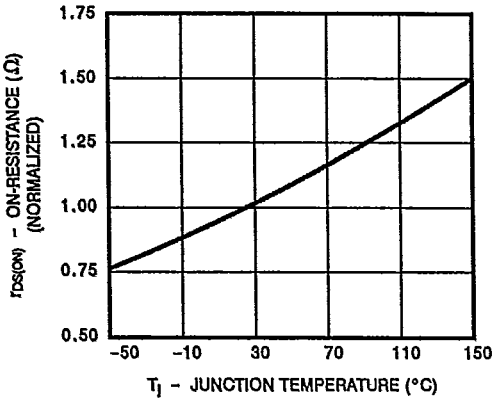
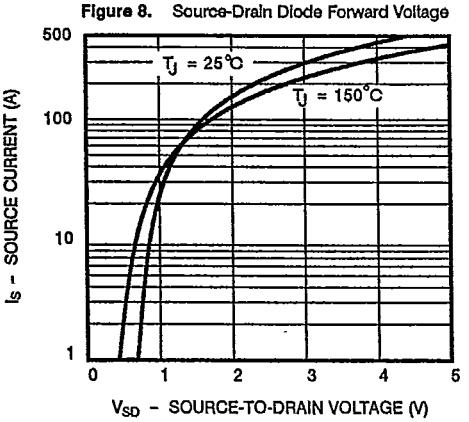


Figure 8. Source-Drain Diode Forward Voltage



THERMAL RATINGS

Figure 9. Maximum Avalanche and Drain Current vs. Case Temperature

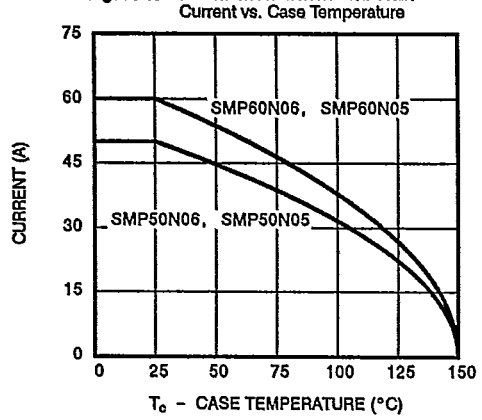
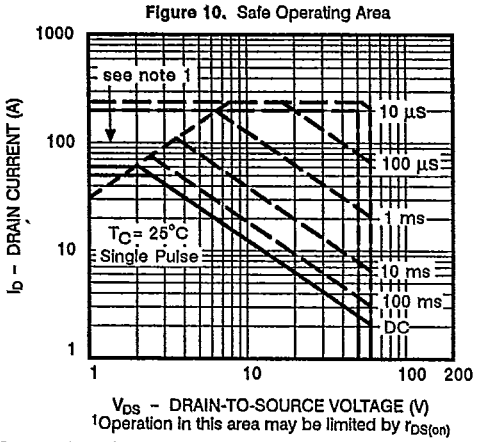


Figure 10. Safe Operating Area



[1]Operation in this area may be limited by $r_{DS(on)}$

Figure 11. Normalized Effective Transient Thermal Impedance, Junction-to-Case