Elektronische Bauelemente

SSPS920NE

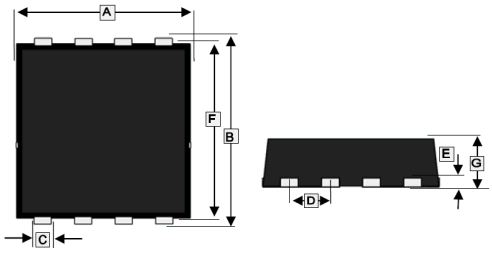
7.1 A, 20 V, $R_{DS(ON)}$ 20 mΩ
Dual-N Channel Mode Power MOSFET

RoHS Compliant Product
A suffix of "-C" specifies halogen & lead-free

DESCRIPTION

These miniature surface mount MOSFETs utilize a high cell density trench process to provide low $R_{DS(on)}$ and to ensure minimal power loss and heat dissipation. Typical applications are DC-DC converters and power management In portable and battery-powered products such as computers, printers, PCMCIA cards, cellular and cordless telephones.

DFN3*3-8PP



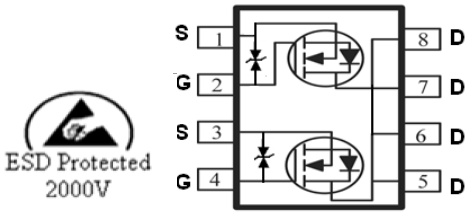
REF.	Millimeter		REF.	Millimeter	
	Min.	Max.		Min.	Max.
A	3.0 BSC.		E	0.08	0.25
B	2.8 BSC.		F	2.3 BSC	
C	0.20	0.35	G	0.7	0.9
D	0.65 BSC.				

FEATURES

- Low $R_{DS(on)}$ provides higher efficiency and extends battery life.
- Low thermal impedance copper leadframe SOP-8 saves board space.
- Fast switching speed.
- High performance trench technology.

PACKAGE INFORMATION

Package	MPQ	Leader Size
DFN3*3-8PP	3K	13' inch



MAXIMUM RATINGS (T_A = 25°C unless otherwise specified)

Parameter		Symbol	Ratings	Unit
Drain-Source Voltage		V_{DS}	20	V
Gate-Source Voltage		V_{GS}	±8	V
Continuous Drain Current [1]	T_A = 25℃	I_D	7.1	A
	T_A = 70℃		5.8	A
Pulsed Drain Current [2]		I_{DM}	40	A
Continuous Source Current (Diode Conduction) [1]		I_S	2.1	A
Total Power Dissipation [1]	T_A = 25℃	P_D	1.5	W
	T_A = 70℃		1	W
Operating Junction & Storage Temperature Range		T_J, T_{STG}	-55 ~ 150	℃
Thermal Resistance Ratings				
Thermal Resistance Junction-ambient (Max.) [1]	t≦10 sec	$R_{\theta JA}$	83	℃ / W
	Steady State		120	℃ / W

Notes:

1. Surface Mounted on 1" x 1" FR4 Board.
2. Pulse width limited by maximum junction temperature.

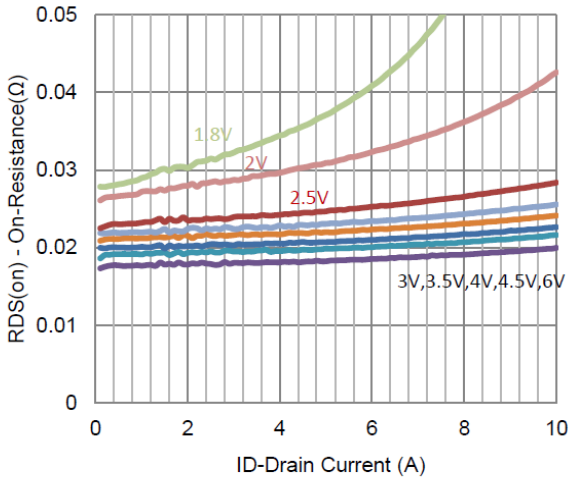
ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise specified)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Teat Conditions
Static						
Gate Threshold Voltage	$V_{GS(th)}$	0.4	-	-	V	V_{DS}= V_{GS}, I_D=250μA
Gate-Body Leakage Current	I_{GSS}	-	-	±100	nA	V_{DS}=0, V_{GS}= ±8V
Zero Gate Voltage Drain Current	I_{DSS}	-	-	1	μA	V_{DS}=16V, V_{GS}=0
		-	-	25	μA	V_{DS}=16V, V_{GS}=0, T_J= 55℃
On-State Drain Current [1]	$I_{D(on)}$	10	-	-	A	V_{DS}= 5V, V_{GS}=4.5V
Drain-Source On-Resistance [1]	$R_{DS(ON)}$	-	-	20	mΩ	V_{GS}= 4.5V, I_D=5.7A
		-	-	24		V_{GS}= 2.5V, I_D=5.2A
		-	-	39		V_{GS}= 1.8V, I_D= 4.8A
Forward Transconductance [1]	g_{fs}	-	15	-	S	V_{DS}= 10V, I_D=5.7A
Diode Forward Voltage	V_{SD}	-	0.71	-	V	I_S=1.1A, V_{GS}=0
Dynamic [2]						
Total Gate Charge	Q_g	-	6	-	nC	I_D= 5.7A V_{DS}= 10V V_{GS}= 4.5V
Gate-Source Charge	Q_{gs}	-	0.9	-		
Gate-Drain Charge	Q_{gd}	-	2.5	-		
Input Capacitance	C_{iss}	-	439	-	pF	V_{GS} =0 V_{DS}=15V f =1.0MHz
Output Capacitance	C_{oss}	-	78	-		
Reverse Transfer Capacitance	C_{rss}	-	68	-		
Turn-On Delay Time	$T_{d(on)}$	-	8	-	nS	V_{DS}= 10V I_D= 5.7A V_{GEN}= 4.5V R_L= 1.8Ω R_{GEN}= 6Ω
Rise Time	T_r	-	14	-		
Turn-Off Delay Time	$T_{d(off)}$	-	42	-		
Fall Time	T_f	-	17	-		

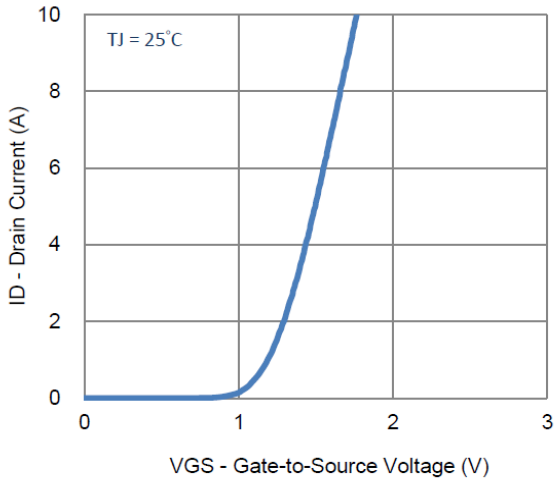
Notes:

1. Pulse test：PW ≦ 300μs duty cycle ≦ 2%.
2. Guaranteed by design, not subject to production testing.

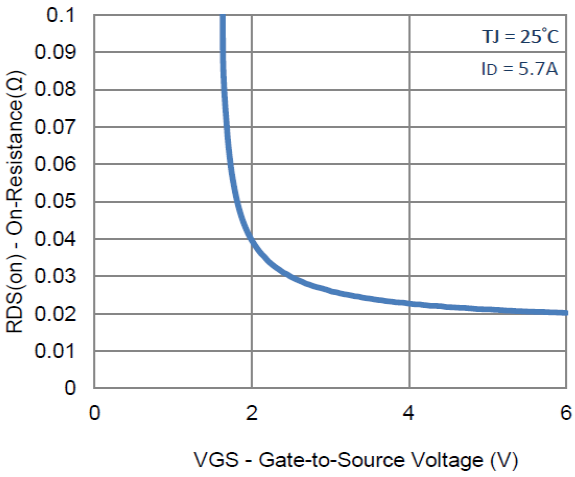
CHARACTERISTIC CURVES



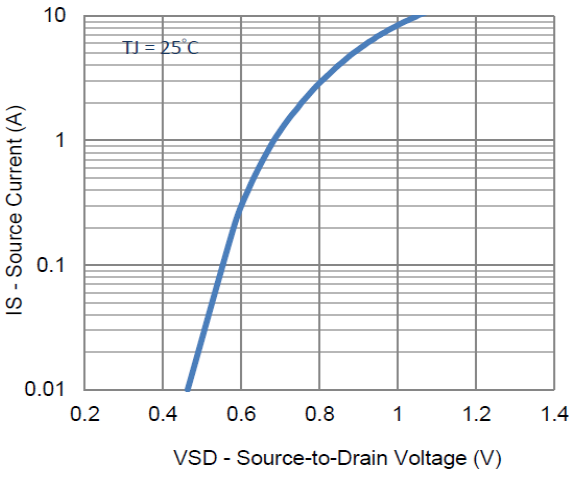
1. On-Resistance vs. Drain Current



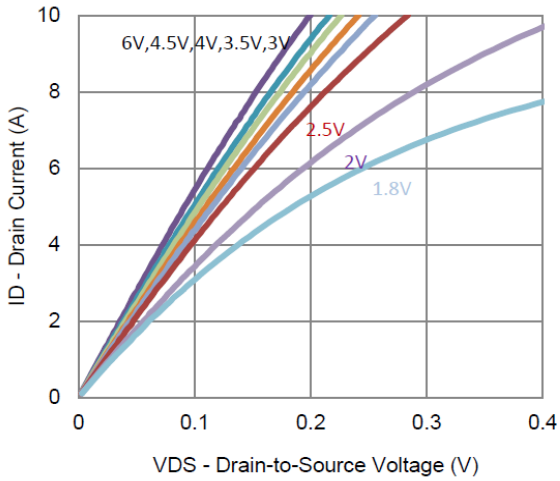
2. Transfer Characteristics



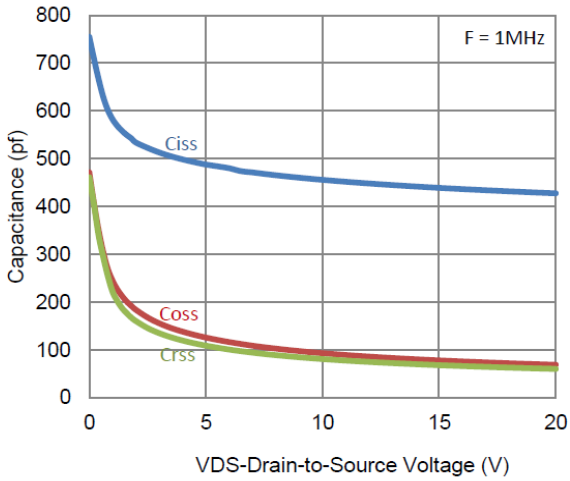
3. On-Resistance vs. Gate-to-Source Voltage



4. Drain-to-Source Forward Voltage

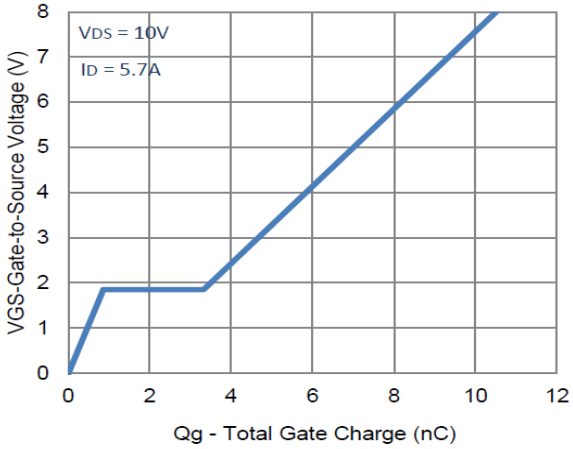


5. Output Characteristics

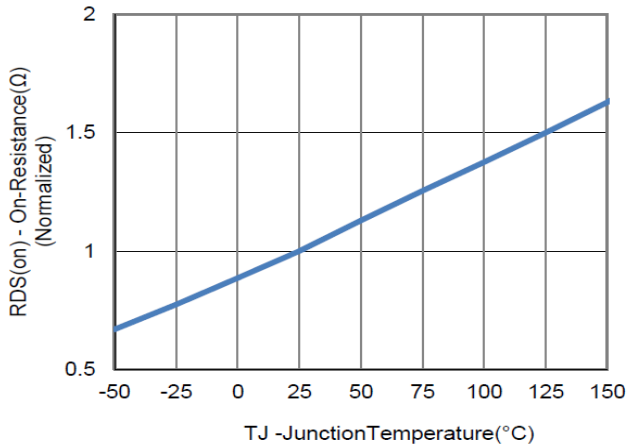


6. Capacitance

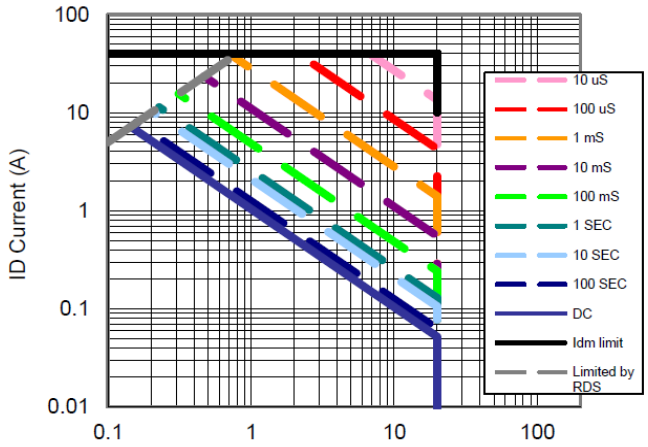
CHARACTERISTIC CURVES



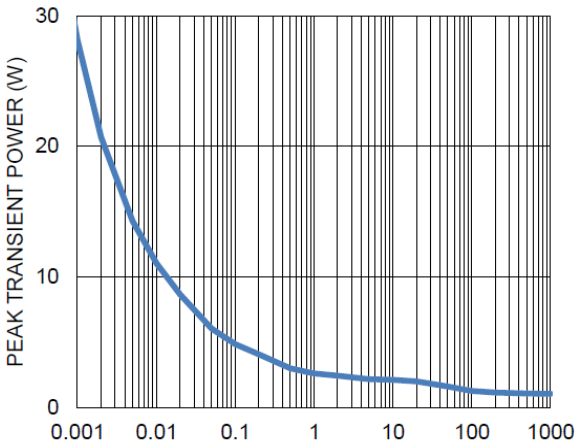
7. Gate Charge



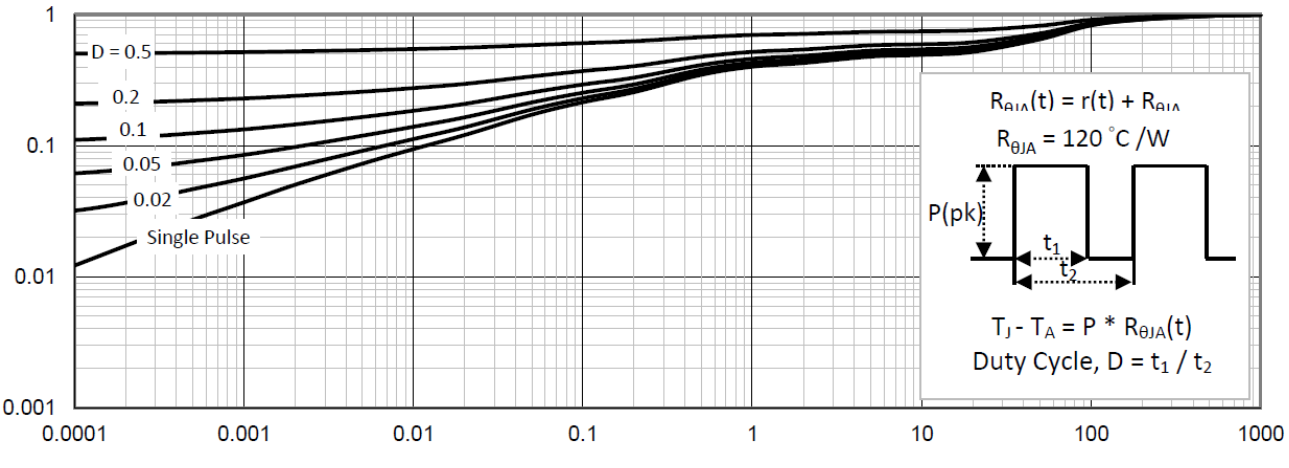
8. Normalized On-Resistance Vs Junction Temperature



9. Safe Operating Area



10. Single Pulse Maximum Power Dissipation



11. Normalized Thermal Transient Junction to Ambient