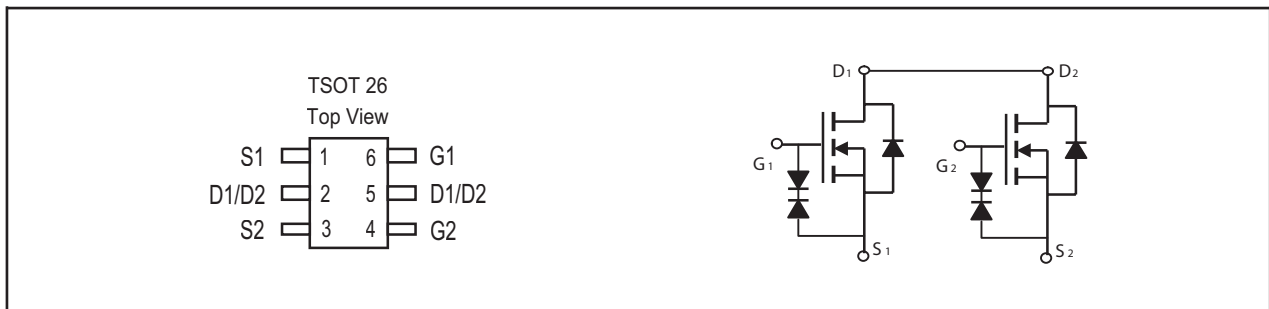


**Dual N-Channel Enhancement Mode Field Effect Transistor**

PRODUCT SUMMARY		
V <sub>DSS</sub>	I <sub>D</sub>	R <sub>DS(ON)</sub> (mΩ) Max
24V	7A	16.5 @ V <sub>GS</sub> =4.0V
		17 @ V <sub>GS</sub> =3.7V
		18 @ V <sub>GS</sub> =3.1V
		27 @ V <sub>GS</sub> =2.5V

**FEATURES**

- Super high dense cell design for low R<sub>DS(ON)</sub>.
- Rugged and reliable.
- Surface Mount Package.
- ESD Protected.

**ABSOLUTE MAXIMUM RATINGS** (T<sub>A</sub>=25°C unless otherwise noted)

Symbol	Parameter	Limit	Units
V <sub>DS</sub>	Drain-Source Voltage	24	V
V <sub>GS</sub>	Gate-Source Voltage	±12	V
I <sub>D</sub>	Drain Current-Continuous <sup>a</sup>	T <sub>A</sub> =25°C	7
		T <sub>A</sub> =70°C	5.6
I <sub>DM</sub>	-Pulsed <sup>b</sup>	45	A
P <sub>D</sub>	Maximum Power Dissipation <sup>a</sup>	T <sub>A</sub> =25°C	1.25
		T <sub>A</sub> =70°C	0.8
T <sub>J</sub> , T <sub>STG</sub>	Operating Junction and Storage Temperature Range	-55 to 150	°C

**THERMAL CHARACTERISTICS**

R <sub>θJA</sub>	Thermal Resistance, Junction-to-Ambient <sup>a</sup>	100	°C/W
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# STS8217

Ver 1.1

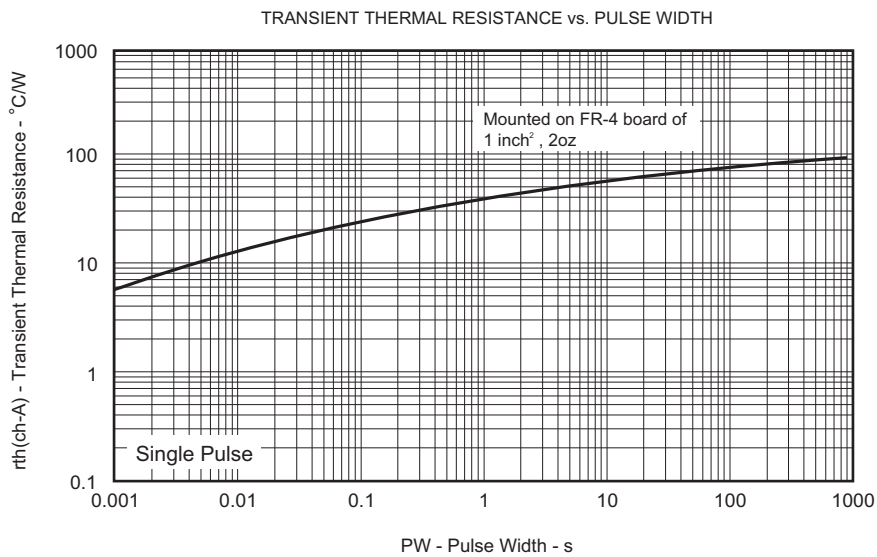
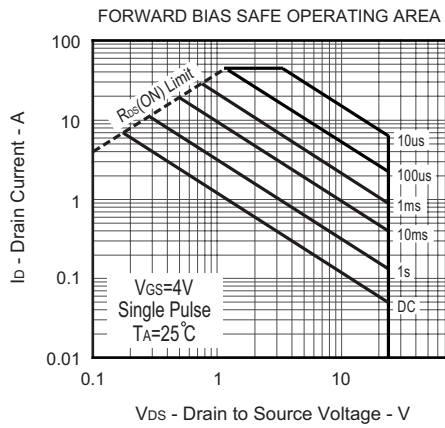
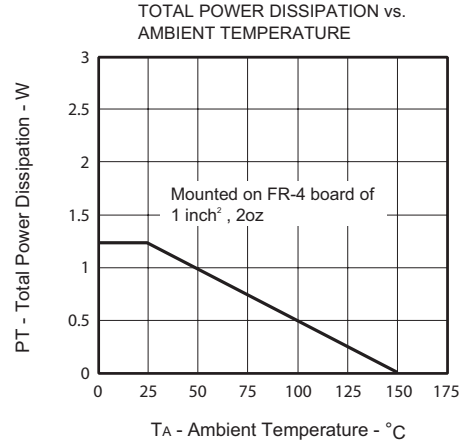
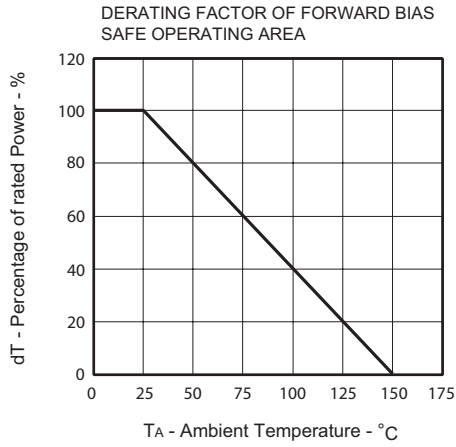
## ELECTRICAL CHARACTERISTICS (TA=25°C unless otherwise noted)

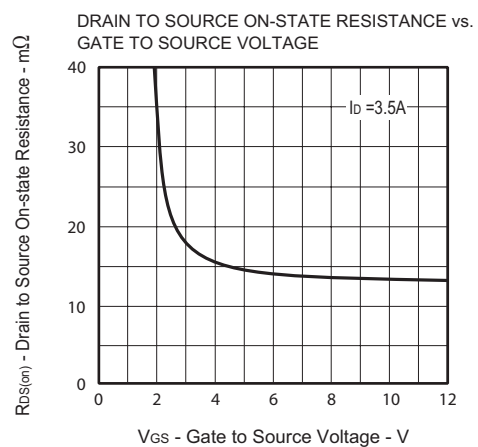
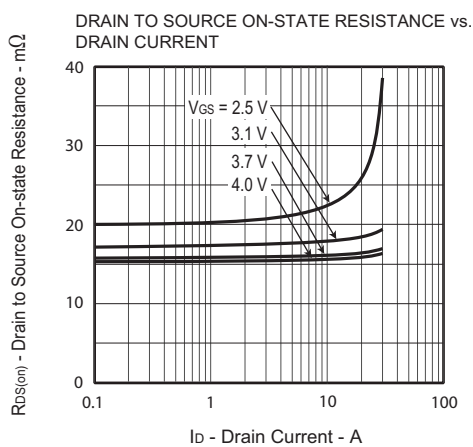
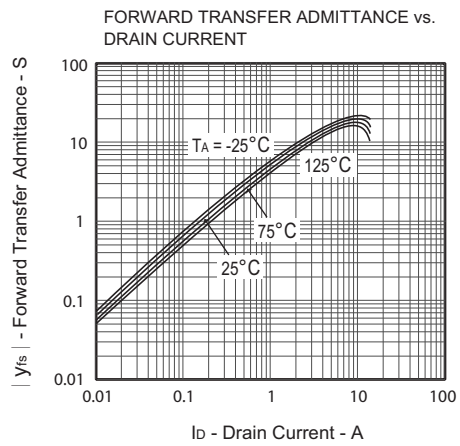
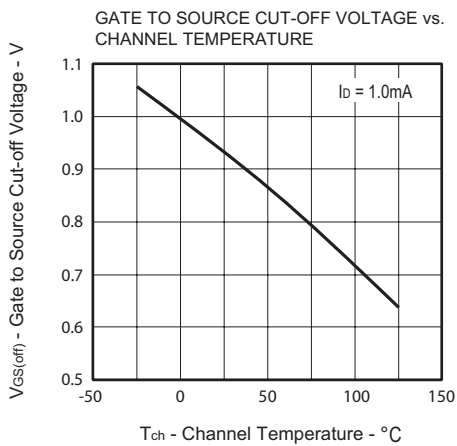
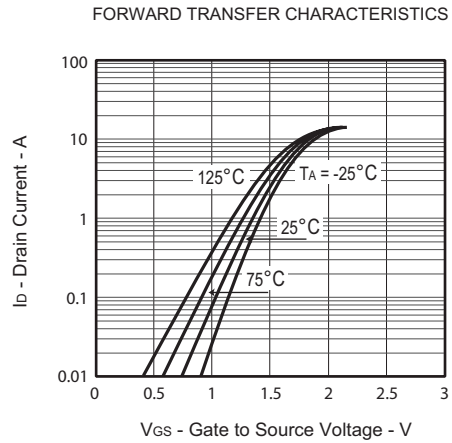
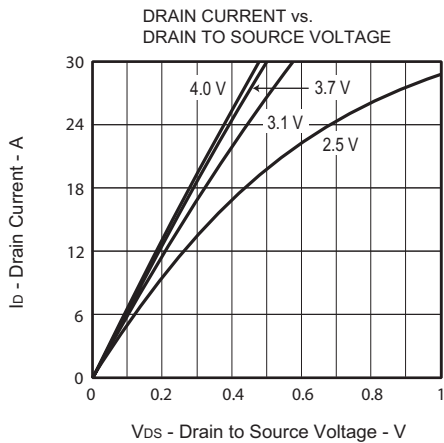
Symbol	Parameter	Conditions	Min	Typ	Max	Units
<b>OFF CHARACTERISTICS</b>						
BV <sub>DSS</sub>	Drain-Source Breakdown Voltage	V <sub>GS</sub> =0V , I <sub>D</sub> =250μA	24			V
I <sub>DSS</sub>	Zero Gate Voltage Drain Current	V <sub>DS</sub> =20V , V <sub>GS</sub> =0V			1	μA
I <sub>GSS</sub>	Gate-Body Leakage Current	V <sub>GS</sub> = ±12V , V <sub>DS</sub> =0V			±10	μA
<b>ON CHARACTERISTICS</b>						
V <sub>GS(th)</sub>	Gate Threshold Voltage	V <sub>DS</sub> =V <sub>GS</sub> , I <sub>D</sub> =1mA	0.5	0.85	1.5	V
R <sub>DS(on)</sub>	Drain-Source On-State Resistance	V <sub>GS</sub> =4.0V , I <sub>D</sub> =3.5A	13	15	16.5	m ohm
		V <sub>GS</sub> =3.7V , I <sub>D</sub> =3.5A	13.5	15.5	17	m ohm
		V <sub>GS</sub> =3.1V , I <sub>D</sub> =3.5A	14.5	16.5	18	m ohm
		V <sub>GS</sub> =2.5V , I <sub>D</sub> =3.5A	15	20	27	m ohm
g <sub>FS</sub>	Forward Transconductance	V <sub>DS</sub> =5V , I <sub>D</sub> =3.5A		16		S
<b>DYNAMIC CHARACTERISTICS <sup>c</sup></b>						
C <sub>ISS</sub>	Input Capacitance	V <sub>DS</sub> =10V, V <sub>GS</sub> =0V f=1.0MHz		564		pF
C <sub>OSS</sub>	Output Capacitance			188		pF
C <sub>RSS</sub>	Reverse Transfer Capacitance			174		pF
<b>SWITCHING CHARACTERISTICS <sup>c</sup></b>						
t <sub>D(ON)</sub>	Turn-On Delay Time	V <sub>DD</sub> =20V I <sub>D</sub> =3.5A V <sub>GS</sub> =4V R <sub>GEN</sub> = 6 ohm		20		ns
t <sub>r</sub>	Rise Time			71.2		ns
t <sub>D(OFF)</sub>	Turn-Off Delay Time			88		ns
t <sub>f</sub>	Fall Time			81.6		ns
Q <sub>g</sub>	Total Gate Charge	V <sub>DS</sub> =20V, I <sub>D</sub> =7A, V <sub>GS</sub> =4V		10.7		nC
Q <sub>gs</sub>	Gate-Source Charge			1.6		nC
Q <sub>gd</sub>	Gate-Drain Charge			4.8		nC
<b>DRAIN-SOURCE DIODE CHARACTERISTICS AND MAXIMUM RATINGS</b>						
V <sub>SD</sub>	Diode Forward Voltage	V <sub>GS</sub> =0V, I <sub>S</sub> =3A		0.81	1.2	V

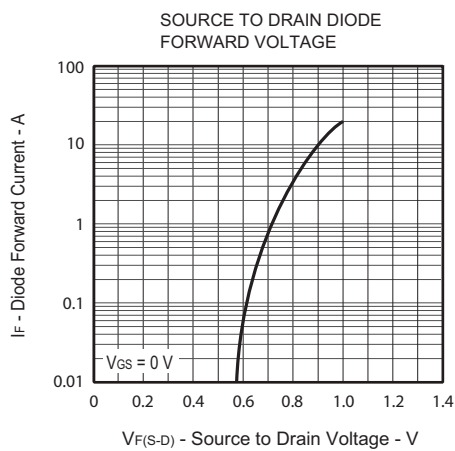
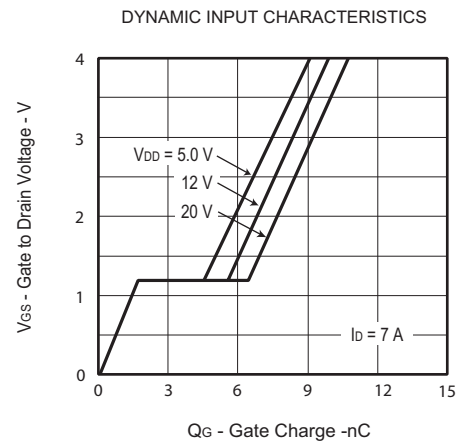
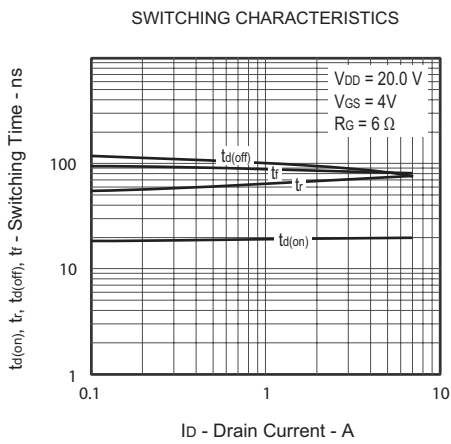
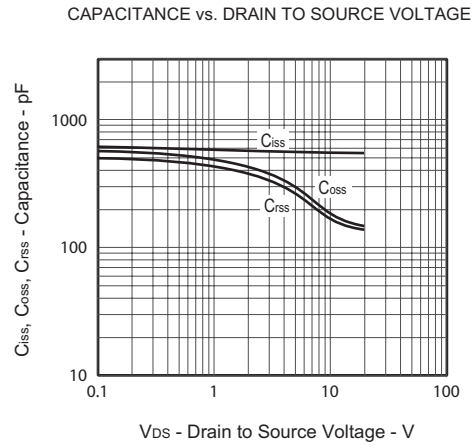
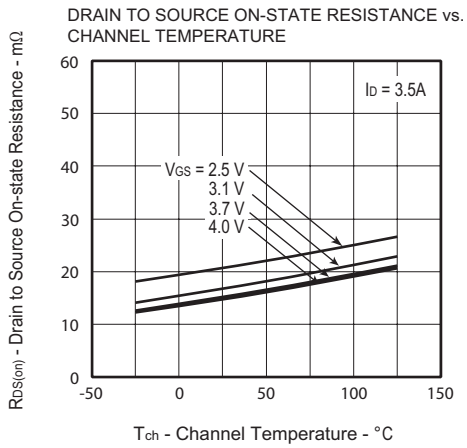
### Notes

- a. Surface Mounted on FR4 Board, t ≤ 10sec.
- b. Pulse Test: Pulse Width ≤ 10μs, Duty Cycle ≤ 1%.
- c. Guaranteed by design, not subject to production testing.

May,07,2012







## PACKAGE OUTLINE DIMENSIONS

