Document Title

256Kx16 Bit High Speed Static RAM(5V Operating), Revolutionary Pin out. Operated at Commercial, Extended and Industrial Temperature Ranges.

Revision History

Rev No.	History	Draft Data	Remark
Rev. 0.0	Initial release with Design Target.	Jun. 14th, 1996	Design Target
Rev. 0.5	Release to Preliminary Data Sheet. 0.1. Replace Design Target to Preliminary. 0.2. Delete 12ns part but add 17ns part. 0.3. Relax D.C and A.C parameters and insert new parameter(I_{CC1}) with the test condition. 0.3.1. Insert I_{CC1} parameter with the test condition as address is increased with binary count. 0.3.2. Relax D.C and A.C parameters.	Sep. 16th, 1996	Preliminary
Rev. 1.0	Release to Final Data Sheet. 1.1. Delete Preliminary. 1.2. Delete Icc1 parameter with the test condition. 1.3. Update D.C parameters. 1.4. Add the test condition for V_{OH1} with Vcc=5V±5% at 25°C. 1.5. Add timing diagram to define t_{WP1} as "(**Timing Wave Form of Write Cycle(OE=Low fixed)".**	Jun. 5th, 1997	Final
Rev.2.0	2.1 Add extended and industrial temperature range parts.	Feb. 25th, 1998	Final
Rev.2.1	Add 44-TSOP2 Package.	Dec. 14th, 1998	Final

Items | Previous spec. (15/ - /20ns part) | Relaxed spec. (15/17/20ns part)

Items	Previous spec. (15/ - /20ns part)	Relaxed spec. (15/17/20ns part)
Icc	250/ - /240mA	280/275/270mA
t_{CW}	10/ - /12ns	12/13/14ns
t_{AW}	10/ - /12ns	12/13/14ns
t_{WP}($\overline{OE}$=H)	10/ - /12ns	12/13/14ns
t_{WP1}($\overline{OE}$=L)	12/ - /14ns	15/17/20ns
t_{DW}	7/ - /9ns	8/ 9/10ns

Items | Previous spec. (15/17/20ns part) | Updated spec. (15/17/20ns part)

Items	Previous spec. (15/17/20ns part)	Updated spec. (15/17/20ns part)
Icc	280/275/270mA	210/205/200mA

256K x 16 Bit High-Speed CMOS Static RAM

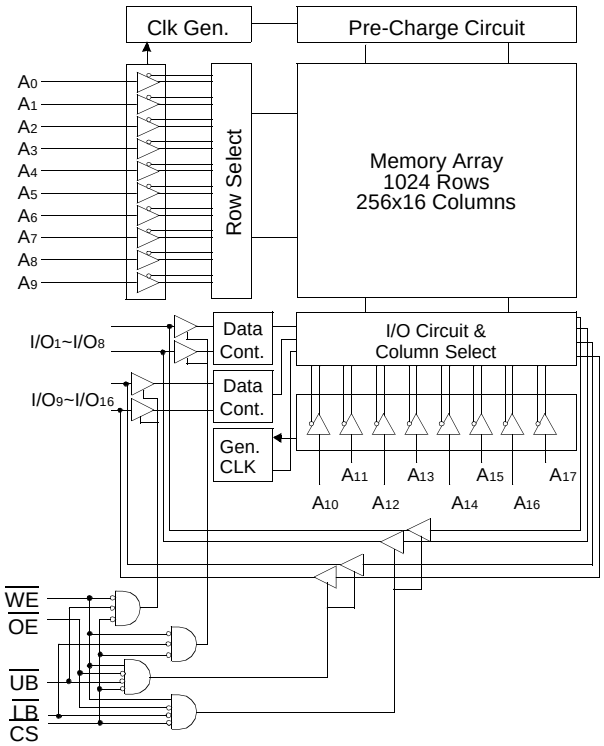
FEATURES

- Fast Access Time 15, 17, 20ns(Max.)
- Low Power Dissipation
  - Standby (TTL) : 50mA(Max.)
  - (CMOS) : 10mA(Max.)
  - Operating K6R4016C1A-15 : 210mA(Max.)
  - K6R4016C1A-17 : 205mA(Max.)
  - K6R4016C1A-20 : 200mA(Max.)
- Single 5.0V±10% Power Supply
- TTL Compatible Inputs and Outputs
- I/O Compatible with 3.3V Devices
- Fully Static Operation
  - No Clock or Refresh required
- Three State Outputs
- Center Power/Ground Pin Configuration
- Data Byte Control ; $\overline{LB}$: I/O_1~ I/O_8, $\overline{UB}$: I/O_9~ I/O_{16}
- Standard Pin Configuration
  - K6R4016C1A-J : 44-SOJ-400
  - K6R4016C1A-T : 44-TSOP2-400BF

ORDERING INFORMATION

K6R4016C1A-C15/C17/C20	Commercial Temp.
K6R4016C1A-E15/E17/E20	Extended Temp.
K6R4016C1A-I15/I17/I20	Industrial Temp.

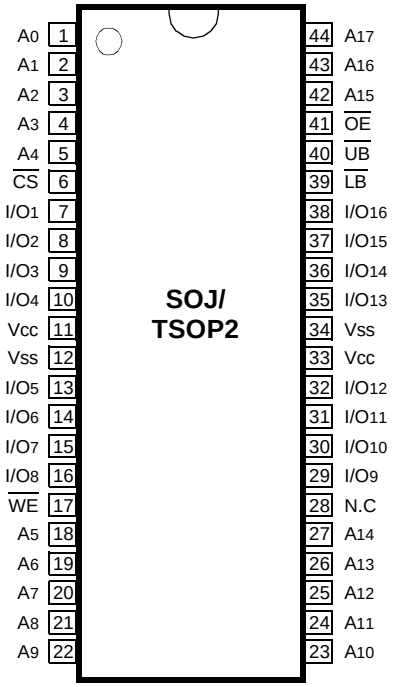
FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

The K6R4016C1A is a 4,194,304-bit high-speed Static Random Access Memory organized as 262,144 words by 16 bits. The K6R4016C1A uses 16 common input and output lines and has an output enable pin which operates faster than address access time at read cycle. Also it allows that lower and upper byte access by data byte control($\overline{UB}$, $\overline{LB}$). The device is fabricated using SAMSUNG′s advanced CMOS process and designed for high-speed circuit technology. It is particularly well suited for use in high-density high-speed system applications. The K6R4016C1A is packaged in a 400mil 44-pin plastic SOJ or TSOP(II) forward.

PIN CONFIGURATION *(Top View)*



PIN FUNCTION

Pin Name	Pin Function
A_0 - A_{17}	Address Inputs
$\overline{WE}$	Write Enable
$\overline{CS}$	Chip Select
$\overline{OE}$	Output Enable
$\overline{LB}$	Lower-byte Control(I/O_1~I/O_8)
$\overline{UB}$	Upper-byte Control(I/O_9~I/O_{16})
I/O_1 ~ I/O_{16}	Data Inputs/Outputs
V_{CC}	Power(+5.0V)
V_{SS}	Ground
N.C	No Connection

ABSOLUTE MAXIMUM RATINGS*

Parameter		Symbol	Rating	Unit
Voltage on Any Pin Relative to V_{SS}		V_{IN}, V_{OUT}	-0.5 to 7.0	V
Voltage on V_{CC} Supply Relative to V_{SS}		V_{CC}	-0.5 to 7.0	V
Power Dissipation		P_D	1.0	W
Storage Temperature		T_{STG}	-65 to 150	°C
Operating Temperature	Commercial	T_A	0 to 70	°C
	Extended	T_A	-25 to 85	°C
	Industrial	T_A	-40 to 85	°C

***** Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operating sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS*(T_A=0 to 70°C)

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Ground	V_{SS}	0	0	0	V
Input High Voltage	V_{IH}	2.2	-	V_{CC} + 0.5**	V
Input Low Voltage	V_{IL}	-0.5*	-	0.8	V

* The above parameters are also guaranteed at extended and industrial temperature ranges.
****** V_{IL}(Min) = -2.0V a.c(Pulse Width ≤ 10ns) for I ≤ 20mA.
******* V_{IH}(Max) = V_{CC} + 2.0V a.c (Pulse Width ≤ 10ns) for I ≤ 20mA.

DC AND OPERATING CHARACTERISTICS*(T_A=0 to 70°C, Vcc=5.0V±10%, unless otherwise specified)

Parameter	Symbol	Test Conditions		Min	Max	Unit
Input Leakage Current	I_{LI}	V_{IN}=V_{SS} to V_{CC}		-2	2	µA
Output Leakage Current	I_{LO}	$\overline{CS}$=V_{IH} or $\overline{OE}$=V_{IH} or $\overline{WE}$=V_{IL} V_{OUT} = V_{SS} to V_{CC}		-2	2	µA
Operating Current	I_{CC}	Min. Cycle, 100% Duty $\overline{CS}$=V_{IL}, V_{IN}=V_{IH} or V_{IL}, I_{OUT}=0mA	15ns	-	210	mA
			17ns	-	205	
			20ns	-	200	
Standby Current	I_{SB}	Min. Cycle, $\overline{CS}$=V_{IH}		-	50	mA
	I_{SB1}	f=0MHz, $\overline{CS}$≥V_{CC}-0.2V, V_{IN}≥V_{CC}-0.2V or V_{IN}≤0.2V		-	10	mA
Output Low Voltage Level	V_{OL}	I_{OL}=8mA		-	0.4	V
Output High Voltage Level	V_{OH}	I_{OH}=-4mA		2.4	-	V

* The above parameters are also guaranteed at extended and industrial temperature ranges.

CAPACITANCE*(T_A=25°C, f=1.0MHz)

Item	Symbol	Test Conditions	MIN	Max	Unit
Input/Output Capacitance	$C_{I/O}$	$V_{I/O}$=0V	-	8	pF
Input Capacitance	C_{IN}	V_{IN}=0V	-	7	pF

* Capacitance is sampled and not 100% tested.

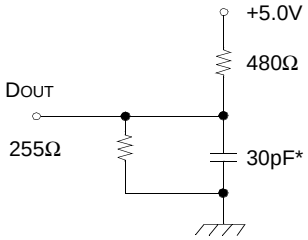
AC CHARACTERISTICS(T_A=0 to 70°C, V_{CC}=5.0V±10%, unless otherwise noted.)

TEST CONDITIONS*

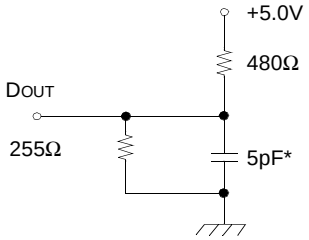
Parameter	Value
Input Pulse Levels	0V to 3V
Input Rise and Fall Times	3ns
Input and Output timing Reference Levels	1.5V
Output Loads	See below

* The above parameters are also guaranteed at extended and industrial temperature ranges.

Output Loads(A)



Output Loads(B)
for t_{HZ}, t_{LZ}, t_{WHZ}, t_{OW}, t_{OLZ} & t_{OHZ}



* Including Scope and Jig Capacitance

READ CYCLE*

Parameter	Symbol	K6R4016C1A-15		K6R4016C1A-17		K6R4016C1A-20		Unit
		Min	Max	Min	Max	Min	Max	
Read Cycle Time	t_{RC}	15	-	17	-	20	-	ns
Address Access Time	t_{AA}	-	15	-	17	-	20	ns
Chip Select to Output	t_{CO}	-	15	-	17	-	20	ns
Output Enable to Valid Output	t_{OE}	-	7	-	8	-	9	ns
$\overline{UB}$, $\overline{LB}$ Access Time	t_{BA}	-	7	-	8	-	9	ns
Chip Enable to Low-Z Output	t_{LZ}	3	-	3	-	3	-	ns
Output Enable to Low-Z Output	t_{OLZ}	0	-	0	-	0	-	ns
$\overline{UB}$, $\overline{LB}$ Enable to Low-Z Output	t_{BLZ}	0	-	0	-	0	-	ns
Chip Disable to High-Z Output	t_{HZ}	0	7	0	8	0	9	ns
Output Disable to High-Z Output	t_{OHZ}	0	7	0	8	0	9	ns
$\overline{UB}$, $\overline{LB}$ Disable to High-Z Output	t_{BHZ}	0	7	0	8	0	9	ns
Output Hold from Address Change	t_{OH}	3	-	3	-	3	-	ns

* The above parameters are also guaranteed at extended and industrial temperature ranges.

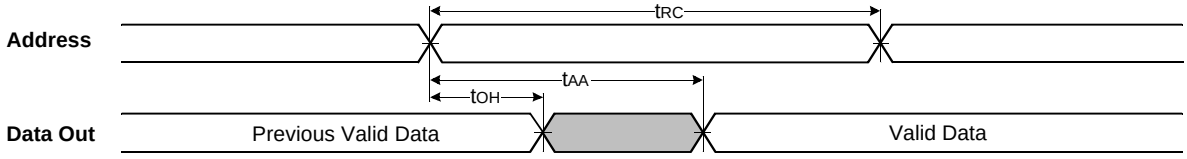
WRITE CYCLE*

Parameter	Symbol	K6R4016C1A-15		K6R4016C1A-17		K6R4016C1A-20		Unit
		Min	Max	Min	Max	Min	Max	
Write Cycle Time	t_{WC}	15	-	17	-	20	-	ns
Chip Select to End of Write	t_{CW}	12	-	13	-	14	-	ns
Address Set-up Time	t_{AS}	0	-	0	-	0	-	ns
Address Valid to End of Write	t_{AW}	12	-	13	-	14	-	ns
Write Pulse Width($\overline{OE}$ High)	t_{WP}	12	-	13	-	14	-	ns
Write Pulse Width($\overline{OE}$ Low)	t_{WP1}	15	-	17	-	20	-	ns
$\overline{UB}$, $\overline{LB}$ Valid to End of Write	t_{BW}	12	-	13	-	14	-	ns
Write Recovery Time	t_{WR}	0	-	0	-	0	-	ns
Write to Output High-Z	t_{WHZ}	0	7	0	8	0	9	ns
Data to Write Time Overlap	t_{DW}	8	-	9	-	10	-	ns
Data Hold from Write Time	t_{DH}	0	-	0	-	0	-	ns
End Write to Output Low-Z	t_{OW}	3	-	3	-	3	-	ns

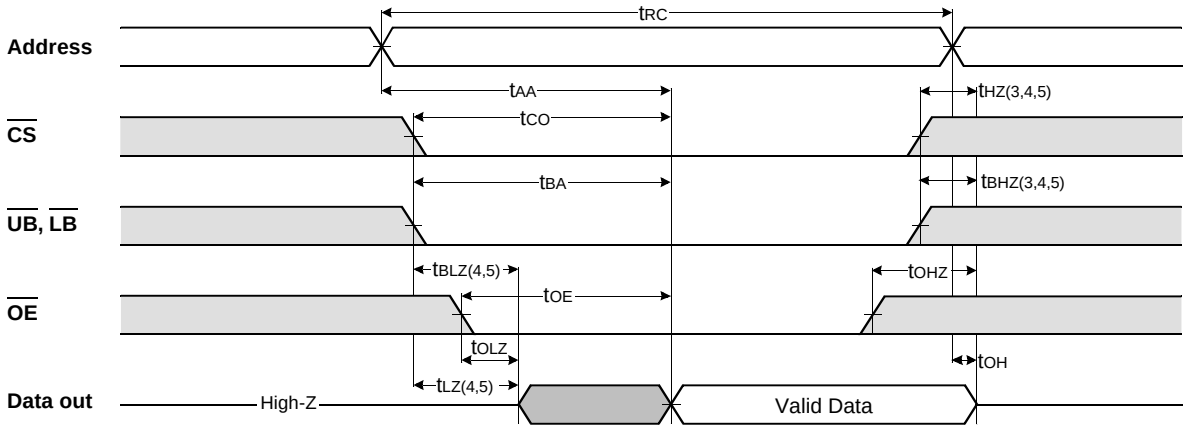
* The above parameters are also guaranteed at extended and industrial temperature ranges.

TIMMING DIAGRAMS

TIMING WAVEFORM OF READ CYCLE(1) (Address Controlled, $\overline{CS}$=$\overline{OE}$=V_{IL}, $\overline{WE}$=V_{IH}, $\overline{UB}$, $\overline{LB}$=V_{IL})



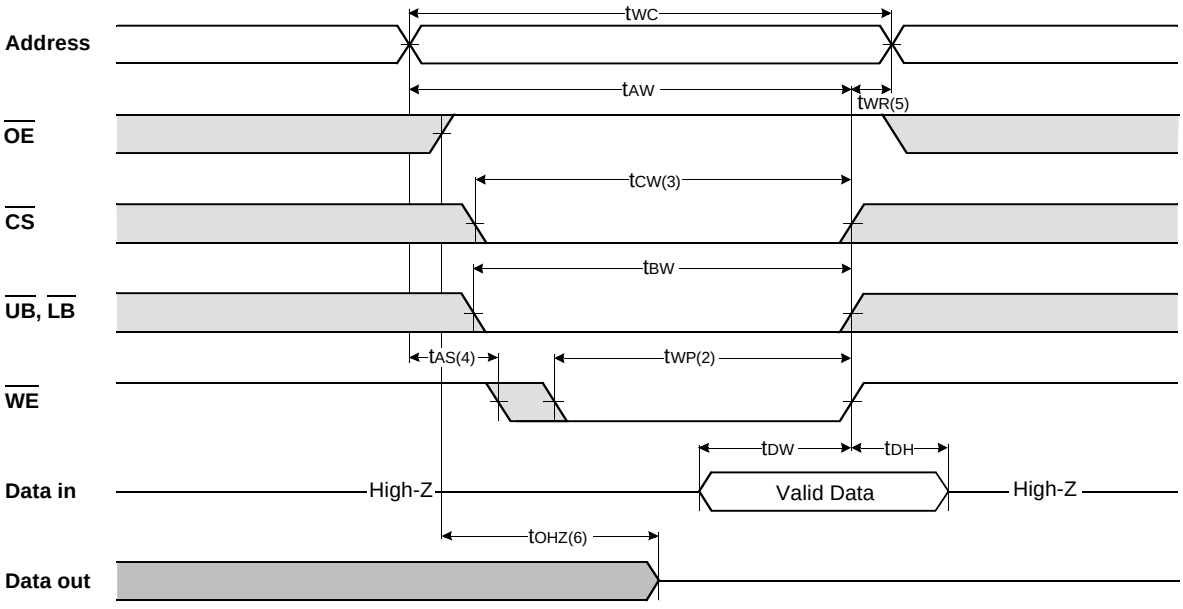
TIMING WAVEFORM OF READ CYCLE(2) ($\overline{WE}$=V_{IH})



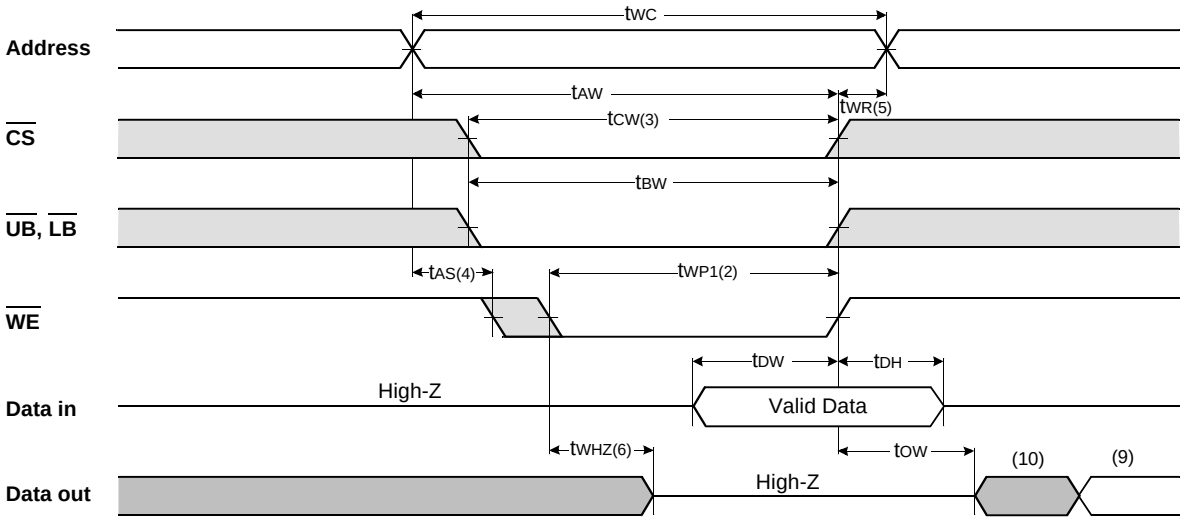
NOTES(READ CYCLE)

1. $\overline{WE}$ is high for read cycle.
2. All read cycle timing is referenced from the last valid address to the first transition address.
3. t_{HZ} and t_{OHZ} are defined as the time at which the outputs achieve the open circuit condition and are not referenced to V_{OH} or V_{OL} levels.
4. At any given temperature and voltage condition, t_{HZ}(Max.) is less than t_{LZ}(Min.) both for a given device and from device to device.
5. Transition is measured ±200mV from steady state voltage with Load(B). This parameter is sampled and not 100% tested.
6. Device is continuously selected with $\overline{CS}$=V_{IL}.
7. Address valid prior to coincident with $\overline{CS}$ transition low.
8. For common I/O applications, minimization or elimination of bus contention conditions is necessary during read and write cycle.

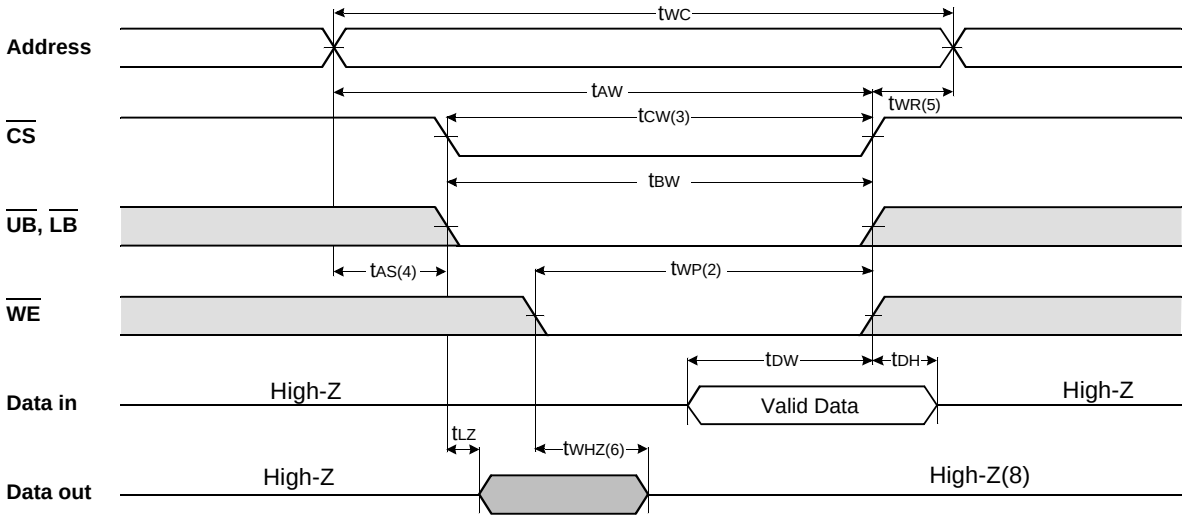
TIMING WAVEFORM OF WRITE CYCLE(1) ($\overline{OE}$ Clock)



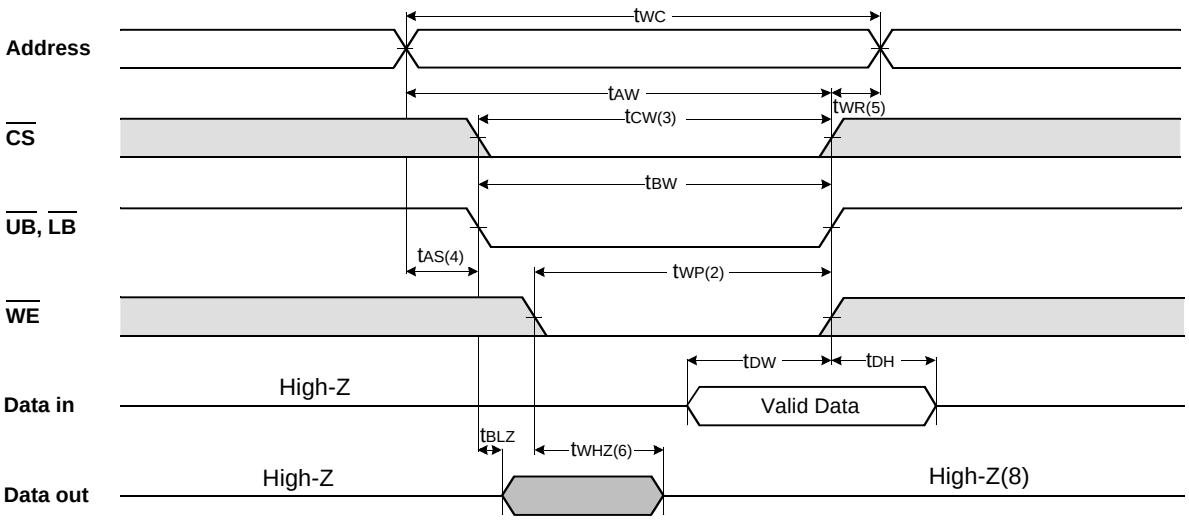
TIMING WAVEFORM OF WRITE CYCLE(2) ($\overline{OE}$ =Low fixed)



TIMING WAVEFORM OF WRITE CYCLE(3) ($\overline{CS}$=Controlled)



TIMING WAVEFORM OF WRITE CYCLE(4) ($\overline{UB}$, $\overline{LB}$ Controlled)



NOTES(WRITE CYCLE)

1. All write cycle timing is referenced from the last valid address to the first transition address.
2. A write occurs during the overlap of a low $\overline{CS}$,$\overline{WE}$,$\overline{LB}$ and $\overline{UB}$. A write begins at the latest transition $\overline{CS}$ going low and $\overline{WE}$ going low; A write ends at the earliest transition $\overline{CS}$ going high or $\overline{WE}$ going high. t_{WP} is measured from the beginning of write to the end of write.
3. t_{CW} is measured from the later of $\overline{CS}$ going low to end of write.
4. t_{AS} is measured from the address valid to the beginning of write.
5. t_{WR} is measured from the end of write to the address change. t_{WR} applied in case a write ends as $\overline{CS}$ or $\overline{WE}$ going high.
6. If $\overline{OE}$, $\overline{CS}$ and $\overline{WE}$ are in the Read Mode during this period, the I/O pins are in the output low-Z state. Inputs of opposite phase of the output must not be applied because bus contention can occur.
7. For common I/O applications, minimization or elimination of bus contention conditions is necessary during read and write cycle.
8. If $\overline{CS}$ goes low simultaneously with $\overline{WE}$ going or after $\overline{WE}$ going low, the outputs remain high impedance state.
9. Dout is the read data of the new address.
10. When $\overline{CS}$ is low: I/O pins are in the output state. The input signals in the opposite phase leading to the output should not be applied.

FUNCTIONAL DESCRIPTION

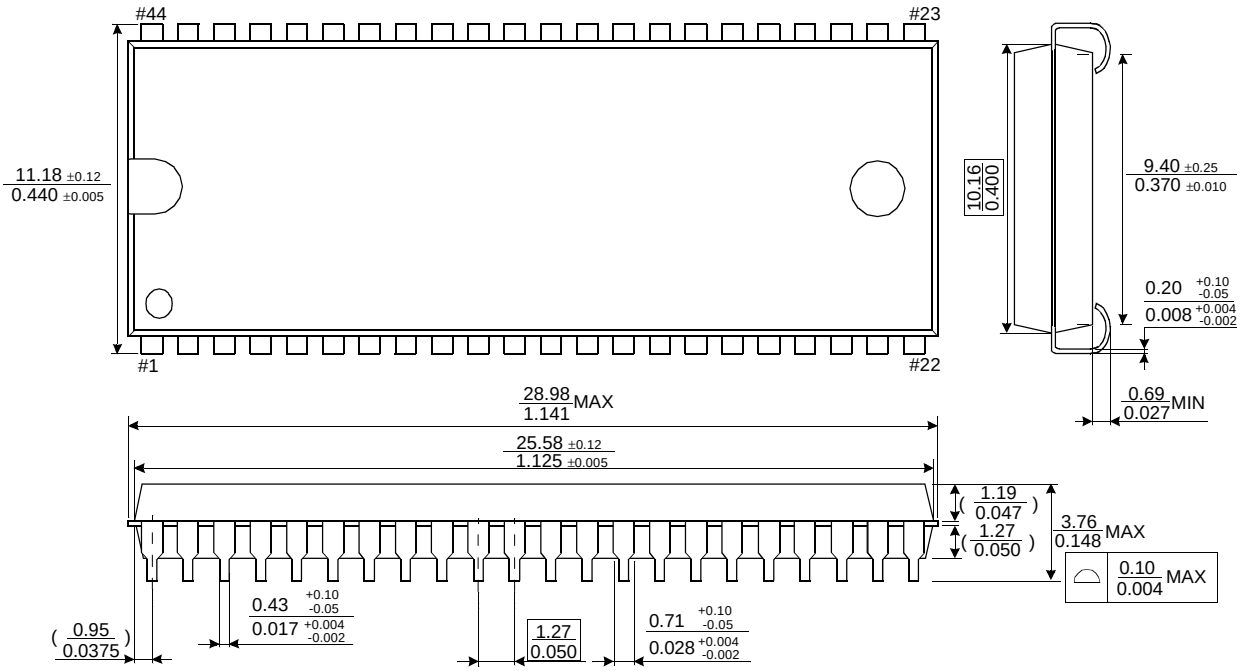
$\overline{CS}$	$\overline{WE}$	$\overline{OE}$	$\overline{LB}$	$\overline{UB}$	Mode	I/O Pin		Supply Current
						I/O_1~I/O_8	I/O_9~I/O_{16}	
H	X	X*	X	X	Not Select	High-Z	High-Z	I_{SB}, I_{SB1}
L	H	H	X	X	Output Disable	High-Z	High-Z	I_{CC}
L	X	X	H	H				
L	H	L	L	H	Read	D_{OUT}	High-Z	I_{CC}
			H	L		High-Z	D_{OUT}	
			L	L		D_{OUT}	D_{OUT}	
L	L	X	L	H	Write	D_{IN}	High-Z	I_{CC}
			H	L		High-Z	D_{IN}	
			L	L		D_{IN}	D_{IN}	

* X means Don't Care.

PACKAGE DIMENSIONS

Units:millimeters/Inches

44-SOJ-400



44-TSOP2-400BF

Units:millimeters/Inches