



SANYO Semiconductors

DATA SHEET

LV8222W — Bi-CMOS IC

CD/MD System Motor Driver

Overview

The LV8222W is a CD/MD system motor driver.

Features

- PWM H-bridge motor driver (3ch) and direct PWM sensorless motor driver.

Specifications

Absolute Maximum Ratings at Ta = 25°C

Parameter	Symbol	Conditions	Ratings	Unit
Power supply voltage	V _{CC} max		6.0	V
Output block power supply voltage	V _S max		6.0	V
Pre-drive voltage (gate voltage)	V _G max		9.5	V
Output current	I _O max		0.8	A
Power dissipation 1	Pd max1	Independent IC	0.5	W
Power dissipation 2	Pd max2	Glass epoxy board: 114.3mm×76.1mm×1.6mm	1.5	W
Operating temperature	T _{opr}		-20 to +85	°C
Storage temperature	T _{stg}		-55 to +150	°C

Recommended operating voltage at Ta = 25°C

Parameter	Symbol	Conditions	Ratings	Unit
Power supply voltage	V _{CC}		2.1 to 5.5	V
Output block power supply voltage	V _S		0 to 5.5	V
Pre-drive voltage (gate voltage)	V _G	V _G ≤ 9.5V	V _S +3.5 to V _S +4.5	V

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LV8222W

Electrical Characteristics at $T_a = 25^\circ\text{C}$, $V_{CC} = 2.4\text{V}$, $V_S = 2.4\text{V}$

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Power supply current 1	I_{CC1}	S/S pin H, MUTE pin H (when operating)		1.5	2.0	mA
Power supply current 2	I_{CC2}	S/S pin L (standby mode)			20	μA
Charge pump output						
Output voltage	VG	$V_S = 2.4\text{V}$	5.9	6.4	6.9	V
VG regulator output						
Output voltage	VGREG		3.5	4.0	4.5	V
Overheat protection circuit						
Thermal protection circuit operating temperature	TSD	*Design target	150	180		$^\circ\text{C}$
Hysteresis width	ΔTSD	*Design target		40		$^\circ\text{C}$
Power supply monitor						
Monitor output voltage	VSMON	$V_S = 2.4\text{V}$	1.1	1.2	1.3	V
Actuator block [Actuator input pin]						
High level input voltage range	VAIH		$V_{CC}-0.5$		V_{CC}	V
Low level input voltage range	VAIL		0		0.5	V
Output block						
Output ON resistance	Ron1,2,3	$I_O = 0.5\text{A}$, sum of upper and lower outputs		1.5	2.5	Ω
Output transmission delay time (H-bridge)	TRISE	*Design target		0.1		μs
	TFALL	*Design target		0.1		μs
Minimum input pulse width	Tmin	Ch1, ch2 output pulse width is 2/3 tmin or more *Design target	200			ns
MUTE pin						
High level input voltage range	VMUH	MUTE OFF	$V_{CC}-0.5$		V_{CC}	V
Low level input voltage range	VMUL	MUTE ON	0		0.5	V
Spindle motor driver side [Output side ON resistance]						
SOURCE1	Ron(H1)	$I_O = 0.5\text{A}$, $V_S = 1.2\text{V}$, $V_G = 5.2\text{V}$, forward TR		0.5	1.0	Ω
SOURCE2	Ron(H2)	$I_O = 0.5\text{A}$, $V_S = 1.2\text{V}$, $V_G = 5.2\text{V}$, reverse TR		0.5	1.0	Ω
SINK	Ron(L)	$I_O = 0.5\text{A}$, $V_S = 1.2\text{V}$		0.5	1.0	Ω
SOURCE+SINK	Ron(H+L)	$I_O = 0.5\text{A}$, $V_S = 1.2\text{V}$, $V_G = 5.2\text{V}$		1.0	2.0	Ω
Position detection comparator						
Input offset voltage	VSOFS	*Design target	-9		+9	mV
VCO pin						
VCO High level voltage	VCOH		0.6	0.8	1.0	V
VCO Low level voltage	VCOL		0.3	0.5	0.7	V
S/S pin						
High level input voltage range	VSSH	Start	$V_{CC}-0.5$		V_{CC}	V
Low level input voltage range	VSSL	Stop	0		0.5	V
Current limiter						
Limiter voltage	VRF		0.17	0.19	0.21	V
BREAK pin						
High level input voltage range	VBRH	Brake ON	$V_{CC}-0.5$		V_{CC}	V
Low level input voltage range	VBRL	Brake OFF	0		0.5	V
PWM pin						
High level input voltage range	VPWMH		$V_{CC}-0.5$		V_{CC}	V
Low level input voltage range	VPWML		0		0.5	V
PWM input frequency	VPWMIN				150	kHz
CLK pin						
High level input voltage range	VCLKH		$V_{CC}-0.5$		V_{CC}	V
Low level input voltage range	VCLKL		0		0.5	V

* Design target value and no measurement is performed.

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LV8222W

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Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
FG output pin						
High level output voltage	VFGH	$I_O = -0.5\text{mA}$	$V_{CC}-0.5$		V_{CC}	V
Low level output voltage	VFGL	$I_O = 0.5\text{mA}$	0		0.5	V
MODE 1/2 pin						
High level output voltage	VMDH		$V_{CC}-0.5$		V_{CC}	V
Low level output voltage	VMDL		0		0.5	V

Actuator Truth Table

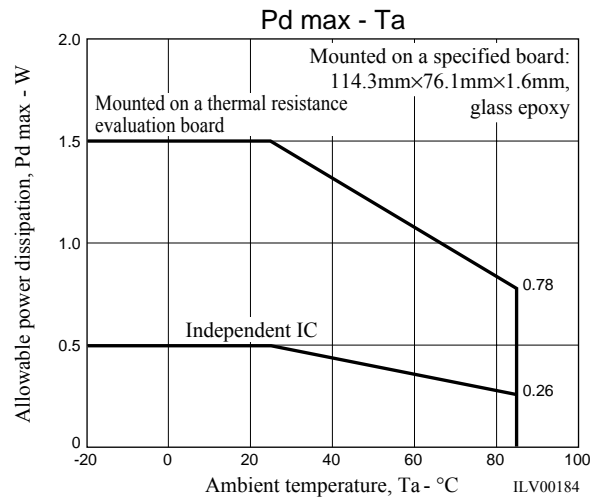
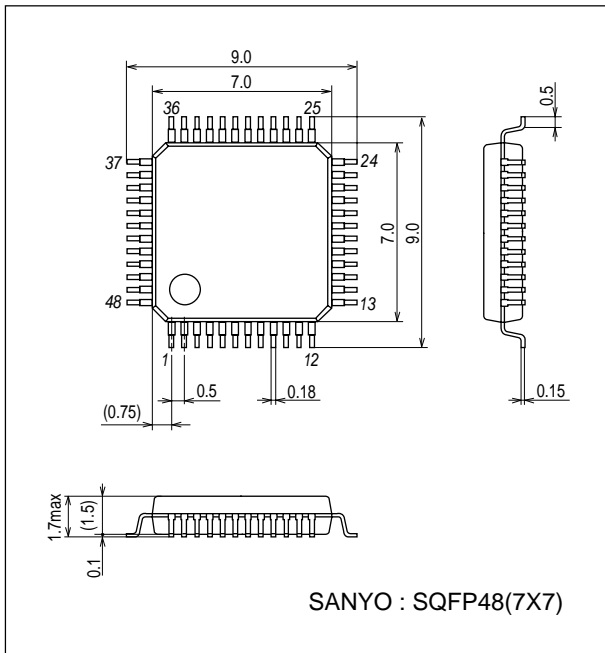
H Bridge Block

MUTE	IN1 to 3F	IN1 to 3R	OUT1 to 3F	OUT1 to 3R
H	L	L	L	L
H	H	L	H	L
H	L	H	L	H
H	H	H	L	L
L	x	x	Z	Z

Package Dimensions

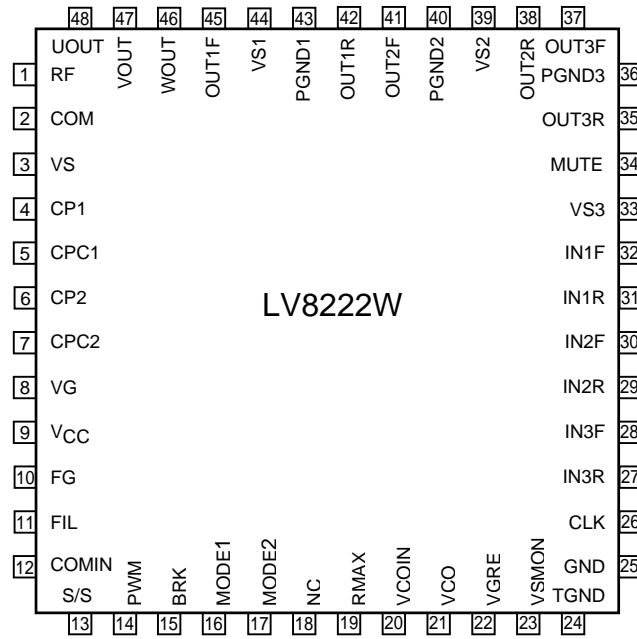
unit : mm (typ)

3163B



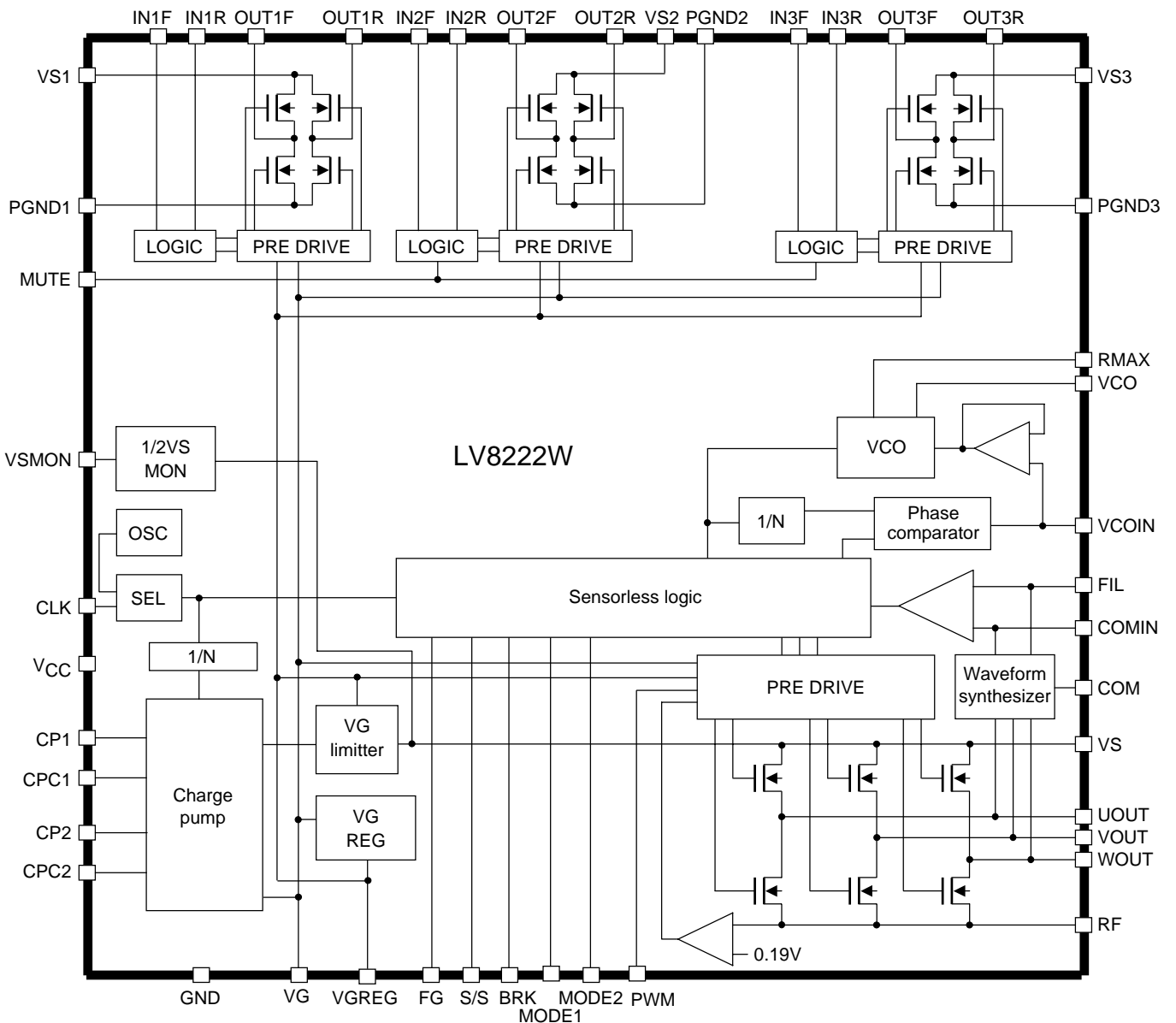
LV8222W

Pin Assignment



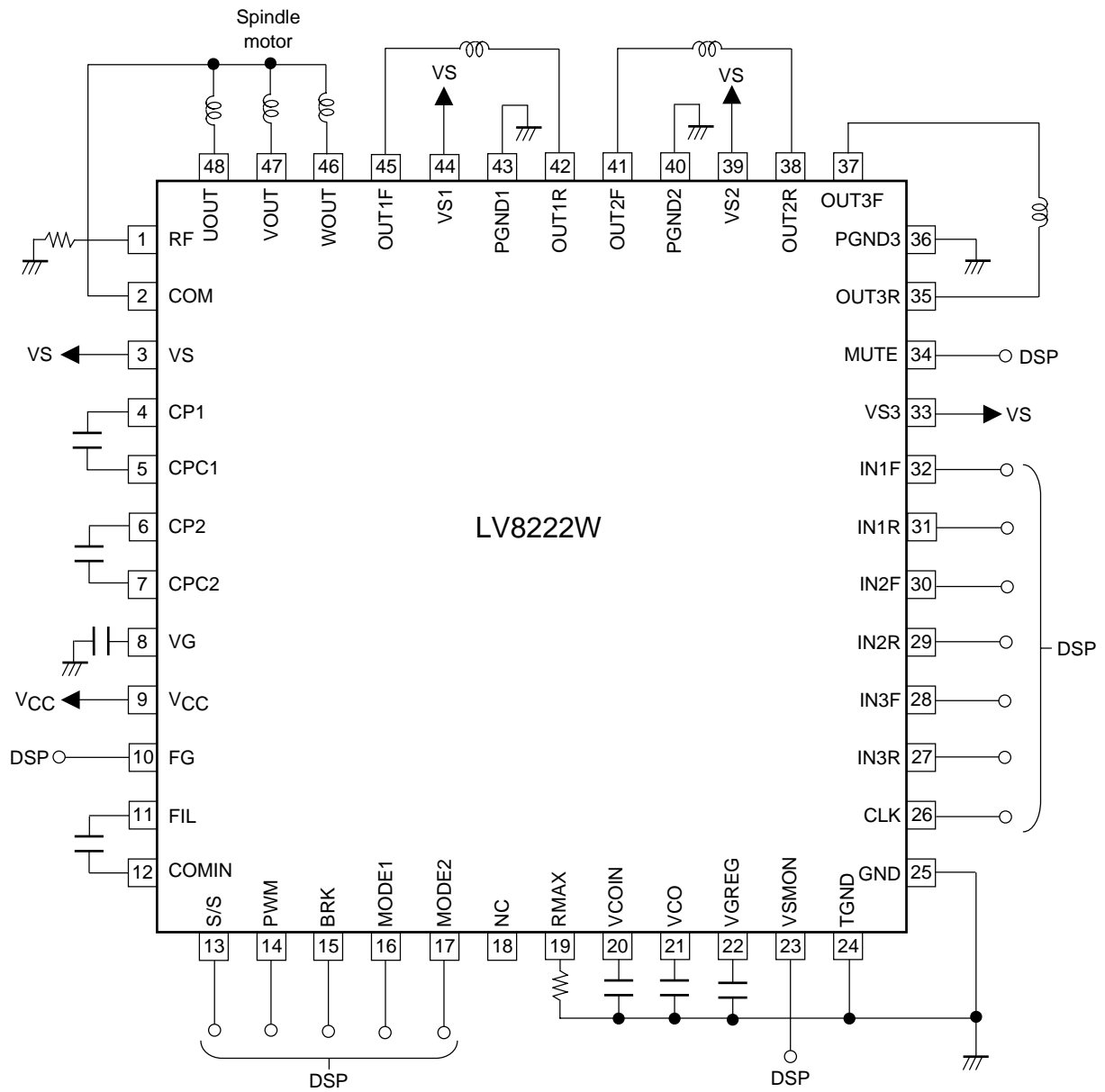
Top view

Block Diagram



LV8222W

Sample Application Circuit



Pin Functions

Pin No.	Pin Name	Pin Description	Equivalent Circuit
1	RF	Output current detection pin. Drive current is detected when a resistor with a small value is connected between this pin and ground.	
3	VS	Spindle motor drive power supply. Insert a capacitor between this pin and ground.	
48 47 46	UOUT VOOUT WOUT	Spindle driver outputs. Connect these pins to the spindle motor.	
2	COM	Connected to the spindle motor COM point.	
11	FIL	Connected to the waveform synthesis filter. Insert a capacitor between this pin and the COMIN pin (pin 12).	
12	COMIN	Position detection comparator differential input. Insert a capacitor between this pin and the FIL pin (pin 11).	
4	CP1	Charge pump step-up pulse output. Insert a capacitor between this pin and the CPC1 pin (pin 5). Leave this pin open when using this circuit as a 2× step-up circuit.	
6	CP2	Charge pump step-up pulse output. Insert a capacitor between this pin and the CPC2 pin (pin 7).	
5	CPC1	Charge pump step-up connection. Insert a capacitor between this pin and the CPC1 pin (pin 5).	
7	CPC2	Charge pump step-up connection. Insert a capacitor between this pin and the CPC2 pin (pin 7).	
8	VG	Charge pump stepped up voltage output. Insert a capacitor between this pin and ground.	

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LV8222W

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Pin No.	Pin Name	Pin Description	Equivalent Circuit
9	VCC	Small-signal system power supply. Insert a capacitor between this pin and ground.	
10	FG	FG pulse output. This pin outputs a three Hall sensor system equivalent pulse signal.	
13	S/S	Spindle motor block start/stop control. A high-level input sets the block to start mode.	
14	PWM	Spindle PWM signal input. A high-level input turns on the transistor.	
15	BRK	Spindle motor brake. A low-level input applies the forward torque and a high-level input switches to brake mode.	
16	MODE1	Spindle PWM frequency switch. The input frequency relationship between the CLK pin (pin 26) and the PWM pin (pin 14) is as follows: High-level input: $f_{PWM} = f_{CLK} / 32$ Low-level input: $f_{PWM} = f_{CLK} / 48$	
17	MODE2	Spindle soft switching characteristic switch. Select low-level if driving noise is an issue and high-level if torque is important.	
26	CLK	System clock input.	
32/31 30/29 28/27	IN1F/R IN2F/R IN3F/R	Actuator H-bridge logic input	
34	MUTE	H-bridge and 3-phase sled muting control. A low-level input goes to the muted state.	
18	NC	NC	
19	RMAX	VCO maximum frequency setting. Insert a resistor between this pin and ground. Reducing the value of that resistor increases the maximum VCO frequency.	

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LV8222W

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Pin No.	Pin Name	Pin Description	Equivalent Circuit
20	VCOIN	VCO control voltage input. Insert a capacitor between this pin and ground.	
21	VCO	VCO oscillator connection. Insert a capacitor between this pin and ground. The VCO oscillator frequency follows the speed of the spindle motor.	
22	VGREG	Pre-drive drive regulator 4V output. Insert a capacitor between this pin and ground.	

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LV8222W

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Pin No.	Pin Name	Pin Description	Equivalent Circuit
23	VSMON	Supply voltage monitor output Outputs 1/2 of the voltage at the VS pin (pin 3). This pin is held low level in standby mode.	
24 25	TGND GND	Small-signal system circuit ground	
33 39 44	VS3 VS2 VS1	H-bridge power supply. Insert capacitors between these pins and ground.	
36 40 43	PGND3 PGND2 PGND1	H bridge output block ground connections	
37/35 41/38 45/42	OUT3F/R OUT2F/R OUT1F/R	H bridge circuit forward/reverse outputs. Connect these pins to the motor coils.	

LV8222W Functional Description and Notes on External Components

The LV8222W is a system driver IC that implements, in a single chip, all the motor driver circuits required for CD and MD players. Incorporating the 3-phase PWM spindle motor driver as well as the sled, focus, and tracking drivers (PWM H-bridge×3 channels), the IC contributes toward set miniaturization, low profiling, and low power dissipation. Since the spindle motor driver uses a direct PWM sensorless drive technique, it achieves high-efficiency motor drive with a minimal number of external components. Read the following notes before designing driver circuits using the LV8222W to design a system with fully satisfactory characteristics.

1. Output Drive Circuit and Speed Control Methods

The LV8222W adopts the synchronous commutation direct PWM drive method to minimize power loss in the output circuits. Low on-resistance DMOS devices (output block high and low on-resistance s: 1.0Ω typ. for the spindle block, 1.5Ω typ. for the actuator block) are used as the output transistors.

The spindle motor driver speed is controlled by BRK and PWM signals provided by an external DSP. The PWM signal controls the sink side transistor. That transistor is switched according to the input duty of the signal input to the PWM pin (pin 14) to control the motor speed. (The sink side transistor is on when the PWM input is high, and off when the PWM input is low.)

2. Soft Switching Circuit

This IC uses variable duty soft switching to minimize motor drive noise.

An excitation current on/off dual-sided soft switching or off soft switching can be selected by the MODE 2 pin (pin 17).

If a motor driving noise is an issue, select excitation current on/off soft switching with the MODE 2 pin set at the low level. If a motor drive torque is important, select off soft switching with the MODE 2 pin set at the high level.

Note that the LV8222W does not use soft switching drive, but instead uses hard switching drive, if it is not supplied with a CLK signal from the DSP. In this operating mode, the CLK signal is provided by an internal oscillator circuit.

3. VCO Circuit Constant

The LV8222W spindle block adopts a sensorless drive technique. Sensorless drive is implemented by detecting the back EMF signal generated by the motor and setting the commutation timing accordingly. Thus the timing control uses the VCO signal. We recommend using the following procedure to determine the values of the VCO circuit's external components.

1) Connect components with provisional values.

Connect a 1.0 μ F capacitor between the VCOIN pin (pin 20) and ground, connect a 68 k Ω resistor between the RMAX pin (pin 19) and ground, and connect a 3300pF capacitor between the VCO pin (pin 21) and ground.

2) Determine the value of the VCO pin (pin 21) capacitor.

Select a value such that the startup time to the target speed is the shortest and such that the variations in startup time are minimized. If the value of this capacitor is too large, the variations in the startup time will be excessive, and if too small, the motor may fail to turn. Since the optimal value of the VCO pin constant differs with the motor characteristics and the startup current, the value of this component must be verified again if the motor used or any circuit specifications are changed.

3) Determine the value of the RMAX pin (pin 19) resistor.

Select a resistor value such that the VCOIN pin voltage is about VCC – 1.0 V or lower with the motor operating at the target maximum speed. If the value of this resistor is too large, the VCOIN pin voltage may rise excessively.

4) Determine the value of the VCOIN pin (pin 20) capacitor.

If the FG output (pin 10) pulse signal becomes unstable at the lowest motor speed that will be used, increase the value of the VCOIN pin capacitor.

4. S/S and MUTE Circuits

The S/S pin (pin 13) functions as the spindle motor driver's start/stop pin; a high-level input specifies that the operation is in the start state. The MUTE pin (pin 34) operates on all driver blocks other than the spindle block; a low-level input mutes these outputs. In the muted state, the corresponding drivers (H bridge) all go to the high-impedance state, regardless of the states of the logic inputs. Since the S/S and MUTE pins operate independently, low-level inputs must be applied to both the S/S and MUTE pins to set the IC to the standby state (power saving mode).

5. Braking Circuit

The BRK pin (pin 15) switches the direction of the torque applied by the spindle motor driver; when a high level is applied to the BRK pin, the driver switches to reverse torque braking mode. When the motor decelerates to an adequately low speed in reverse torque braking mode, the driver switches to short-circuit braking mode to stop the motor. (Note: the IC cannot be set to low-power mode at this time.)

Note that when stopping the motor with the braking function, if this circuit switches to short-circuit braking too quickly and problems such as the motor remaining in motion occur, the value of the resistor connected to the RMAX pin (pin 19) must be reduced. If the motor moves back and forth without stopping and the IC does not switch to short-circuit braking when the speed approaches zero, insert a resistor with a value of a few k Ω at the COM pin. (Caution: Verify that insertion of this resistor does not degrade the startup characteristics.)

6. Note on the CLK and PWM signals

The LV8222W CLK pin (pin 26) is used as the sensorless logic reference clock, for step-up circuit pulse generation, and for other purposes. Therefore, if the CLK signal is supplied from the DSP, it must always be input in start mode. The CLK input signal must have a frequency that is either 32 or 48 times that of the PWM input signal. The MODE1 pin (pin 16) selects the relationship between the CLK and PWM frequencies. If the CLK signal is 32 times the PWM signal, the MODE1 pin must be set high, and if the CLK signal is 48 times the PWM signal, the MODE1 pin must be set low. We recommend that the CLK input frequency be less than 7MHz.

As was mentioned previously in the section on soft switching, if the CLK signal is not supplied by the DSP (the CLK pin is left open or is shorted to ground), the internal oscillator circuit operates and supplies the CLK signal. In this case, the spindle motor drive operation will be hard switching drive.

7. FG Output Circuit

The FG pin (pin 10) is the spindle block FG output. It outputs a pulse signal equivalent to a three Hall sensor FG output. This output has an MOS circuit structure.

8. Spindle Block Position Detection Comparator Circuit

The spindle block position detection comparator circuit is provided to detect the position of the rotor using the back EMF generated when the motor turns. The IC determines the timing with which the output block applies current to the motor based on the position information acquired by this circuit. Startup problems due to comparator input noise can be resolved by inserting a capacitor (about 1000 to 4700pF) between the COMIN pin (pin 12) and the FIL pin (pin 11). Note that if this capacitor is too large, the output commutation timing may be delayed at higher speeds and efficiency may be reduced.

9. Charge Pump Circuit

The LV8222W n-channel DMOS output structure allows it to provide a charge pump based voltage step-up circuit. A voltage V_S+4V of the V_{CC} voltage (Design circuit so that stepped-up voltage (VG) is clamped at about V_S+4V) can be acquired by inserting a capacitor (recommended value: $0.22\mu F$ or larger) between the CP2 and CPC2 pins. We recommend using this circuit with values such that the voltage relationship between the stepped-up voltage (VG) and the motor supply voltage (V_S) is $V_G-V_S \geq 3.5V$. A larger capacitor must be used on the VG pin if the ripple on the stepped-up voltage (VG) results in V_{Gmax} exceeding 9.5V.

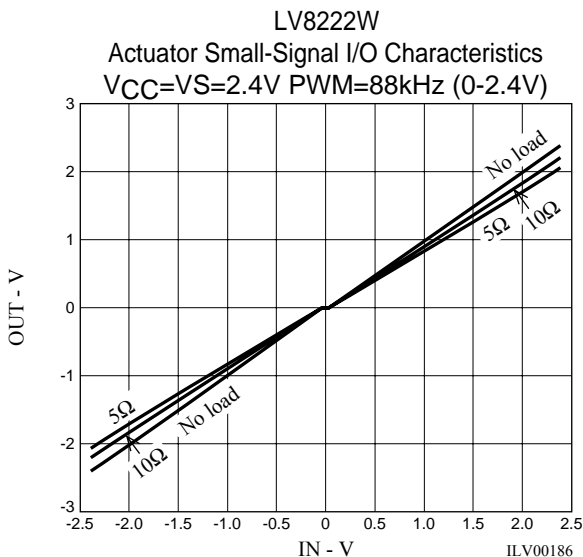
Observe the following points if the VG voltage is supplied from external circuits.

- 1) The VG voltage supplied from the external circuits must not exceed the absolute maximum rating V_{Gmax} .
- 2) The capacitor between the CP1 and CPC1 pins (pin 4 and 5) and between CP2 and CPC2 (pin 6 and 7) are not required.
- 3) The VG voltage must be applied in the correct order. The VG voltage must be applied after the V_{CC} level is applied, and must be cut before the V_{CC} power supply is turned off.
- 4) There is an IC-internal diode between the V_{CC} and VG pins. Therefore, supply voltages such that $V_{CC} > V_G$ must never be applied to this IC.

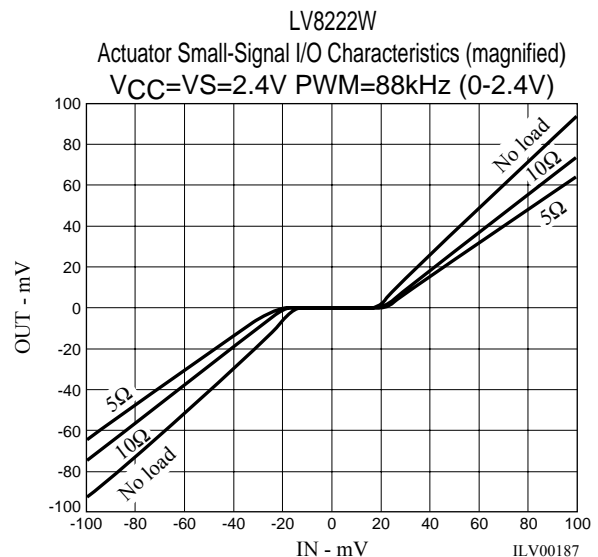
10. Actuator Block

The LV8222W incorporates three H bridge channels for use as actuator drivers for the sled, focus, and tracking systems. The logic input pin circuits incorporates pull-down resistors. A PWM signal is used for control, and the circuit supports synchronous commutation.

The figures below show reference data related to the dead band during control.



The input and output are smoothed with a low-pass filter consisting of a $1.0k\Omega$ resistor and $2.2\mu F$ capacitor.



The input and output are smoothed with a low-pass filter consisting of a $1.0k\Omega$ resistor and $2.2\mu F$ capacitor.

11. Notes on PCB Pattern Design

The LV8222W is a system driver IC implemented in a Bi-DMOS process; the IC chip includes bipolar circuits, MOS logic circuits, and MOS drive circuits integrated on the same chip. As a result, extreme care is required with respect to the pattern layout when designing application circuits.

1) Ground and VCC/VS wiring layout

The LV8222W ground and power supply pins are classified as follows.

Small-signal system ground pins → GND (pin 25), TGND (pin 24)

Large-signal system ground pins → PGND1 (pin 43), PGND2 (pin 40), PGND3 (pin 36)

Small-signal system power supply pin → VCC (pin 9)

Large-signal system power supply pins → VS (pin 3), VS1 (pin 44), VS2 (pin 39), VS3 (pin 33)

A capacitor must be inserted, as close as possible to the IC, between the small-signal system power supply pin (pin 9) and ground pins (pin 25, 26).

The large-signal system ground pins (PGND) must be connected with the shortest possible lines, and furthermore in a manner such that there is no shared impedance with the small-signal system ground lines. Capacitors must also be inserted, as close as possible to the IC, between the large-signal system power supply pins (VS) and the corresponding large-signal system ground pins.

2) Positioning the small-signal system external components

The small-signal system external components that are also connected to ground must be connected to the small-signal system ground with lines that are as short as possible.

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