



# SPN8910

## N-Channel Enhancement Mode MOSFET

### DESCRIPTION

The SPN8910 is the N-Channel logic enhancement mode power field effect transistor which is produced using super high cell density DMOS trench technology. The SPN8910 has been designed specifically to improve the overall efficiency of DC/DC converters using either synchronous or conventional switching PWM controllers. It has been optimized for low gate charge, low  $R_{DS(ON)}$  and fast switching speed.

### FEATURES

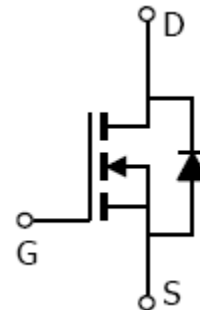
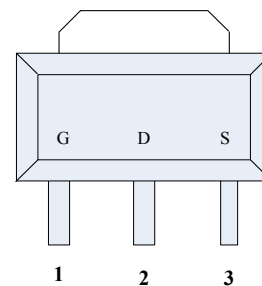
- ◆ 100V/2A,  $R_{DS(ON)} = 320m\Omega @ V_{GS} = 10V$
- ◆ High density cell design for extremely low  $R_{DS(ON)}$
- ◆ Exceptional on-resistance and maximum DC current capability
- ◆ SOT-89 package design

### APPLICATIONS

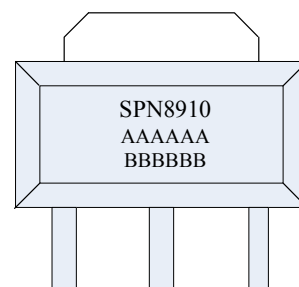
- High Frequency Small Power Switching for MB/NB/VGA
- Network DC/DC Power System
- Load Switch

### PIN CONFIGURATION

#### SOT-89



### PART MARKING





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### PIN DESCRIPTION

Pin	Symbol	Description
1	G	Gate
2	D	Drain
3	S	Source

### ORDERING INFORMATION

Part Number	Package	Part Marking
SPN8910S89RGB	SOT-89	SPN8910
SPN8910S89TGB	SOT-89	SPN8910

※ SPN8910S89RGB : Tape Reel ; Pb – Free ; Halogen - Free

※ SPN8910S89TGB : Tube ; Pb – Free ; Halogen - Free

### ABSOLUTE MAXIMUM RATINGS

(TA=25°C Unless otherwise noted)

Parameter	Symbol	Typical	Unit	
Drain-Source Voltage	V <sub>DSS</sub>	100	V	
Gate –Source Voltage	V <sub>GSS</sub>	±20	V	
Continuous Drain Current(T <sub>J</sub> =150°C)	I <sub>D</sub>	T <sub>A</sub> =25°C	2.2	A
		T <sub>A</sub> =70°C	1.7	
Pulsed Drain Current	I <sub>DM</sub>	5.5	A	
Power Dissipation	P <sub>D</sub>	1.5	W	
Operating Junction Temperature	T <sub>J</sub>	-55/150	°C	
Storage Temperature Range	T <sub>STG</sub>	-55/150	°C	
Thermal Resistance-Junction to Ambient	R <sub>θJA</sub>	85	°C/W	



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### ELECTRICAL CHARACTERISTICS

( $T_A=25^\circ\text{C}$  Unless otherwise noted)

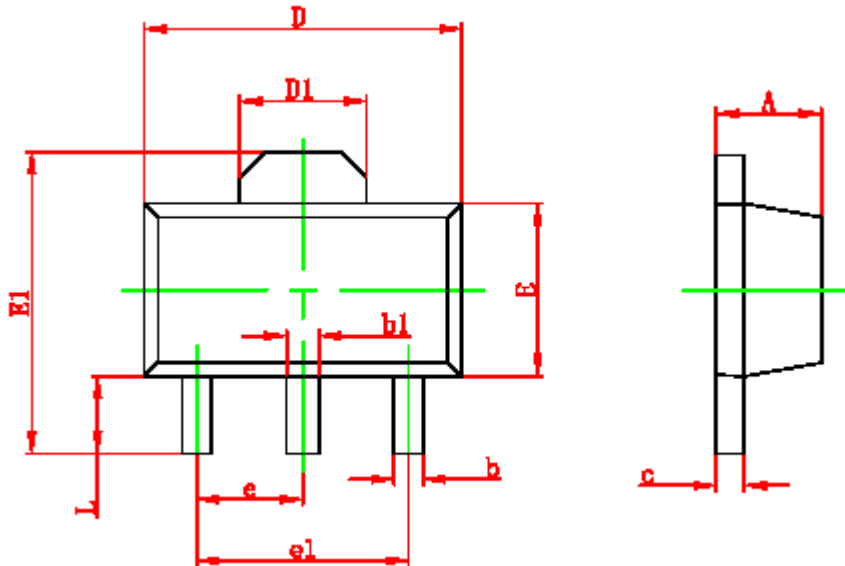
Parameter	Symbol	Conditions	Min.	Typ	Max.	Unit
<b>Static</b>						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	$V_{GS}=0V, I_D=250\mu A$	100			V
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS}=V_{GS}, I_D=250\mu A$	1	2.0	2.5	
Gate Leakage Current	$I_{GSS}$	$V_{DS}=0V, V_{GS}=\pm 20V$			$\pm 100$	nA
Zero Gate Voltage Drain Current	$I_{DSS}$	$V_{DS}=80V, V_{GS}=0V$			1	uA
		$V_{DS}=80V, V_{GS}=0V$ $T_J=55^\circ\text{C}$			5	
On-State Drain Current	$I_{D(on)}$	$V_{DS}\geq 5V, V_{GS}=10V$	2.2			A
Drain-Source On-Resistance	$R_{DS(on)}$	$V_{GS}=10V, I_D=2A$		0.30	0.32	$\Omega$
		$V_{GS}=4.5V, I_D=1A$		0.31	0.34	$\Omega$
Forward Transconductance	$g_{fs}$	$V_{DS}=5V, I_D=2A$		2.4		S
Diode Forward Voltage	$V_{SD}$	$I_S=1A, V_{GS}=0V$			1.2	V
<b>Dynamic</b>						
Total Gate Charge	$Q_g$	$V_{DS}=50V, V_{GS}=10V$ $I_D=2A$		9	13	nC
Gate-Source Charge	$Q_{gs}$			2		
Gate-Drain Charge	$Q_{gd}$			1.4		
Input Capacitance	$C_{iss}$	$V_{DS}=15V, V_{GS}=0V$ $f=1\text{MHz}$		508		pF
Output Capacitance	$C_{oss}$			29		
Reverse Transfer Capacitance	$C_{rss}$			16.5		
Turn-On Time	$t_{d(on)}$	$V_{DD}=50V, I_D=2A,$ $V_{GEN}=10V, R_G=3.3\Omega$		2		nS
	$t_r$			21.5		
Turn-Off Time	$t_{d(off)}$			11.2		
	$t_f$			18.8		



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### SOT-89 PACKAGE OUTLINE



Symbol	Dimensions in Millimeters		Dimensions in Inches	
	Min	Max	Min	Max
A	1.400	1.600	0.055	0.063
b	0.320	0.520	0.013	0.020
b1	0.400	0.580	0.016	0.023
c	0.350	0.440	0.014	0.017
D	4.400	4.600	0.173	0.181
D1	1.550 REF.		0.061 REF.	
E	2.300	2.600	0.091	0.102
E1	3.940	4.250	0.155	0.167
e	1.500 TYP.		0.060 TYP.	
e1	3.000 TYP.		0.118 TYP.	
L	0.900	1.200	0.035	0.047



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