S1C17F13

EPSON
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16-bit Single Chip Microcontroller for Active EPD

■ DESCRIPTIONS

The S1C17F13 is an ultra low-power MCU equipped with a display memory and an EPD timing controller to send display data for using the active EPD panels. This IC includes the synchronous serial interface, parallel interface, UART, and I2C to communicate with an EPD panel and other devices. This IC allows measurement of various environmental conditions such as a temperature and humidity measurement using the R/F converter, and a supply voltage measurement using the supply voltage detector and brownout reset circuits.

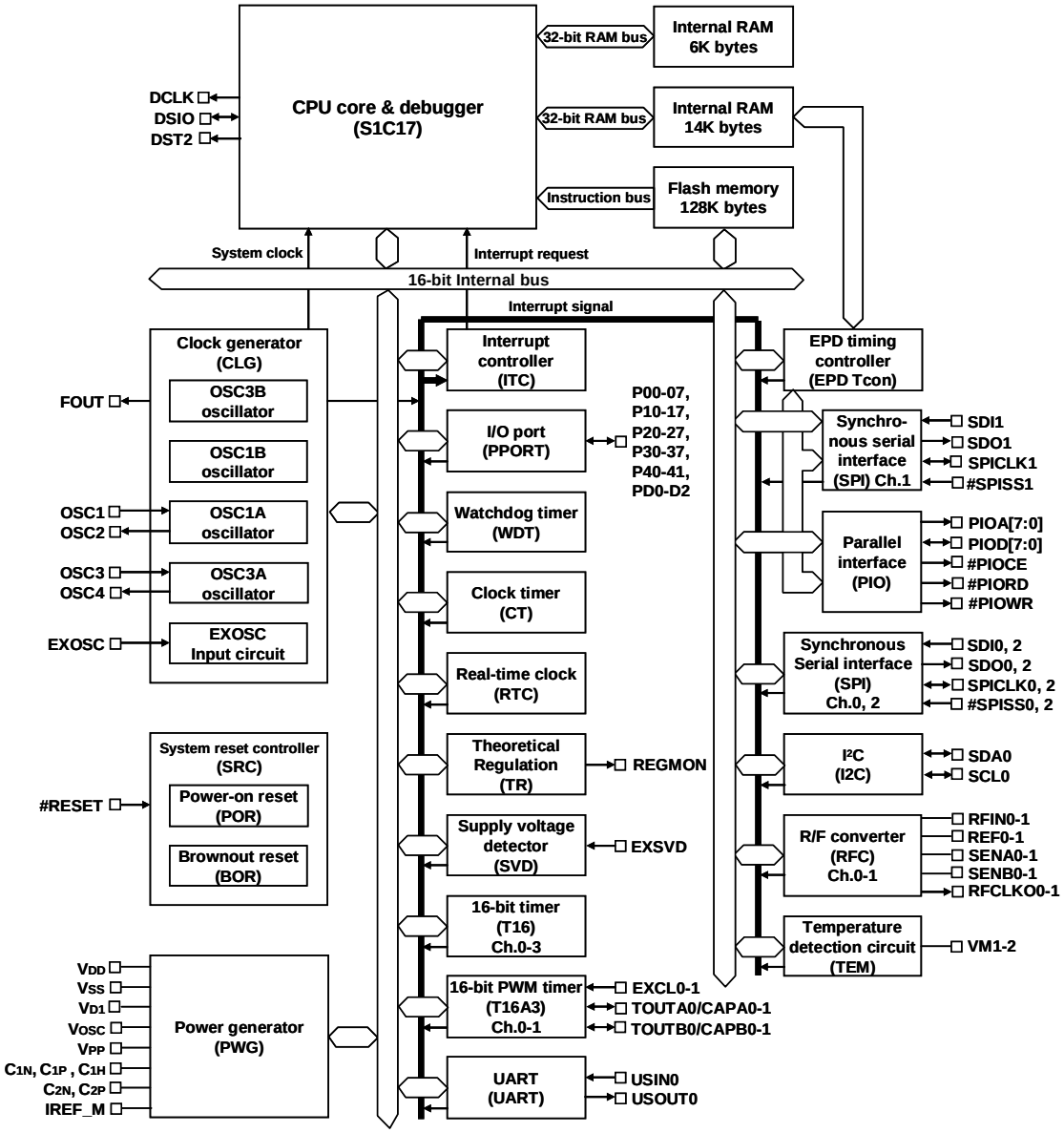
■ FEATURES

CPU	
CPU core	Seiko Epson original 16-bit RISC CPU core S1C17
Multiplier/Divider (COPRO)	16-bit × 16-bit multiplier
	16-bit × 16-bit + 32-bit multiply and accumulation unit
	16-bit ÷ 16-bit divider
Other	On-chip debugger
Embedded Flash memory	
Capacity	128K bytes (for both instructions and data) *1
Erase/program count	50 times (min.) * Programming by the debugging tool ICDmini
Other	Security function to protect from reading/programming by ICDmini
	On-board programming function using ICDmini
	Embedded Flash voltage booster to generate the Flash erasing/programming voltage
Embedded RAM	
Capacity	6K bytes (area accessed by CPU only)
	14K bytes (area accessed by CPU and EPD Tcon)
Clock generator (CLG)	
System clock source	5 sources (OSC3B, OSC3A, OSC1B, OSC1A, and EXOSC)
System clock frequency (operating frequency)	20 MHz (max.)
OSC3B internal high-speed oscillator circuit (boot clock source)	20/16/12/8 MHz (typ.) selectable via software
OSC1B internal low-speed oscillator circuit	32 kHz (typ.)
OSC3A high-speed oscillator circuit	20 MHz (max.) crystal or ceramic oscillator circuit
OSC1A low-speed oscillator circuit	32.768 kHz (typ.) crystal oscillator circuit
EXOSC clock input	20 MHz (max.) square or sine wave input
Other	Configurable system clock division ratio
	Configurable system clock (except for OSC1A and OSC1B) used at wake up from SLEEP state
	Operating clock frequency for the CPU and all peripheral circuits is selectable.
I/O port (PPORT)	
Number of general-purpose I/O ports	37 bits (max.) (Pins are shared with the peripheral I/O.)
Number of input interrupt ports	8 bits
Other	All pins contain a pull-up/down resistor that can be enabled/disabled via software
	16 bits contain an interrupt function and a chattering filter function.
Display control	
EPD timing controller (EPD Tcon)	Controls display on the active-matrix EPD via the embedded SPI or PIO.
	Includes a display data read function from the embedded RAM (area for both CPU and EPD Tcon).
	Can be controlled with the dedicated API library.
Communication interfaces	
UART (UART)	1 channel
	IrDA1.0 supported
	Embedded baud-rate generator
Synchronous serial interface (SPI)	3 channels
	Configurable as the communication interface for EPD Tcon (SPI Ch.1)
I^2C (I2C)	1 channel
	Master and slave operations supported
	Embedded baud-rate generator
Parallel interface (PIO)	Address length: 8 bits (max.)
	Data width: 8 bits (max.)
	Control signals: #CE, #RD, #WR

	Configurable as the communication interface for EPD Tcon
Timers	
Watchdog timer (WDT)	1 channel
	Generates NMI or watchdog timer reset.
16-bit timer (T16)	4 channels
	Generates the SPI master clocks. (Ch.1 to Ch.3)
Clock timer (CT)	1 channel
	128–1 Hz counter
Real-time clock (RTC)	Hour, minute, and second counters
Theoretical regulation function (TR)	Time adjustment function in -31/32,768 to +32/32,768 second units (applied to T16A3, CT, and RTC clocks)
	Supports correction value alteration according to temperature variations.
16-bit PWM timer (T16A3)	2 channels
	PWM output, event counter, and count capture functions
Supply voltage detector (SVD)	
Detection level	19 values (1.8 to 3.6 V)
Other	Intermittent operation mode
	Generates an interrupt or reset according to the detection level evaluation.
R/F converter (RFC)	
Conversion method	CR oscillation type with 24-bit counters
Number of conversion channels	2 channels (Up to four sensors can be connected.)
Supported sensors	DC-bias resistive sensors and AC-bias resistive sensors
Temperature detection circuit (TEM)	
Resolution/accuracy	1 °C steps, ±5 °C accuracy
Reset	
#RESET pin	Reset when the reset pin is set to low.
Power-on reset	Reset at power-on.
Brownout reset	Reset when brownout (VDD = 1.45 V typ.) is detected.
Key entry reset	Reset when the P00 to P01/P02/P03 keys are pressed simultaneously (can be enabled/ disabled using a register).
Watchdog timer reset	Reset when the watchdog timer overflows (can be enabled/disabled using a register).
Supply voltage detector reset	Reset when the supply voltage detector detects the set voltage level (can be enabled/ disabled using a register).
Interrupt	
Non-maskable interrupt	4 systems (Reset, address misaligned interrupt, debug, NMI)
Programmable interrupt	External interrupt: 1 system (8 levels)
	Internal interrupt: 19 systems (8 levels)
Power supply voltage	
VDD operating voltage	2.0 to 3.6 V
Operating temperature	
Operating temperature range	-20 to 70 °C
Current consumption	
SLEEP mode	0.35 µA OSC1 = OFF, RTC = OFF, OSC3B = OFF, OSC3A = OFF
HALT mode	0.78 µA OSC1 = 32 kHz (OSC1A), RTC = OFF, OSC3B = OFF, OSC3A = OFF
	0.80 µA OSC1 = 32 kHz (OSC1A), RTC = ON, OSC3B = OFF, OSC3A = OFF
RUN mode	11.9 µA OSC1 = 32 kHz (OSC1A), RTC = OFF, OSC3B = OFF, OSC3A = OFF
	5.43 mA OSC1 = OFF, RTC = OFF, OSC3B = OFF, OSC3A = 20 MHz ceramic
	5.5 mA OSC1 = OFF, RTC = OFF, OSC3B = 20 MHz, OSC3A = OFF
Shipping form	
1	TQFP13-64pin (Lead pitch: 0.5 mm)
2	Chip (Pad pitch: 90 µm)

*1 When using the EPD timing controller (EPD Tcon), an area for storing the timing parameters must be allocated in the Flash memory. When using the internal Flash voltage booster as the Flash programing power supply, an area for storing the control program must be allocated in the Flash memory.

■ BLOCK DIAGRAM



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