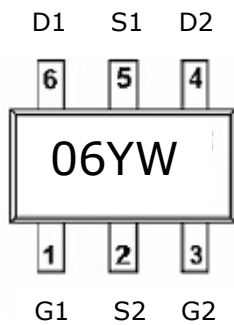


**DESCRIPTION**

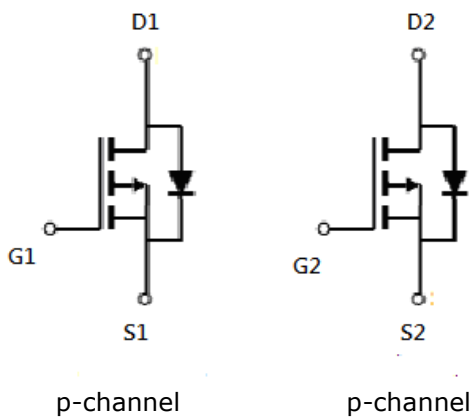
The STC6506 is the dual P-Channel enhancement mode power field effect transistor which is produced using high cell density, DMOS trench technology. This high density process is especially tailored to minimize on-state resistance and provide superior switching performance. These devices are particularly suited for low voltage application, such as notebook computer power management and other battery powered circuits where high-side switching, low in-line power loss, and resistance to transients are needed.

**PIN CONFIGURATION  
TSOP-6**


**Y: Year**  
**A: Produces Code**

**FEATURE**

- ◆ -30V/-2.8A,  $R_{DS(ON)}=105\text{mohm@VGS}=-10\text{V}$
- ◆ -30V/-2.5A,  $R_{DS(ON)}=135\text{mohm@VGS}=-4.5\text{V}$
- ◆ Super high density cell design for extremely low  $R_{DS(ON)}$
- ◆ Exceptional an-resistance and maximum DC current capability
- ◆ TSOP-6P package design





**STP6506**  Lead-free

Dual P Channel Enhancement Mode MOSFET  
-2.8A

**ABSOLUTE MAXIMUM RATINGS** (Ta = 25°C Unless otherwise noted )

Parameter		Symbol	Typical		Unit
Drain-Source Voltage		V <sub>DSS</sub>	-30		V
Gate-Source Voltage		V <sub>GSS</sub>	±20		V
Continuous Drain Current (T <sub>J</sub> =150°C)	T <sub>A</sub> =25°C	I <sub>D</sub>	-2.8		A
	T <sub>A</sub> =70°C		-2.1		
Pulsed Drain Current		I <sub>DM</sub>	-8		A
Continuous Source Current (Diode Conduction)		I <sub>S</sub>	-1.4		A
Power Dissipation	T <sub>A</sub> =25°C	P <sub>D</sub>	1.15		W
	T <sub>A</sub> =70°C		0.75		
Operation Junction Temperature		T <sub>J</sub>	-55/150		°C
Storage Temperature Range		T <sub>STG</sub>	-55/150		°C
Thermal Resistance-Junction to Ambient	T ≤ 10sec	R <sub>θJA</sub>	50	52	°C/W
	Steady State		90	90	



**STP6506**  Lead-free

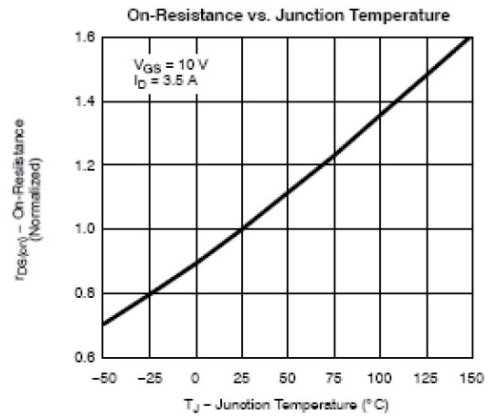
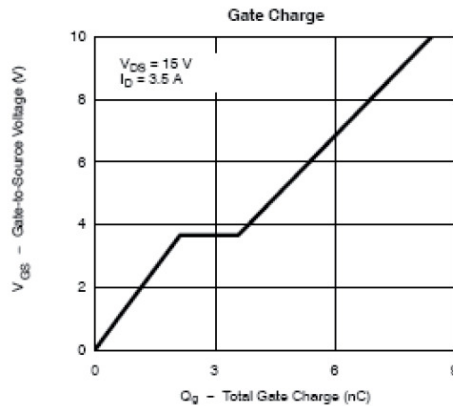
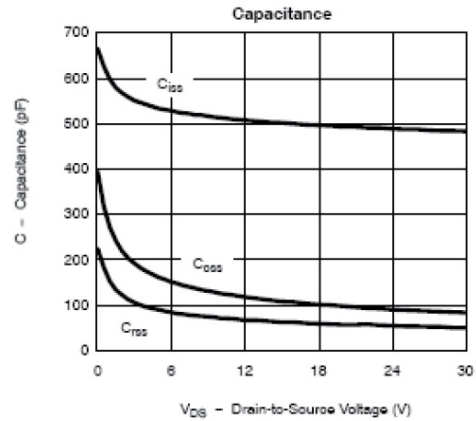
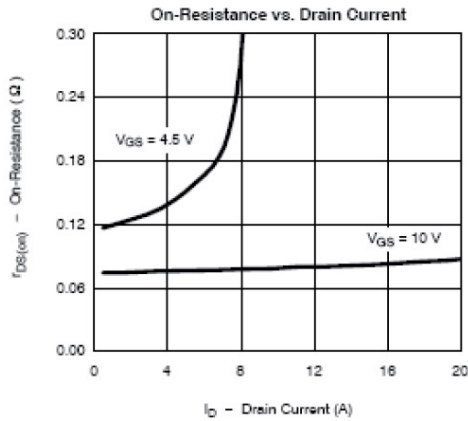
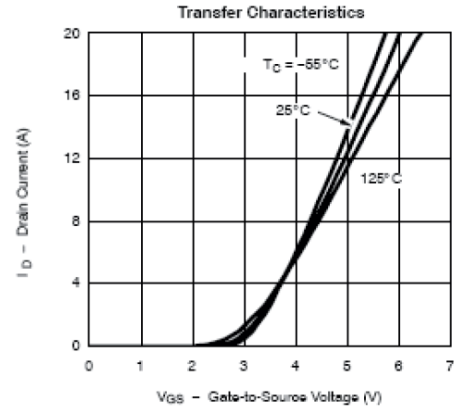
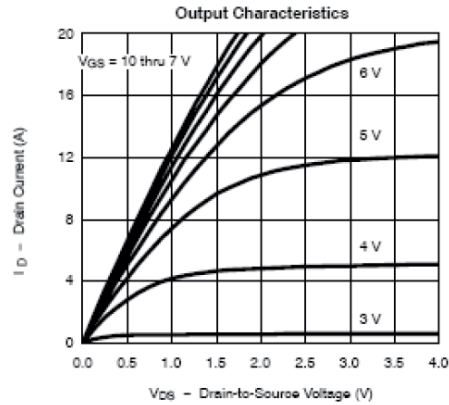
Dual P Channel Enhancement Mode MOSFET  
-2.8A

**ELECTRICAL CHARACTERISTICS** ( Ta = 25°C Unless otherwise noted )

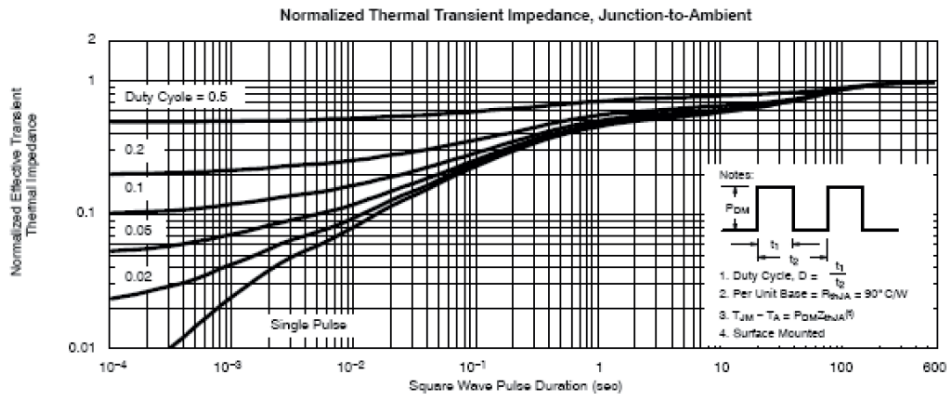
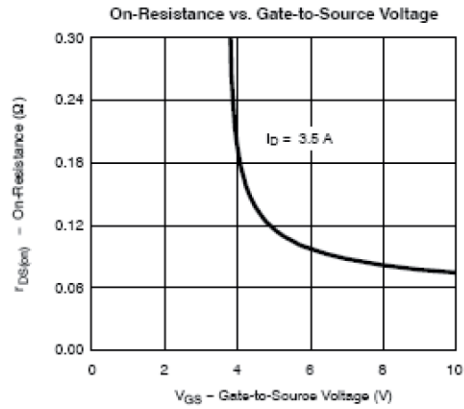
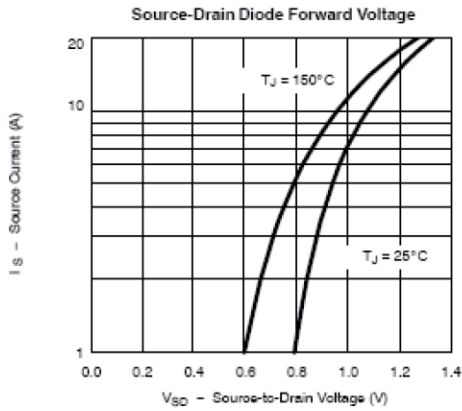
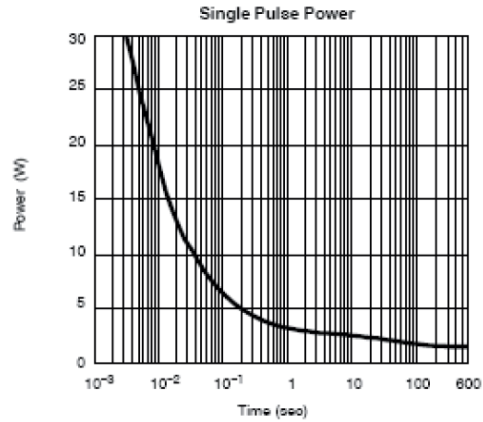
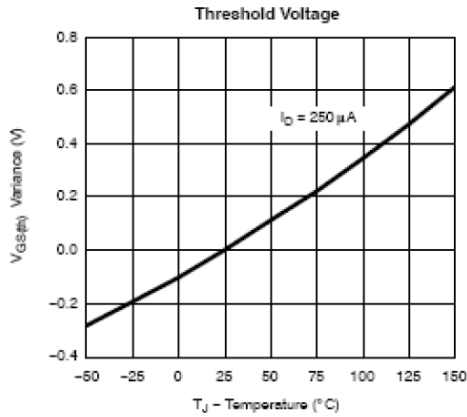
Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	$V_{GS}=0V, I_D=-250\mu A$	-30			V
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS}=V_{GS}, I_D=-250\mu A$	-1		-3	V
Gate Leakage Current	$I_{GSS}$	$V_{DS}=0V, V_{GS}=\pm 20V$			$\pm 100$	nA
Zero Gate Voltage Drain Current	$I_{DSS}$	$V_{DS}=-24V, V_{GS}=0V$			-1	$\mu A$
		$V_{DS}=-24V, V_{GS}=0V$ $T_J=55^\circ C$			-10	
On-State Drain Current	$I_{D(on)}$	$V_{DS}\leq -5V, V_{GS}=-10V$	-6			A
Drain-source On-Resistance	$R_{DS(on)}$	$V_{GS}=-10V, I_D=-2.8A$		0.088	0.103	$\Omega$
		$V_{GS}=-4.5V, I_D=-2.5A$		0.110	0.132	
Forward Transconductance	$g_{fs}$	$V_{DS}=-10V, I_D=-2.8A$		-4.0		S
Diode Forward Voltage	$V_{SD}$	$I_S=-1.2A, V_{GS}=0V$		-0.8	-1.2	V

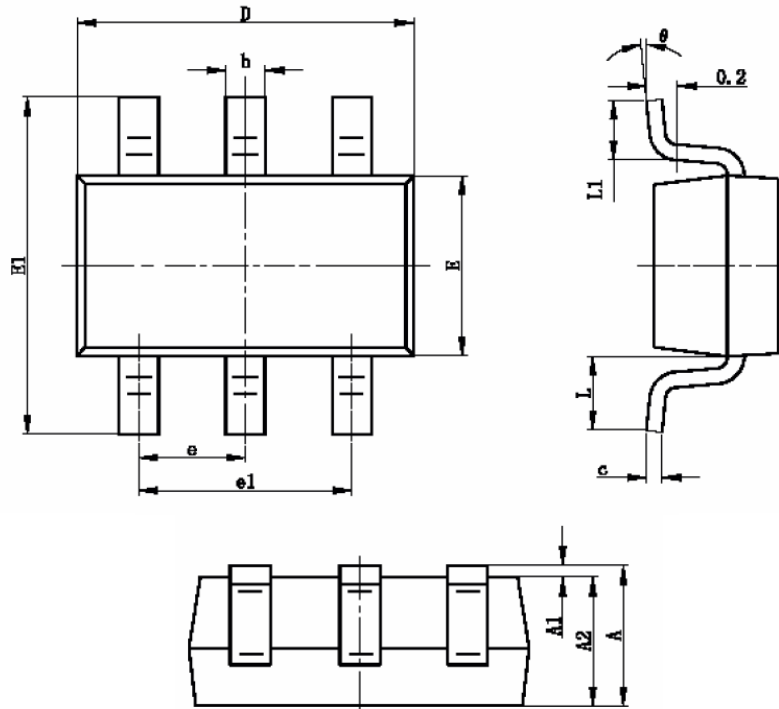
**Dynamic**

Total Gate Charge	$Q_g$	$V_{DS}=-15V, V_{GS}=-10V,$ $V_{DS}=-1.7A$		5.8	10	nC
Gate-Source Charge	$Q_{gs}$			0.8		
Gate-Drain Charge	$Q_{gd}$			1.5		
Input Capacitance	$C_{iss}$	$V_{DS}=-15V, V_{GS}=-0V,$ $f=1MHz$		226		
Output Capacitance	$C_{oss}$			87		
Reverse Transfer Capacitance	$C_{rss}$			19		
Turn-On Time	$T_{d(on)}$	$V_{DD}=-15V, R_L=15\Omega,$ $V_{GEN}=-10V, R_G=6\Omega$ $I_D=1.0A$		9	20	nS
	$t_r$			9	20	
Turn-Off Time	$T_{d(off)}$			18	35	
	$t_f$			6	20	

**TYPICAL CHARACTERISTICS**


**TYPICAL CHARACTERISTICS**



**TSOP-6 PACKAGE OUTLINE**


Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	1.050	1.250	0.041	0.049
A1	0.000	0.100	0.000	0.004
A2	1.050	1.150	0.041	0.045
b	0.300	0.400	0.012	0.016
c	0.100	0.200	0.004	0.008
D	2.820	3.020	0.111	0.119
E	1.500	1.700	0.059	0.067
E1	2.650	2.950	0.104	0.116
e	0.950TYP		0.037TYP	
e1	1.800	2.000	0.071	0.079
L	0.700REF		0.028REF	
L1	0.300	0.600	0.012	0.024
θ	0°	8°	0°	8°