SONY

CXK5972P/J -15/20

8,192-word × 9-bit High Speed CMOS Static RAM

Description

The CXK5972P/J is a high speed CMOS static RAM which consists of 8,192-word × 9-bit. It operates at 15ns and 20ns high speed from 5V single power supply.

Features

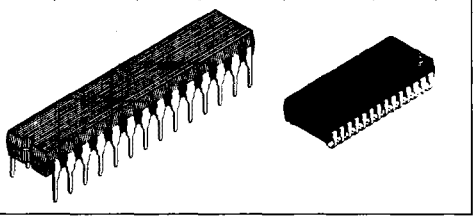
- High speed, low power consumption :

	Access time (Max.)	Power consumption (Typ., Cycle=Min.)
CXK5972P/J-15	15ns	400mW
CXK5972P/J-20	20ns	325mW

- Single +5V power supply : 5V ± 10%
- Fully static memory...No clock or timing strobe required.
- Equal access and cycle time.
- Common data input and output : three state output.
- Directly TTL compatible all inputs and outputs.
- Available in 28 pin 300mil DIP, 300mil SOJ package.

CXK5972P
28 pin DIP (Plastic)

CXK5972J
28 pin SOJ (Plastic)



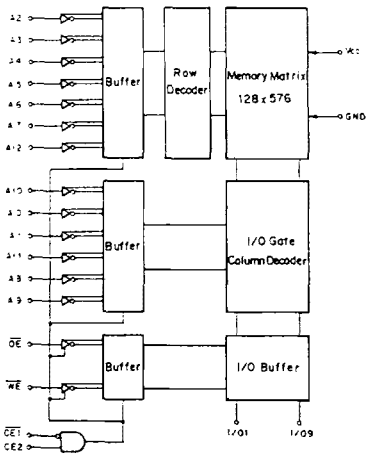
Function

8,192-word × 9-bit static RAM

Structure

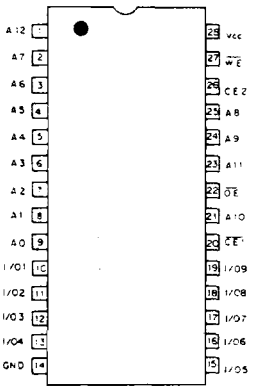
Silicon gate CMOS IC

Block Diagram



Pin Configuration

(Top View)



Pin Description

Symbol	Description
A0 to A12	Address input
I/O1 to I/O9	Data input/output
$\overline{CE1}$, CE2	Chip enable 1, 2 input
$\overline{WE}$	Write enable input
$\overline{OE}$	Output enable input
V_{CC}	+5V power supply
GND	Ground

PE89Y51A18 – ST

Absolute Maximum Ratings (Ta = 25℃, GND = 0V)

Item	Symbol	Rating	Unit
Supply voltage	V_{CC}	− 0.5* to + 7.0	V
Input voltage	V_{IN}	− 0.5* to V_{CC} + 0.5	V
Input and output voltage	$V_{I/O}$	− 0.5* to V_{CC} + 0.5	V
Allowable power dissipation	P_D	1.0	W
Operating temperature	Topr	0 to + 70	℃
Storage temperature	Tstg	− 55 to + 150	℃
Soldering temperature • time	Tsolder	260 • 10	℃ • sec

* V_{CC}, V_{IN}, $V_{I/O}$ = − 3.5V Min. for pulse width less than 20ns.

Truth Table

$\overline{CE1}$	CE2	$\overline{OE}$	$\overline{WE}$	Mode	I/O1 to I/O9	V_{CC} Current
H	X	X	X	Not selected	High Z	I_{SB1}, I_{SB2}
X	L	X	X	Not selected	High Z	I_{SB1}, I_{SB2}
L	H	H	H	Output disable	High Z	I_{CC1}, I_{CC2}
L	H	L	H	Read	Data out	I_{CC1}, I_{CC2}
L	H	X	L	Write	Data in	I_{CC1}, I_{CC2}

X : "H" or "L"

DC Recommended Operating Conditions (Ta = 0 to + 70℃, GND = 0V)

Item	Symbol	Min.	Typ.	Max.	Unit
Supply voltage	V_{CC}	4.5	5.0	5.5	V
Input high voltage	V_{IH}	2.2	—	V_{CC} + 0.3	V
Input low voltage	V_{IL}	− 0.3*	—	0.8	V

* V_{IL} = − 3.0V Min. for pulse width less than 20ns.

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Electrical Characteristics

• DC and operating characteristics

(Vcc = 5V ± 10%, GND = 0V, Ta = 0 to +70°C)

Item	Symbol	Test conditions		Min.	Typ.*	Max.	Unit
Input leakage current	I_{LI}	V_{IN} = GND to Vcc		−1	—	1	μA
Output leakage current	I_{LO}	$V_{I/O}$ = GND to Vcc, $\overline{CE1}$ = V_{IH} or CE2 = V_{IL} or $\overline{OE}$ = V_{IH} or $\overline{WE}$ = V_{IL}		−1	—	1	μA
Operating power supply current	I_{CC1}	$\overline{CE1}$ = V_{IL}, CE2 = V_{IH}, V_{IN} = V_{IH} or V_{IL}, I_{OUT} = 0mA		—	—	—	
Average operating current	I_{CC2}	Cycle = Min., Duty = 100%, I_{OUT} = 0mA	−15	—	80	120	mA
			−20	—	65	100	
Standby current	I_{SB1}	$\overline{CE1}$ ≧ Vcc − 0.2V or CE2 ≦ 0.2V, V_{IN} ≧ Vcc − 0.2V or V_{IN} ≦ 0.2V		—	—	1	mA
	I_{SB2}	$\overline{CE1}$ = V_{IH} or CE2 = V_{IL}, V_{IN} = V_{IH}/V_{IL}, Cycle = Min.		—	15	25	mA
Output high voltage	V_{OH}	I_{OH} = −4.0mA		2.4	—	—	V
Output low voltage	V_{OL}	I_{OL} = 8.0mA		—	—	0.4	V

* Vcc = 5V, Ta = 25°C

I/O capacitance

(Ta = 25°C, f = 1MHz)

Item	Symbol	Test conditions	Min.	Max.	Unit
Input capacitance	C_{IN}	V_{IN} = 0V	—	6	pF
I/O capacitance	$C_{I/O}$	$V_{I/O}$ = 0V	—	6	pF

Note) This parameter is sampled and is not 100% tested.

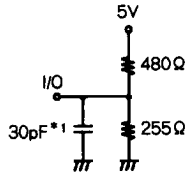
AC characteristics

• AC test conditions

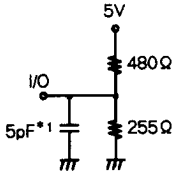
(Vcc = 5V ± 10%, Ta = 0 to +70°C)

Item	Conditions
Input pulse high level	V_{IH} = 3.0V
Input pulse low level	V_{IL} = 0V
Input rise time	tr = 3ns
Input fall time	tf = 3ns
Input and output reference level	1.5V
Output load conditions	Fig. 1

Output Load (1)



Output Load (2)*2



*1. including scope and jig capacitance
*2. for t_{LZ1}, t_{LZ2}, t_{OLZ}, t_{HZ1}, t_{HZ2}, t_{OHZ}, t_{OW}, t_{WHZ}

Fig. 1

• **Read cycle**

Item	Symbol	−15		−20		Unit
		Min.	Max.	Min.	Max.	
Read cycle time	t_{RC}	15	—	20	—	ns
Address access time	t_{AA}	—	15	—	20	ns
Chip enable access time ($\overline{CE1}$)	t_{CO1}	—	15	—	20	ns
Chip enable access time (CE2)	t_{CO2}	—	15	—	20	ns
Output enable to output valid	t_{OE}	—	8	—	10	ns
Output hold from address change	t_{OH}	5	—	5	—	ns
Chip enable to output in low Z ($\overline{CE1}$, CE2)	t_{LZ1}*, t_{LZ2}*	5	—	5	—	ns
Output enable to output in low Z ($\overline{OE}$)	t_{OLZ}*	2	—	2	—	ns
Chip disable to output in high Z ($\overline{CE1}$, CE2)	t_{HZ1}*, t_{HZ2}*	0	8	0	9	ns
Output disable to output in high Z ($\overline{OE}$)	t_{OHZ}*	0	7	0	8	ns
Chip enable to power up time ($\overline{CE1}$, CE2)	t_{PU}	0	—	0	—	ns
Chip disable to power down time ($\overline{CE1}$, CE2)	t_{PD}	—	15	—	20	ns

* Transition is measured ± 200mV from steady voltage with specified loading in Fig. 1-(2). This parameter is sampled and is not 100% tested.

• **Write cycle**

Item	Symbol	−15		−20		Unit
		Min.	Max.	Min.	Max.	
Write cycle time	t_{WC}	15	—	20	—	ns
Address valid to end of write	t_{AW}	12	—	14	—	ns
Chip enable to end of write	t_{CW}	12	—	14	—	ns
Data to write time overlap	t_{DW}	9	—	10	—	ns
Data hold from write time	t_{DH}	0	—	0	—	ns
Write pulse width	t_{WP}	11	—	13	—	ns
Address set up time	t_{AS}	0	—	0	—	ns
Write recovery time ($\overline{WE}$)	t_{WR}	0	—	0	—	ns
Write recovery time ($\overline{CE1}$, CE2)	t_{WR1}	0	—	0	—	ns
Output active from end of write	t_{OW}*	5	—	5	—	ns
Write to output in high Z	t_{WHZ}*	0	7	0	9	ns

* Transition is measured ± 200mV from steady voltage with specified loading in Fig. 1-(2). This parameter is sampled and is not 100% tested.

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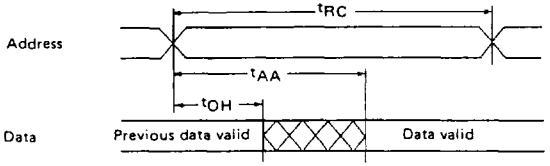
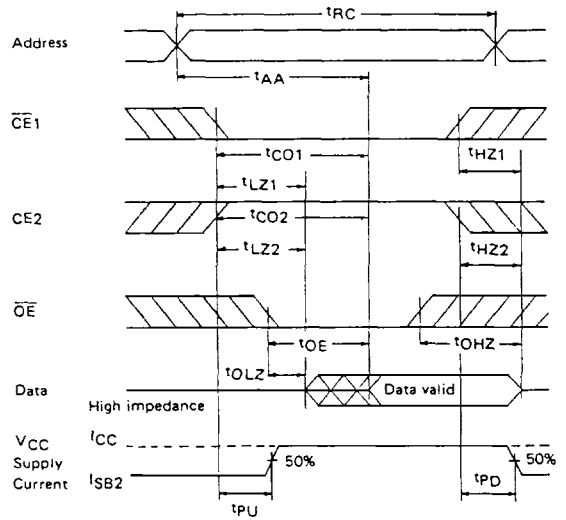
Timing Waveform

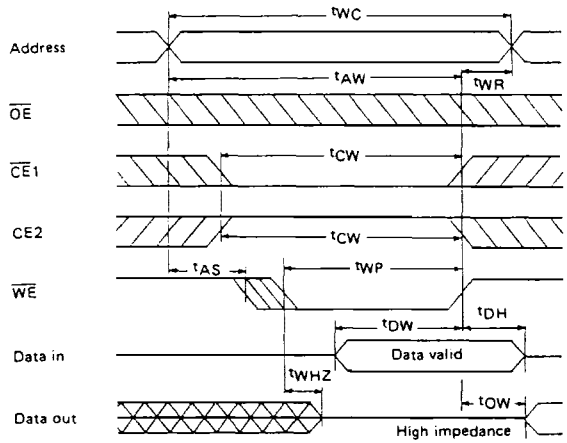
• Read cycle (1) : $\overline{CE1}$ = $\overline{OE}$ = V_{IL}, CE2 = V_{IH}, $\overline{WE}$ = V_{IH}



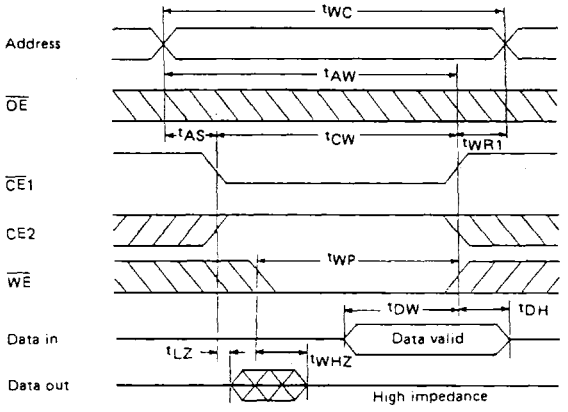
• Read cycle (2) : $\overline{WE}$ = V_{IH}



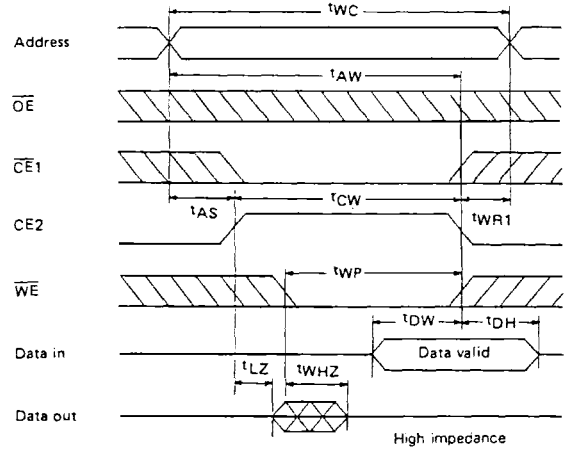
• Write cycle (1) : $\overline{WE}$ control



• Write cycle (2) : $\overline{CE1}$ control



• Write cycle (3) : CE2 control



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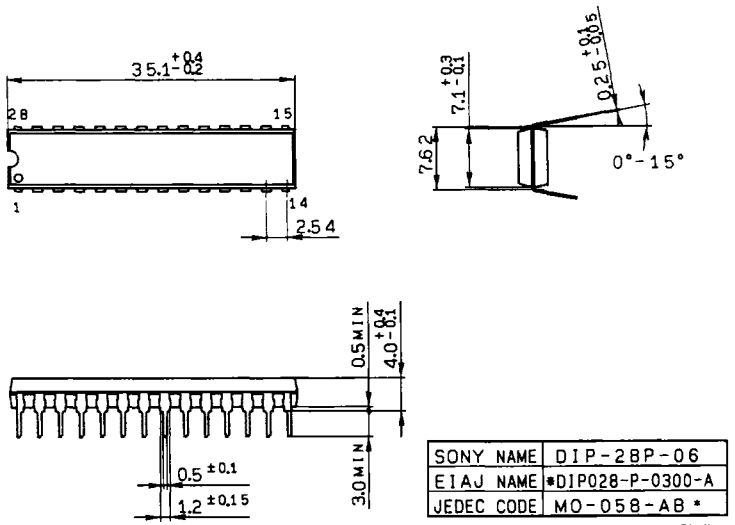
* During I/O pins are in the output state, the data input signals of opposite phase to the output must not be applied.

Package Outline Unit : mm

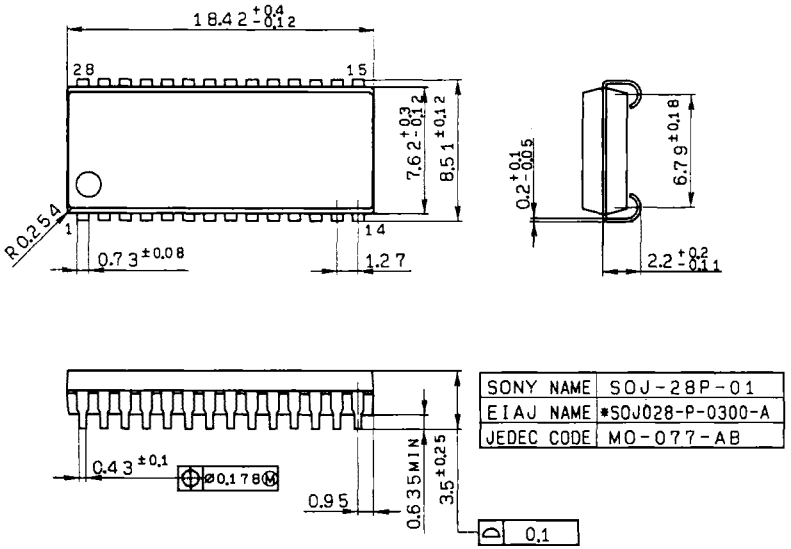
CXK5972P 28pin DIP (Plastic) 300mil 2.0g



SONY NAME	DIP-28P-06
EIAJ NAME	*DIP028-P-0300-A
JEDEC CODE	MO-058-AB *

* (Similar)

CXK5972J 28pin SOJ (Plastic) 300mil 0.8g



SONY NAME	SOJ-28P-01
EIAJ NAME	*SOJ028-P-0300-A
JEDEC CODE	MO-077-AB