MICRON

WIDE DRAM

2 MEG x 8 DRAM

5.0V, SELF REFRESH (MT4C2M8A1/2 S)
3.0/3.3V, SELF REFRESH (MT4LC2M8A1/2 S)

WIDE DRAM (vertical sidebar text)

FEATURES

- SELF REFRESH, or "Sleep Mode"
- Industry-standard x8 pinouts, timing, functions and packages
- Address entry: 12 row-address, 9 column-addresses (512ms)
- High-performance CMOS silicon-gate process
- Single +5V only or 3.0/3.3V only ±10% power supply
- All device pins are TTL-compatible
- Refresh modes: $\overline{RAS}$-ONLY, $\overline{CAS}$-BEFORE-$\overline{RAS}$ (CBR), HIDDEN and BATTERY BACKUP (BBU)
- Optional FAST-PAGE-MODE access cycle
- NONPERSISTENT MASKED WRITE access cycle (MT4(L)C2M8A2 S only)
- 4,096-cycle refresh (2,048-cycle refresh available as MT4(L)C2M8B1/2 S)
- Low power, 2mW standby; 400mW active, typical (5V)

OPTIONS   MARKING

- Timing
  - 60ns access   -6
  - 70ns access   -7
  - 80ns access   -8

- Power Supply
  - 5V ±10% only   4C
  - 3.0/3.3V ±10% only   4LC

- MASKED WRITE
  - Not available   A1 S
  - Available   A2 S

- Packages
  - Plastic 28-pin SOJ (400 mil)   DJ
  - Plastic 28-pin TSOP (400 mil)   TG
  - Plastic 32-pin SOJ (400 mil)   DL
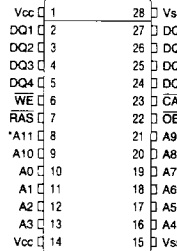 - Plastic 32-pin TSOP (400 mil)   TL

- Part Number Example: MT4C2M8A1DJ-7 S

PART DESCRIPTION

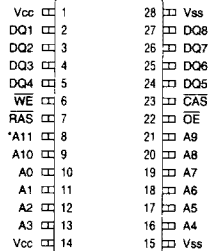|	
MT4C2M8A1 S	5V, NONMASKED WRITE
MT4C2M8A2 S	5V, MASKED WRITE
MT4LC2M8A1 S	3.0/3.3V, NONMASKED WRITE
MT4LC2M8A2 S	3.0/3.3V, MASKED WRITE

GENERAL DESCRIPTION

The MT4C2M8A1/2 S and MT4LC2M8A1/2 S are randomly accessed solid-state memories containing 16,777,216 bits organized in a x8 configuration. The
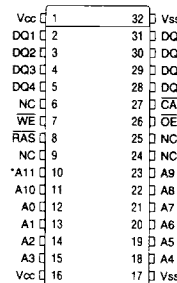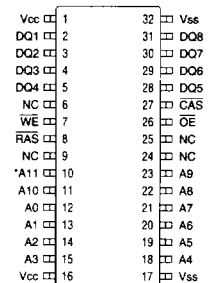
PIN ASSIGNMENT (Top View)

28-Pin SOJ (DC-4)

Vcc	1	28	Vss
DQ1	2	27	DQ8
DQ2	3	26	DQ7
DQ3	4	25	DQ6
DQ4	5	24	DQ5
$\overline{WE}$	6	23	$\overline{CAS}$
$\overline{RAS}$	7	22	$\overline{OE}$
*A11	8	21	A9
A10	9	20	A8
A0	10	19	A7
A1	11	18	A6
A2	12	17	A5
A3	13	16	A4
Vcc	14	15	Vss

28-Pin TSOP (DD-3)

Vcc	1	28	Vss
DQ1	2	27	DQ8
DQ2	3	26	DQ7
DQ3	4	25	DQ6
DQ4	5	24	DQ5
$\overline{WE}$	6	23	$\overline{CAS}$
$\overline{RAS}$	7	22	$\overline{OE}$
*A11	8	21	A9
A10	9	20	A8
A0	10	19	A7
A1	11	18	A6
A2	12	17	A5
A3	13	16	A4
Vcc	14	15	Vss

32-Pin SOJ (DC-5)

Vcc	1	32	Vss
DQ1	2	31	DQ8
DQ2	3	30	DQ7
DQ3	4	29	DQ6
DQ4	5	28	DQ5
NC	6	27	$\overline{CAS}$
$\overline{WE}$	7	26	$\overline{OE}$
$\overline{RAS}$	8	25	NC
NC	9	24	NC
*A11	10	23	A9
A10	11	22	A8
A0	12	21	A7
A1	13	20	A6
A2	14	19	A5
A3	15	18	A4
Vcc	16	17	Vss

32-Pin TSOP (DD-4)

|		
Vcc	1	32	Vss
DQ1	2	31	DQ8
DQ2	3	30	DQ7
DQ3	4	29	DQ6
DQ4	5	28	DQ5
NC	6	27	$\overline{CAS}$
$\overline{WE}$	7	26	$\overline{OE}$
$\overline{RAS}$	8	25	NC
NC	9	24	NC
*A11	10	23	A9
A10	11	22	A8
A0	12	21	A7
A1	13	20	A6
A2	14	19	A5
A3	15	18	A4
Vcc	16	17	Vss

*NC on 11 row-address version

MT4C2M8A1/2 S and the MT4LC2M8A1/2 S are the same DRAM versions except that the MT4LC2M8A1/2 S are low voltage versions of the MT4C2M8A1/2 S. The MT4LC2M8A1/2 S are designed to operate in either a 3.0V ±10% or a 3.3V ±10% memory system. All further references made for the MT4C2M8A1/2 S also apply to the MT4LC2M8A1/2 S, unless specifically stated otherwise. Each byte is uniquely addressed through the 21 address bits during READ or WRITE cycles. The address is entered first by $\overline{RAS}$ latching 12 bits (A0-11) and then $\overline{CAS}$ latching 9 bits (A0-A9).

The MT4C2M8A2 S has NONPERSISTENT MASKED WRITE, allowing it to perform WRITE-PER-BIT accesses.

FUNCTIONAL BLOCK DIAGRAM
4096 ROWS

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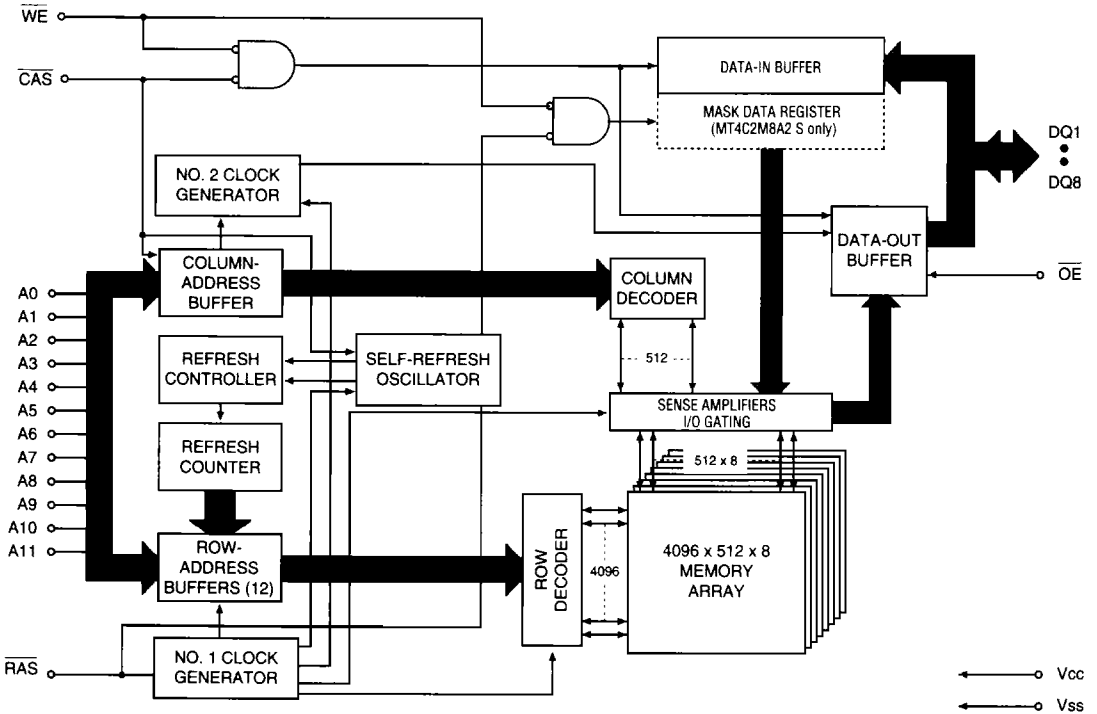
PIN DESCRIPTIONS

28-PIN DEVICE PIN NUMBERS	32-PIN DEVICE PIN NUMBERS	SYMBOL	TYPE	DESCRIPTION
7	8	$\overline{RAS}$	Input	Row-Address Strobe: $\overline{RAS}$ is used to clock-in the 12 row-address bits and strobe the $\overline{WE}$ and DQs in the MASKED WRITE mode (MT4C2M8A2 S only).
23	27	$\overline{CAS}$	Input	Column-Address Strobe: $\overline{CAS}$ is used to clock-in the 9 column-address bits, enable the DRAM output buffers and strobe the data inputs on WRITE cycles.
6	7	$\overline{WE}$	Input	Write Enable: $\overline{WE}$ is used to select a READ ($\overline{WE}$ = HIGH) or WRITE ($\overline{WE}$ = LOW) cycle. $\overline{WE}$ also serves as a mask enable ($\overline{WE}$ = LOW) at the falling edge of $\overline{RAS}$ in a MASKED WRITE cycle (MT4C2M8A2 S).
22	26	$\overline{OE}$	Input	Output Enable: $\overline{OE}$ enables the output buffers when taken LOW during a READ access cycle. $\overline{RAS}$ and $\overline{CAS}$ must be LOW and $\overline{WE}$ must be HIGH before $\overline{OE}$ will control the output buffers. Otherwise, the output buffers are in a High-Z state.
10-13, 16-21, 9, 8	12-15, 18-23, 11, 10	A0-A11	Input	Address Inputs: These inputs are multiplexed and clocked by $\overline{RAS}$ and $\overline{CAS}$ to select one byte out of the 2 Meg available words.
2-5, 24-27	2-5, 28-31	DQ1-DQ8	Input	Data I/O: Includes inputs, outputs or High-Z and/or output masked data input (for MASKED WRITE cycle only).
	6, 9, 24, 25	NC	-	No Connect: These pins should be either left unconnected or tied to ground.
1, 14	1, 16	Vcc	Supply	Power Supply: +5V ±10% (C), 2.7V to 3.6V (LC)
15, 28	17, 32	Vss	Supply	Ground

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FUNCTIONAL DESCRIPTION

Each bit is uniquely addressed through the 21 address bits during READ or WRITE cycles. First, $\overline{RAS}$ is used to latch 12 bits (A0-A11) then, $\overline{CAS}$ latches 9 bits (A0-A8).

The $\overline{CAS}$ control also determines whether the cycle will be a refresh cycle ($\overline{RAS}$-ONLY) or an active cycle (READ, WRITE or READ-WRITE) once $\overline{RAS}$ goes LOW.

READ or WRITE cycles are selected by $\overline{WE}$. A logic HIGH on $\overline{WE}$ dictates READ mode while a logic LOW on $\overline{WE}$ dictates WRITE mode. During a WRITE cycle, data-in (D) is latched by the falling edge of $\overline{WE}$ or $\overline{CAS}$, whichever occurs last. Taking $\overline{WE}$ LOW will initiate a WRITE cycle, selecting DQ1 through DQ8. If $\overline{WE}$ goes LOW prior to $\overline{CAS}$ going LOW, the output pin(s) remain open (High- Z) until the next $\overline{CAS}$ cycle. If $\overline{WE}$ goes LOW after $\overline{CAS}$ goes LOW and data reaches the output pins, data-out (Q) is activated and retains the selected cell data as long as $\overline{CAS}$ and $\overline{OE}$ remain LOW (regardless of $\overline{WE}$ or $\overline{RAS}$). This late $\overline{WE}$ pulse results in a READ-WRITE cycle.

The eight data inputs and eight data outputs are routed through eight pins using common I/O and pin direction is controlled by $\overline{OE}$ and $\overline{WE}$.

FAST-PAGE-MODE operations allow faster data operations (READ, WRITE or READ-MODIFY-WRITE) within a row-address-defined (A0-12) page boundary. The FAST-PAGE-MODE cycle is always initiated with a row-address strobed-in by $\overline{RAS}$ followed by a column-address strobed-in by $\overline{CAS}$. $\overline{CAS}$ may be toggled-in by holding $\overline{RAS}$ LOW and strobing-in different column-addresses, thus executing faster memory cycles. Returning $\overline{RAS}$ HIGH terminates the FAST-PAGE-MODE operation.

Returning $\overline{RAS}$ and $\overline{CAS}$ HIGH terminates a memory cycle and decreases chip current to a reduced standby level. The chip is also preconditioned for the next cycle during the $\overline{RAS}$ HIGH time. Memory cell data is retained in its correct state by maintaining power and executing any $\overline{RAS}$ cycle (READ, WRITE) or $\overline{RAS}$ REFRESH cycle ($\overline{RAS}$-ONLY, CBR, or HIDDEN) so that all 4,096 combinations of $\overline{RAS}$ addresses (A0-11) are executed at least every 512ms, regardless of sequence. The CBR REFRESH cycle will also invoke the refresh counter and controller for row-address control.

BBU is a CBR REFRESH performed at the extended refresh rate with CMOS input levels. This mode provides a very low-current, data-retention cycle. $\overline{RAS}$ or $\overline{CAS}$ time refers to the time at which $\overline{RAS}$ or $\overline{CAS}$ transition from HIGH to LOW).

SELF REFRESH is similar to BBU except that the DRAM provides its own internal clocking during sleep mode. Thus, an external clock is not required for additional power savings and design ease. The SELF REFRESH version retains the extended refresh rate of 512ms.

MASKED WRITE ACCESS CYCLE (MT4C2M8A2 S ONLY)

Every WRITE access cycle can be a MASKED WRITE, depending on the state of $\overline{WE}$ at $\overline{RAS}$ time. A MASKED WRITE is selected when $\overline{WE}$ is LOW at $\overline{RAS}$ time and mask data is supplied on the DQ pins.

The mask data present on the DQ1-DQ8 inputs at $\overline{RAS}$ time will be written to an internal mask data register and will then act as an individual write enable for each of the corresponding DQ inputs. If a LOW (logic "0") is written to a mask data register bit, the input port for that bit is disabled during the subsequent WRITE operation and no new data will be written to that DRAM cell location. A HIGH (logic "1") on a mask data register bit enables the input port and allows normal WRITE operations to proceed. At $\overline{CAS}$ time, the bits present on the DQ1-DQ8 inputs will be written to the DRAM (if the mask data bit was HIGH) or ignored (if the mask data bit was LOW).

In NONPERSISTENT MASKED WRITEs, new mask data must be supplied each time a MASKED WRITE cycle is initiated.

Figure 1 illustrates the MT4C2M8A2 S MASKED WRITE operation (Note: $\overline{RAS}$ or $\overline{CAS}$ time refers to the time at which $\overline{RAS}$ or $\overline{CAS}$ transition from HIGH to LOW).
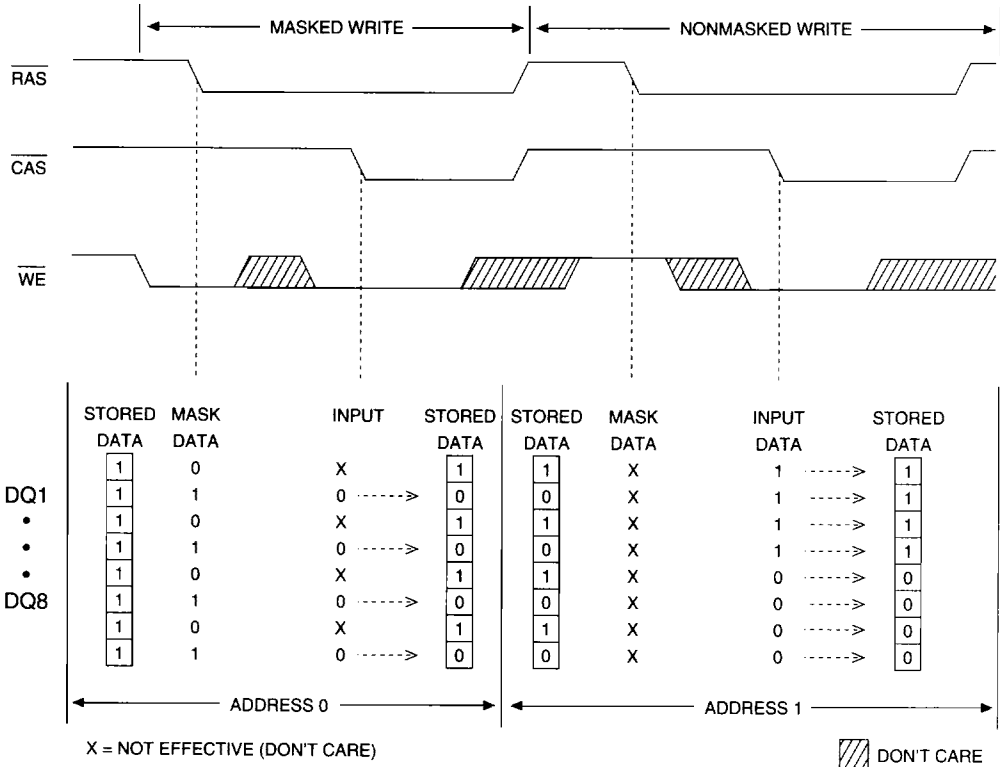
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Figure 1
MT4C2M8A2 S MASKED WRITE EXAMPLE

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TRUTH TABLE

FUNCTION		$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	$\overline{OE}$	ADDRESSES ^{t}R	^{t}C	DQs	NOTES
Standby		H	H→X	X	X	X	X	High-Z	
READ		L	L	H	L	ROW	COL	Data-Out	
EARLY-WRITE		L	L	L	X	ROW	COL	Data-In	1
READ-WRITE		L	L	H→L	L→H	ROW	COL	Data-Out, Data-In	1
FAST-PAGE-	1st Cycle	L	H→L	H	L	ROW	COL	Data-Out	
MODE READ	2nd Cycle	L	H→L	H	L	n/a	COL	Data-Out	
FAST-PAGE-	1st Cycle	L	H→L	L	X	ROW	COL	Data-In	1
MODE WRITE	2nd Cycle	L	H→L	L	X	n/a	COL	Data-In	1
FAST-PAGE-MODE	1st Cycle	L	H→L	H→L	L→H	ROW	COL	Data-Out, Data-In	1
READ-WRITE	2nd Cycle	L	H→L	H→L	L→H	n/a	COL	Data-Out, Data-In	1
HIDDEN	READ	L→H→L	L	H	L	ROW	COL	Data-Out	
REFRESH	WRITE	L→H→L	L	L	X	ROW	COL	Data-In	1, 2
$\overline{RAS}$-ONLY REFRESH		L	H	X	X	ROW	n/a	High-Z	
CBR REFRESH		H→L	L	H	X	X	X	High-Z	
BBU REFRESH		H→L	L	H	X	X	X	High-Z	
SELF REFRESH		H→L	L	H	X	X	X	High-Z	

NOTE: 1. Data-in will be dependent on the mask provided (MT4C2M8A2 S only). Refer to Figure 1.
2. EARLY WRITE only.

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ABSOLUTE MAXIMUM RATINGS*

Voltage on Vcc supply relative to Vss (5V) .... -1V to +7V
Voltage on Vcc supply relative to Vss (3V) .... -1V to +4.6V
Operating Temperature, T$_A$ (ambient) .... 0°C to +70°C
Storage Temperature (plastic) .... -55°C to +150°C
Power Dissipation 1W
Short Circuit Output Current 50mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

DC OPERATING SPECIFICATIONS FOR 5V VERSION

(Notes: 1, 3, 4, 6, 7, 30) (0°C ≤ T$_A$ ≤ 70°C; Vcc = 5V ±10%)

PARAMETER/CONDITION	SYMBOL	MIN	MAX	UNITS	NOTES
Supply Voltage	Vcc	4.5	5.5	V	1, 30
Input High (Logic 1) Voltage, all inputs	VIH	2.4	Vcc+1	V	1
Input Low (Logic 0) Voltage, all inputs	VIL	-1.0	0.8	V	1
INPUT LEAKAGE CURRENT Any input 0V ≤ VIN ≤ Vcc (All other pins not under test = 0V)	Ii	-2	2	μA	
OUTPUT LEAKAGE CURRENT (Q is disabled; 0V ≤ VOUT ≤ 5.5V)	Ioz	-10	10	μA	
OUTPUT LEVELS Output High Voltage (IOUT = -2.5mA)	VOH	2.4		V	
Output Low Voltage (IOUT = 2.1mA)	VOL		0.4	V	

DC OPERATING SPECIFICATIONS FOR 3.0/3.3V VERSION

(Notes: 1, 3, 4, 6, 7, 31) (0°C ≤ T$_A$ ≤ 70°C; Vcc = 2.7V to 3.6V)

PARAMETER/CONDITION	SYMBOL	MIN	MAX	UNITS	NOTES
Supply Voltage	Vcc	2.7	3.6	V	1, 31
Input High (Logic 1) Voltage, all inputs	VIH	2.0	Vcc+1	V	1
Input Low (Logic 0) Voltage, all inputs	VIL	-1.0	0.8	V	1
INPUT LEAKAGE CURRENT Any input 0V ≤ VIN ≤ Vcc (All other pins not under test = 0V)	Ii	-2	2	μA	
OUTPUT LEAKAGE CURRENT (Q is disabled; 0V ≤ VOUT ≤ 3.6V)	Ioz	-10	10	μA	
OUTPUT LEVELS Output High Voltage (IOUT = -2mA)	VOH	2.4		V	
Output Low Voltage (IOUT = 2mA)	VOL		0.4	V	

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DC OPERATING SPECIFICATIONS FOR 5V VERSION

(Notes: 1, 3, 4, 6, 7, 30) (0°C ≤ T_A ≤ 70°C; Vcc = 5V ±10%)

PARAMETER/CONDITION	SYMBOL	MAX			UNITS	NOTES
		-6	-7	-8		
STANDBY CURRENT: TTL ($\overline{RAS}$ = $\overline{CAS}$ = V_{IH})	I_{CC1}	2	2	2	mA	
STANDBY CURRENT: CMOS ($\overline{RAS}$ = $\overline{CAS}$ = Vcc -0.2V)	I_{CC2}	200	200	200	µA	25
OPERATING CURRENT: Random READ/WRITE Average power supply current ($\overline{RAS}$, $\overline{CAS}$, Address Cycling: ^tRC = ^tRC [MIN])	I_{CC3}	110	100	90	mA	3, 4, 32
OPERATING CURRENT: FAST-PAGE-MODE Average power supply current ($\overline{RAS}$ = V_{IL}, $\overline{CAS}$, Address Cycling: ^tPC = ^tPC [MIN]; ^tCP, ^tASC = 10ns)	I_{CC4}	80	70	60	mA	3, 4, 32
REFRESH CURRENT: $\overline{RAS}$-ONLY Average power supply current ($\overline{RAS}$ Cycling, $\overline{CAS}$ = V_{IH}: ^tRC = ^tRC [MIN])	I_{CC5}	110	100	90	mA	3, 32
REFRESH CURRENT: CBR Average power supply current ($\overline{RAS}$, $\overline{CAS}$, Address Cycling: ^tRC = ^tRC [MIN])	I_{CC6}	110	100	90	mA	3, 5
REFRESH CURRENT: BBU Average power supply current during BBU REFRESH: $\overline{CAS}$ = 0.2V or CBR cycling; $\overline{RAS}$ = ^tRAS (MIN) to 300ns; $\overline{WE}$, A0-A11 and D_{IN} = Vcc - 0.2V (D_{IN} may be left open), ^tRC = 125µs (1,024 rows at 125µs = 128ms)	I_{CC7}	300	300	300	µA	3, 30
REFRESH CURRENT: SELF Average power supply current during SELF REFRESH: CBR cycle with $\overline{RAS}$ ≥ ^tRASS (MIN) and $\overline{CAS}$ held LOW; $\overline{WE}$ = Vcc - 0.2V; A0-A9 and D_{IN} = Vcc - 0.2V or 0.2V (D_{IN} may be left open)	I_{CC8}	300	300	300	µA	5

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DC OPERATING SPECIFICATIONS FOR 3.0/3.3V VERSION

(Notes: 1, 3, 4, 6, 7, 31) (0°C ≤ T_A ≤ 70°C; Vcc = 2.7V to 3.6V)

PARAMETER/CONDITION	SYMBOL	MAX -6	-7	-8	UNITS	NOTES
STANDBY CURRENT: TTL ($\overline{RAS}$ = $\overline{CAS}$ = VIH)	Icc1	2	2	2	mA	
STANDBY CURRENT: CMOS ($\overline{RAS}$ = $\overline{CAS}$ = Vcc -0.2V)	Icc2	200	200	200	µA	25
OPERATING CURRENT: Random READ/WRITE Average power supply current ($\overline{RAS}$, $\overline{CAS}$, Address Cycling: ^tRC = ^tRC [MIN])	Icc3	110	100	90	mA	3, 4, 32
OPERATING CURRENT: FAST-PAGE-MODE Average power supply current ($\overline{RAS}$ = VIL, $\overline{CAS}$, Address Cycling: ^tPC = ^tPC [MIN]; ^tCP, ^tASC = 10ns)	Icc4	80	70	60	mA	3, 4, 32
REFRESH CURRENT: $\overline{RAS}$-ONLY Average power supply current ($\overline{RAS}$ Cycling, $\overline{CAS}$ = VIH: ^tRC = ^tRC [MIN])	Icc5	110	100	90	mA	3, 32
REFRESH CURRENT: CBR Average power supply current ($\overline{RAS}$, $\overline{CAS}$, Address Cycling: ^tRC = ^tRC [MIN])	Icc6	110	100	90	mA	3, 5
REFRESH CURRENT: BBU Average power supply current during BBU REFRESH: $\overline{CAS}$ = 0.2V or CBR cycling; $\overline{RAS}$ = ^tRAS (MIN) to 300ns; $\overline{WE}$, A0-A11 and DIN = Vcc - 0.2V (DIN may be left open), ^tRC = 125µs (1,024 rows at 125µs = 128ms)	Icc7	300	300	300	µA	3, 30
REFRESH CURRENT: SELF Average power supply current during SELF REFRESH: CBR cycle with $\overline{RAS}$ ≥ ^tRASS (MIN) and $\overline{CAS}$ held LOW; $\overline{WE}$ = Vcc - 0.2V; A0-A9 and DIN = Vcc - 0.2V or 0.2V (DIN may be left open)	Icc8	300	300	300	µA	5

CAPACITANCE

PARAMETER	SYMBOL	MAX	UNITS	NOTES
Input Capacitance: A0-A11	C_{I1}	5	pF	2
Input Capacitance: RAS, CAS, WE, OE	C_{I2}	7	pF	2
Input/Output Capacitance: DQ	C_{IO}	7	pF	2

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 6, 7, 8, 9, 10, 11, 12, 13) (0°C ≤ T_A ≤ +70°C)

AC CHARACTERISTICS PARAMETER	SYM	-6 MIN	-6 MAX	-7 MIN	-7 MAX	-8 MIN	-8 MAX	UNITS	NOTES
Random READ or WRITE cycle time	tRC	110		130		150		ns	
READ-WRITE cycle time	tRWC	155		180		200		ns	
FAST-PAGE-MODE READ or WRITE cycle time	tPC	35		40		45		ns	
FAST-PAGE-MODE READ-WRITE cycle time	tPRWC	85		95		100		ns	
Access time from RAS	tRAC		60		70		80	ns	14
Access time from CAS	tCAC		15		20		20	ns	15
Output Enable	tOE		15		15		15	ns	
Access time from column-address	tAA		30		35		40	ns	
Access time from CAS precharge	tCPA		35		40		45	ns	
RAS pulse width	tRAS	60	100,000	70	100,000	80	100,000	ns	
RAS pulse width (FAST-PAGE-MODE)	tRASP	60	100,000	70	100,000	80	100,000	ns	
RAS hold time	tRSH	15		20		20		ns	
RAS precharge time	tRP	40		50		60		ns	
CAS pulse width	tCAS	15	100,000	20	100,000	20	100,000	ns	
CAS hold time	tCSH	60		70		80		ns	
CAS precharge time	tCPN	10		10		10		ns	16
CAS precharge time (FAST-PAGE-MODE)	tCP	10		10		10		ns	
RAS to CAS delay time	tRCD	15	45	20	50	20	60	ns	17
CAS to RAS precharge time	tCRP	5		5		5		ns	
Row-address setup time	tASR	0		0		0		ns	
Row-address hold time	tRAH	10		10		10		ns	
RAS to column-address delay time	tRAD	15	30	15	35	15	40	ns	18
Column-address setup time	tASC	0		0		0		ns	
Column-address hold time	tCAH	10		15		15		ns	
Column-address hold time (referenced to RAS)	tAR	50		55		60		ns	
Column-address to RAS lead time	tRAL	30		35		40		ns	
Read command setup time	tRCS	0		0		0		ns	26
Read command hold time (referenced to CAS)	tRCH	0		0		0		ns	19, 26
Read command hold time (referenced to RAS)	tRRH	0		0		0		ns	19
CAS to output in Low-Z	tCLZ	3		3		3		ns	34
Output buffer turn-off delay	tOFF	3	15	3	20	3	20	ns	20, 29, 34

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ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 6, 7, 8, 9, 10, 11, 12, 13) (0°C ≤ T$_A$ ≤ +70°C)

| AC CHARACTERISTICS PARAMETER	SYM	-6 MIN	-6 MAX	-7 MIN	-7 MAX	-8 MIN	-8 MAX	UNITS	NOTES
$\overline{WE}$ command setup time	^{t}WCS	0		0		0		ns	21, 26
Write command hold time	^{t}WCH	10		15		15		ns	26
Write command hold time (referenced to $\overline{RAS}$)	^{t}WCR	45		55		60		ns	26
Write command pulse width	^{t}WP	10		15		15		ns	26
Write command to $\overline{RAS}$ lead time	^{t}RWL	15		20		20		ns	26
Write command to $\overline{CAS}$ lead time	^{t}CWL	15		20		20		ns	26
Data-in setup time	^{t}DS	0		0		0		ns	22
Data-in hold time	^{t}DH	10		15		15		ns	22
Data-in hold time (referenced to $\overline{RAS}$)	^{t}DHR	45		55		60		ns	
$\overline{RAS}$ to $\overline{WE}$ delay time	^{t}RWD	85		95		105		ns	21
Column-address to $\overline{WE}$ delay time	^{t}AWD	55		60		65		ns	21
$\overline{CAS}$ to $\overline{WE}$ delay time	^{t}CWD	40		45		45		ns	21
Transition time (rise or fall)	^{t}T	3	50	3	50	3	50	ns	9, 10
Refresh period (4,096 cycles)	^{t}REF		512		512		512	ms	
$\overline{RAS}$ to $\overline{CAS}$ precharge time	^{t}RPC	0		0		0		ns	
$\overline{CAS}$ setup time (CBR REFRESH)	^{t}CSR	5		5		5		ns	5
$\overline{CAS}$ hold time (CBR REFRESH)	^{t}CHR	15		15		15		ns	5
$\overline{WE}$ hold time (MASKED WRITE and CBR REFRESH)	^{t}WRH	15		15		15		ns	26
$\overline{WE}$ setup time (CBR REFRESH)	^{t}WRP	10		10		10		ns	26
$\overline{WE}$ setup time (MASKED WRITE)	^{t}WRS	10		10		10		ns	26
$\overline{OE}$ setup prior to RAS during HIDDEN REFRESH cycle	^{t}ORD	0		0		0		ns	
Output disable	^{t}OD	3	15	3	15	3	15	ns	29, 34
$\overline{OE}$ hold time from $\overline{WE}$ during READ-MODIFY-WRITE cycle	^{t}OEH	15		15		15		ns	28
$\overline{RAS}$ pulse width during SELF REFRESH cycle	^{t}RASS	100		100		100		µs	
$\overline{RAS}$ precharge time during SELF REFRESH cycle	^{t}RPS	150		150		150		ns	
$\overline{CAS}$ hold time during SELF REFRESH cycle	^{t}CHS	-70		-70		-70		ns	

NOTES

1. All voltages referenced to V_{SS}.
2. This parameter is sampled. $V_{CC} = 5V \pm 10\%$; $f = 1$ MHz.
3. I_{CC} is dependent on cycle rates.
4. I_{CC} is dependent on output loading and cycle rates. Specified values are obtained with minimum cycle time and the outputs open.
5. Enables on-chip refresh and address counters.
6. The minimum specifications are used only to indicate cycle time at which proper operation over the full temperature range ($0°C \leq T_A \leq 70°C$) is assured.
7. An initial pause of 100µs is required after power-up followed by eight $\overline{RAS}$ refresh cycles ($\overline{RAS}$-ONLY or CBR) before proper device operation is assured. The eight $\overline{RAS}$ cycle wake-ups should be repeated any time the ^tREF refresh requirement is exceeded.
8. AC characteristics assume $^tT = 5$ns.
9. V_{IH} (MIN) and V_{IL} (MAX) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}).
10. In addition to meeting the transition rate specification, all input signals must transit between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}) in a monotonic manner.
11. If $\overline{CAS}$ = V_{IH}, data output is high impedance.
12. If $\overline{CAS}$ = V_{IL}, data output may contain data from the last valid READ cycle.
13. Measured with a load equivalent to one TTL gate and 50pF.
14. Assumes that $^tRCD < {}^tRCD$ (MAX). If ^tRCD is greater than the maximum recommended value shown in this table, ^tRAC will increase by the amount that ^tRCD exceeds the value shown.
15. Assumes that $^tRCD \geq {}^tRCD$ (MAX).
16. If $\overline{CAS}$ is LOW at the falling edge of $\overline{RAS}$, Q will be maintained from the previous cycle. To initiate a new cycle and clear the Q buffer, $\overline{CAS}$ must be pulsed HIGH for ^tCPN.
17. Operation within the ^tRCD (MAX) limit ensures that ^tRAC (MAX) can be met. ^tRCD (MAX) is specified as a reference point only; if ^tRCD is greater than the specified ^tRCD (MAX) limit, access time is controlled exclusively by ^tCAC.
18. Operation within the ^tRAD limit ensures that ^tRCD (MAX) can be met. ^tRAD (MAX) is specified as a reference point only; if ^tRAD is greater than the specified ^tRAD (MAX) limit, access time is controlled exclusively by ^tAA.
19. Either ^tRCH or ^tRRH must be satisfied for a READ cycle.
20. ^tOFF (MAX) defines the time at which the output achieves the open circuit condition; it is not a reference to V_{OH} or V_{OL}.

21. ^tWCS, ^tRWD, ^tAWD and ^tCWD are restrictive operating parameters in LATE-WRITE and READ-MODIFY-WRITE cycles only. If $^tWCS \geq {}^tWCS$ (MIN), the cycle is an EARLY-WRITE cycle and the data output will remain an open circuit throughout the entire cycle. If $^tRWD \geq {}^tRWD$ (MIN), $^tAWD \geq {}^tAWD$ (MIN) and $^tCWD \geq {}^tCWD$ (MIN), the cycle is a READ-WRITE and the data output will contain data read from the selected cell. If neither of the above conditions is met, the state of data-out is indeterminate. $\overline{OE}$ held HIGH and $\overline{WE}$ taken LOW after $\overline{CAS}$ goes LOW results in a LATE-WRITE ($\overline{OE}$-controlled) cycle.
22. These parameters are referenced to $\overline{CAS}$ leading edge in EARLY-WRITE cycles and $\overline{WE}$ leading edge in LATE-WRITE or READ-MODIFY-WRITE cycles.
23. During a READ cycle, if $\overline{OE}$ is LOW then taken HIGH before $\overline{CAS}$ goes HIGH, Q goes open. If $\overline{OE}$ is tied permanently LOW, LATE-WRITE or READ-MODIFY-WRITE operations are not possible.
24. A HIDDEN REFRESH may also be performed after a WRITE cycle. In this case, $\overline{WE}$ = LOW and $\overline{OE}$ = HIGH.
25. All other inputs at Vcc -0.2V.
26. Write command is defined as $\overline{WE}$ going LOW.
27. MT4C2M8A2 S only.
28. LATE-WRITE and READ-MODIFY-WRITE cycles must have both ^tOD and ^tOEH met ($\overline{OE}$ HIGH during WRITE cycle) in order to ensure that the output buffers will be open during the WRITE cycle. If $\overline{OE}$ is taken back LOW while $\overline{CAS}$ remains LOW, the DQs will remain open.
29. The DQs open during READ cycles once ^tOD or ^tOFF occur. If $\overline{CAS}$ goes HIGH before $\overline{OE}$, the DQs will open regardless of the state of $\overline{OE}$. If $\overline{CAS}$ stays LOW while $\overline{OE}$ is brought HIGH, the DQs will open. If $\overline{OE}$ is brought back LOW ($\overline{CAS}$ still LOW), the DQs will provide the previously read data.
30. BBU current is reduced as ^tRAS is reduced from its maximum specification during BBU cycle.
31. The 3.0/3.3V version is restricted to operate between 2.7 V and 3.6V only. The -6 speed version is only valid for Vcc = 3.0V to 3.6 V whereas the -7 and -8 speed versions are valid for Vcc = 2.7V to 3.6V.
32. The 3.0/3.3V version is restricted to operate between 2.7 V and 3.6V only.
33. Column-address changed once while $\overline{RAS}$ = V_{IL} and $\overline{CAS}$ = V_{IH}.
34. The 3ns minimum is a parameter guaranteed by design.
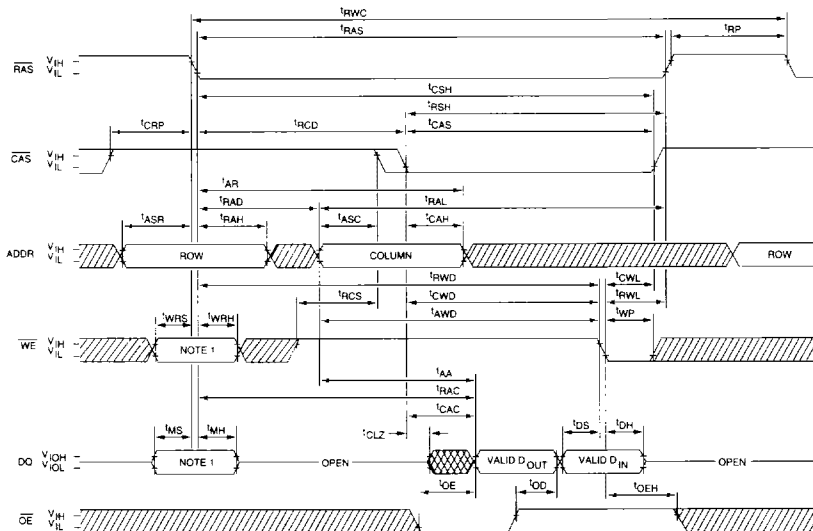
WIDE DRAM
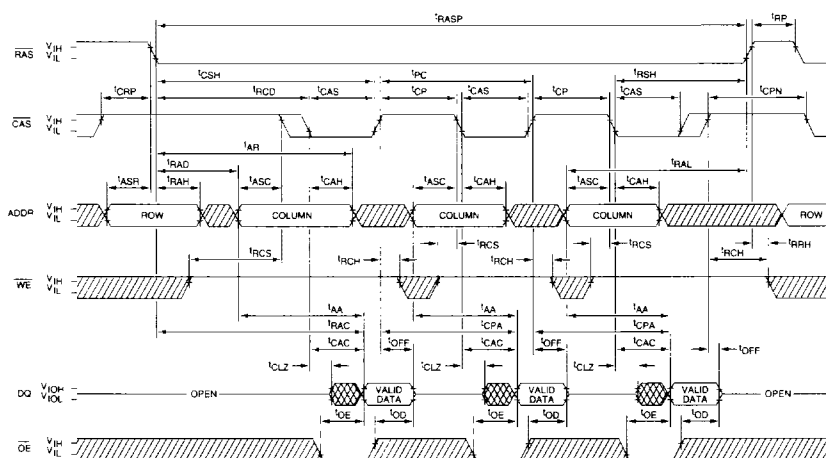
READ CYCLE
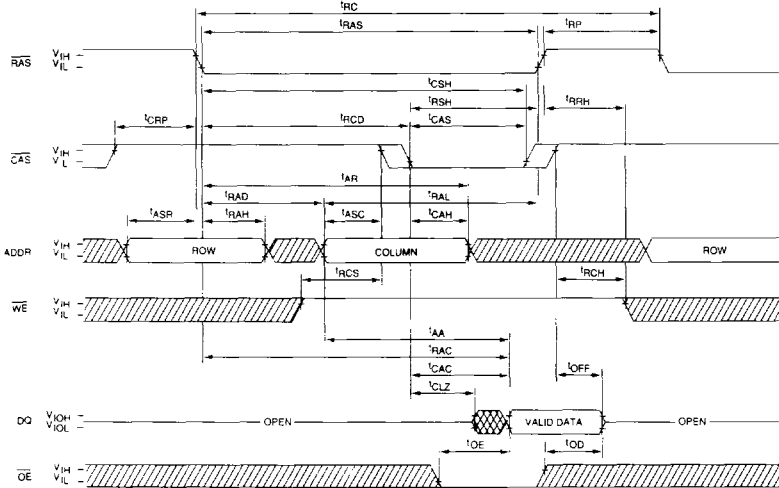
EARLY-WRITE CYCLE
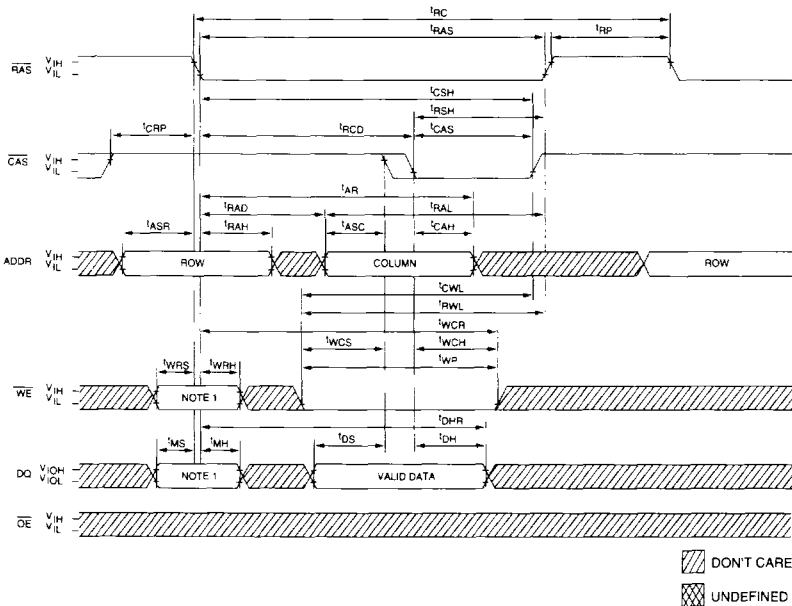
▨ DON'T CARE

▨ UNDEFINED

NOTE: 1. Applies to MT4C2M8A2 S only; $\overline{WE}$ and DQ inputs on MT4C2M8A1 S are "don't care" at $\overline{RAS}$ time. $\overline{WE}$ selects between normal WRITE and MASKED WRITE at $\overline{RAS}$ time. The DQ inputs are "don't care" for a normal WRITE ($\overline{WE}$ HIGH at $\overline{RAS}$ time). The DQ inputs provide the mask data at $\overline{RAS}$ time for a MASKED WRITE, $\overline{WE}$ LOW at $\overline{RAS}$ time.

MICRON

WIDE DRAM

READ-WRITE CYCLE
(LATE-WRITE and READ-MODIFY-WRITE CYCLES)

FAST-PAGE-MODE READ CYCLE

▨ DON'T CARE

▨ UNDEFINED

NOTE: 1. Applies to MT4C2M8A2 S only; $\overline{WE}$ and DQ inputs on MT4C2M8A1 S are "don't care" at $\overline{RAS}$ time. $\overline{WE}$ selects between normal WRITE and MASKED WRITE at $\overline{RAS}$ time. The DQ inputs are "don't care" for a normal WRITE ($\overline{WE}$ HIGH at $\overline{RAS}$ time). The DQ inputs provide the mask data at $\overline{RAS}$ time for a MASKED WRITE, $\overline{WE}$ LOW at $\overline{RAS}$ time.

WIDE DRAM

FAST-PAGE-MODE EARLY-WRITE CYCLE

FAST-PAGE-MODE READ-WRITE CYCLE
(LATE-WRITE and READ-MODIFY-WRITE CYCLES)
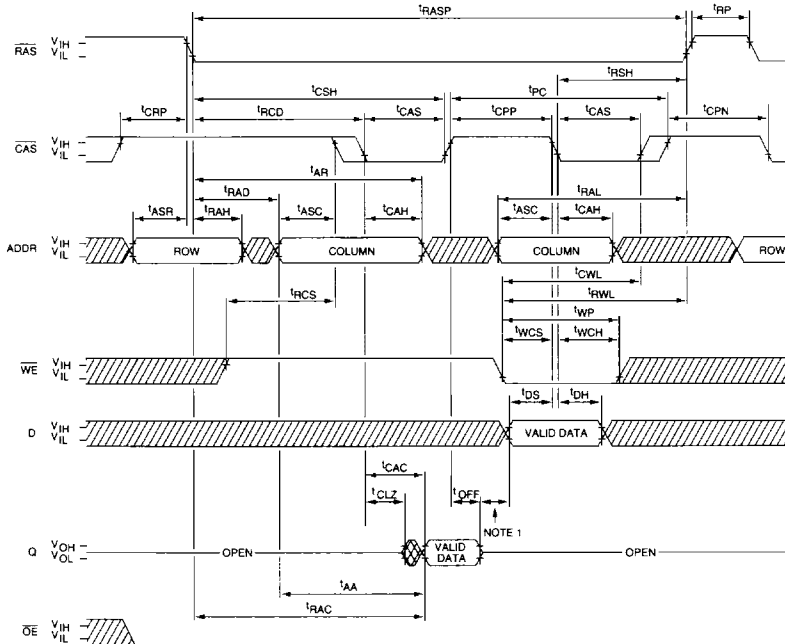

DON'T CARE

UNDEFINED

NOTE: 1. Applies to MT4C2M8A2 S only; $\overline{WE}$ and DQ inputs on MT4C2M8A1 S are "don't care" at $\overline{RAS}$ time. $\overline{WE}$ selects between normal WRITE and MASKED WRITE at $\overline{RAS}$ time. The DQ inputs are "don't care" for a normal WRITE ($\overline{WE}$ HIGH at $\overline{RAS}$ time). The DQ inputs provide the mask data at $\overline{RAS}$ time for a MASKED WRITE, $\overline{WE}$ LOW at $\overline{RAS}$ time.

WIDE DRAM

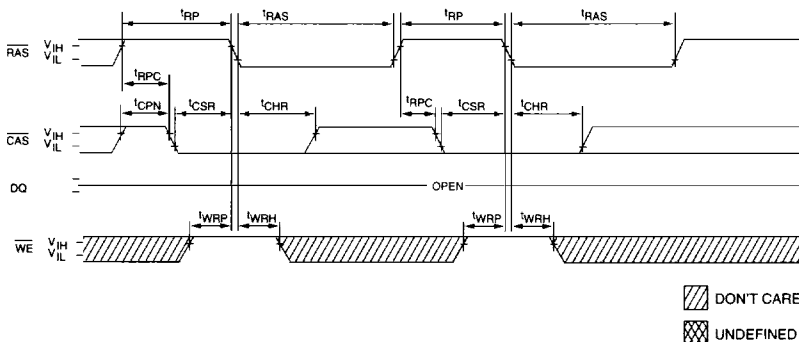## FAST-PAGE-MODE READ-EARLY-WRITE CYCLE
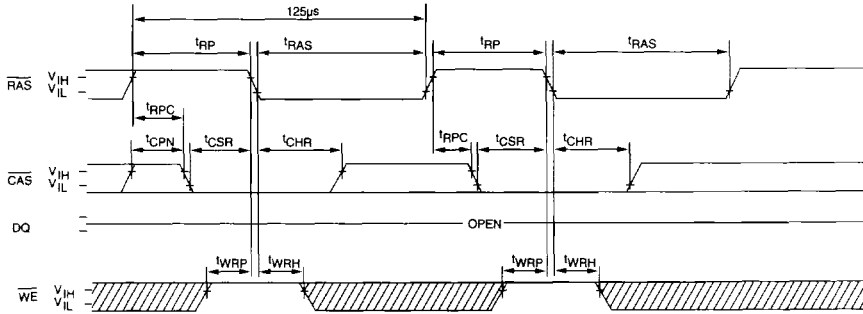### (Pseudo READ-MODIFY-WRITE)

NOTE: 1. Do not drive data prior to High-Z; that is completion of ^tOFF. ^tCPP is equal to $^tOFF + ^tDS(MIN)$ + guardband between data-out and driving new data-in.
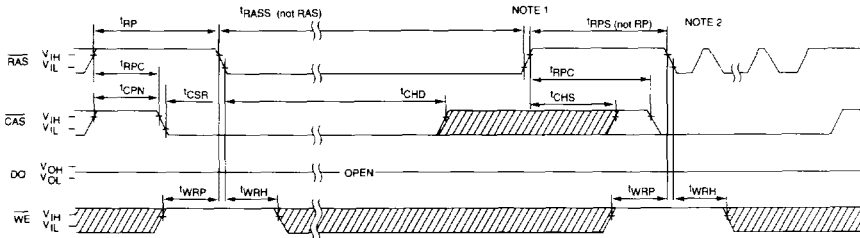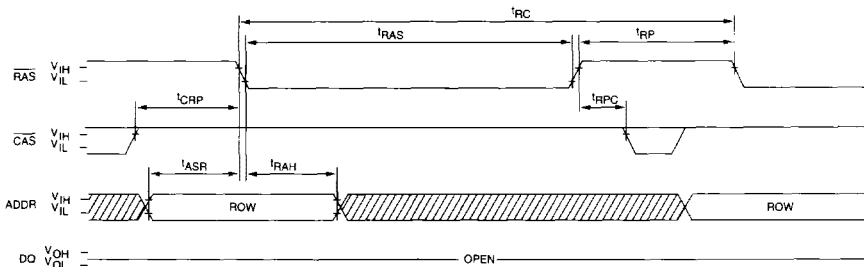
CBR REFRESH CYCLE
(A0-A11; $\overline{OE}$ = DON'T CARE)

DON'T CARE

UNDEFINED

WIDE DRAM

BBU REFRESH CYCLE
(A0-A11; $\overline{OE}$ = DON'T CARE)

125µs

t_{RP} t_{RAS} t_{RP} t_{RAS}

$\overline{RAS}$ V_{IH} V_{IL}

t_{RPC}

t_{CPN} t_{CSR} t_{CHR} t_{RPC} t_{CSR} t_{CHR}

$\overline{CAS}$ V_{IH} V_{IL}

DQ OPEN

t_{WRP} t_{WRH} t_{WRP} t_{WRH}

$\overline{WE}$ V_{IH} V_{IL}

SELF REFRESH CYCLE ("SLEEP MODE")
(A0-A11; $\overline{OE}$ = DON'T CARE)

t_{RP} t_{RASS} (not RAS) NOTE 1 t_{RPS} (not RP) NOTE 2

$\overline{RAS}$ V_{IH} V_{IL}

t_{RPC} t_{RPC}

t_{CPN} t_{CSR} t_{CHD} t_{CHS}

$\overline{CAS}$ V_{IH} V_{IL}

DQ V_{OH} V_{OL} OPEN

t_{WRP} t_{WRH} t_{WRP} t_{WRH}

$\overline{WE}$ V_{IH} V_{IL}

$\overline{RAS}$-ONLY REFRESH CYCLE
($\overline{OE}$ and $\overline{WE}$ = DON'T CARE)

t_{RC}

t_{RAS} t_{RP}

$\overline{RAS}$ V_{IH} V_{IL}

t_{CRP} t_{RPC}

$\overline{CAS}$ V_{IH} V_{IL}

t_{ASR} t_{RAH}

ADDR V_{IH} V_{IL} ROW ROW

DQ V_{OH} V_{OL} OPEN

DON'T CARE

UNDEFINED

WIDE DRAM

HIDDEN REFRESH CYCLE [24]
($\overline{WE}$ = HIGH; $\overline{OE}$ = LOW)

DON'T CARE

UNDEFINED