Icemos
Cooler than cool

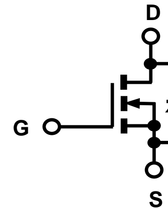
Preliminary Data Sheet
ICE4N73

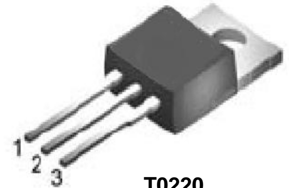
Product Summary			
I_D	T_A=25°C	4A	Max
$V_{(BR)DSS}$	I_D=250uA	730V	Min
$r_{DS(on)}$	V_{GS}=10V	1.0Ω	Typ
Q_g	V_{DS}=480V	21nC	Typ

ICE4N73 N-Channel Enhancement Mode MOSFET

Features

- Low $r_{DS(on)}$
- Ultra Low Gate Charge
- High dv/dt capability
- High Unclamped Inductive Switching (UIS) capability
- High peak current capability
- Increased transconductance performance
- Optimized design for high performance power systems





T0220

Standard Metal Heatsink

1=Gate, 2=Drain, 3=Source.

ICEMOS AND ITS SISTER COMPANY 3D SEMI OWN THE FUNDAMENTAL PATENTS FOR SUPERJUNCTION MOSFETS. THE MAJORITY OF THESE PATENTS HAVE 17 to 20 YEARS OF REMAINING LIFE. THIS PORTFOLIO HAS GRANTED PATENTS ISSUED IN USA, CHINA, KOREA, JAPAN, TAIWAN & EUROPE.

Maximum ratings [b], at T_j=25°C, unless otherwise specified

Parameter	*Symbol*	*Conditions*	*Value*	*Unit*
Continuous drain current	I_D	T_c=25°C	4	A
Pulsed drain current	$I_{D, pulse}$	T_c=25°C	12	A
Avalanche energy, single pulse	E_{AS}	I_D=2A	80	mJ
Avalanche current, repetitive	I_{AR}	limited by $T_j$max	2	A
MOSFET dv/dt ruggedness	dv/dt	V_{DS}=480V, I_D=4A, T_j=125°C	50	V/ns
Gate source voltage	V_{GS}	Static	±20	V
		AC (f>1Hz)	±30	
Power dissipation	P_{tot}	T_c=25°C	65	W
Operating and storage temperature	T_j, T_{stg}		-55 to +150	°C
Mounting torque		M 3 & 3.5 screws	60	Ncm

a When mounted on 1inch square 2oz copper clad FR-4

b Preliminary Data Sheet – Specifications subject to change

Parameter	Symbol	Conditions	Values			Unit
			Min	Typ	Max	

Thermal characteristics

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Thermal resistance, junction-case	R_{thJC}		-	-	1.9	°C/W
Thermal resistance, junction-ambient	R_{thJA}	leaded	-	-	68	
Soldering temperature, wave soldering only allowed at leads	T_{sold}	1.6mm (0.063in.) from case for 10 s	-	-	260	°C

Electrical characteristics [b], at T_j=25°C, unless otherwise specified

Static characteristics

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Drain-source breakdown voltage	$V_{(BR)DSS}$	V_{GS}=0 V, I_D=250μA	730	770	-	V
Gate threshold voltage	$V_{GS(th)}$	V_{DS}=V_{GS}, I_D=250μA	2.1	3	3.9	
Zero gate voltage drain current	I_{DSS}	V_{DS}=730V, V_{GS}=0V, T_j=25°C	-	0.5	5	μA
		V_{DS}=730V, V_{GS}=0V, T_j=150°C	-	-	100	
Gate source leakage current	I_{GSS}	V_{GS}=±20 V, V_{DS}=0V	-	-	100	nA
Drain-source on-state resistance	$R_{DS\ (on)}$	V_{GS}=10V, I_D=2A, T_j=25°C	-	1.0	1.2	Ω
		V_{GS}=10V, I_D=2A, T_j=150°C	-	2.6	-	
Gate resistance	R_G	f=1 MHZ, open drain	-	6.3	-	Ω

Dynamic characteristics

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Input capacitance	C_{iss}	V_{GS}=0 V, V_{DS}=25 V, f=1 MHz	-	630	-	pF
Output capacitance	C_{oss}		-	430	-	
Reverse transfer capacitance	C_{rss}		-	12	-	
Transconductance	g_{fs}	V_{DS}>2*I_D*R_{DS}, I_D=2A	-	4	-	S
Turn-on delay time	$t_{d(on)}$	V_{DS}=480V, V_{GS}=10V, I_D=4A, R_G=4Ω (External)	-	22	-	ns
Rise time	t_r		-	5	-	
Turn-off delay time	$t_{d(off)}$		-	67	-	
Fall time	t_f		-	4.5	-	

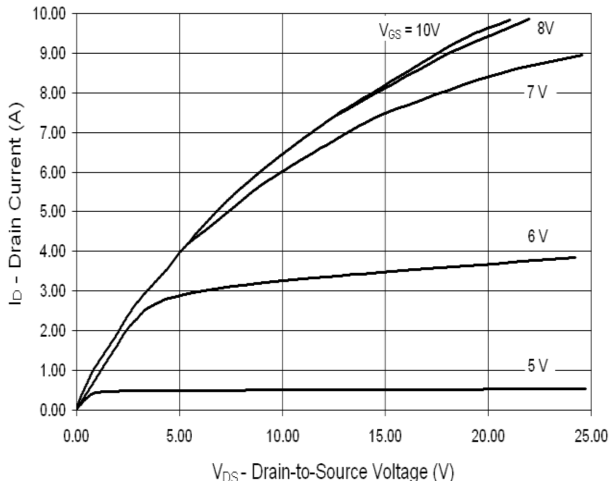
Parameter	Symbol	Conditions	Values			Unit
			Min	Typ	Max	

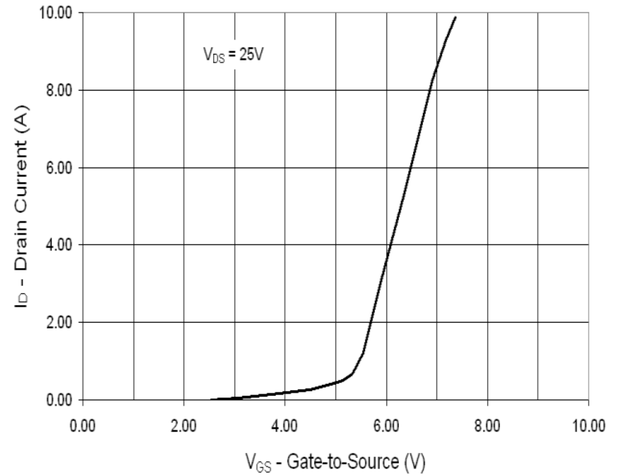
Gate charge characteristics

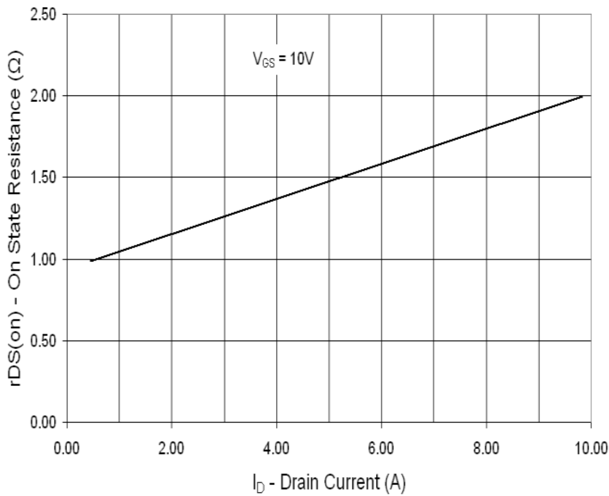
Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Gate to source charge	Q_{gs}	V_{DS}=480 V, I_D=4A, V_{GS}=0 to 10 V	-	4.6	-	nC
Gate to drain charge	Q_{gd}		-	6.8	-	
Gate charge total	Q_g		-	21	-	
Gate plateau voltage	$V_{plateau}$		-	5.5	-	V

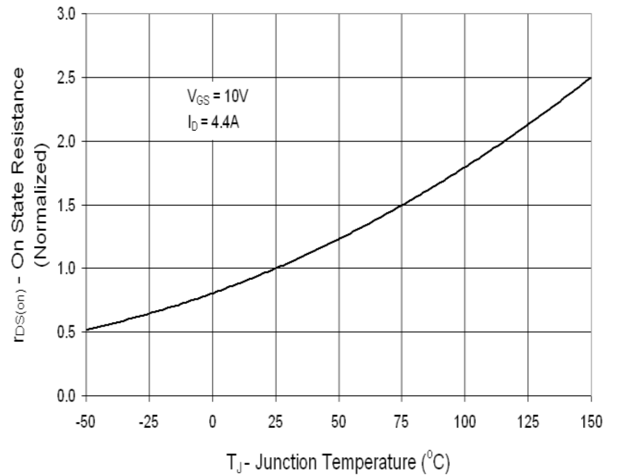
Reverse Diode

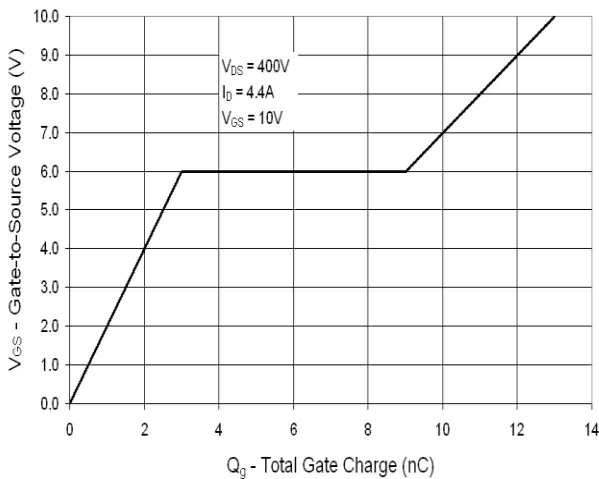
Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Diode forward voltage	V_{SD}	V_{GS}=0V, $I_{S=}I_F$	-	1.0	1.2	V
Reverse recovery time	t_{rr}	V_{RR}=480V, $I_{S=}I_F$, d_{iF}/d_t=100 A/µS	-	280	-	ns
Reverse recovery charge	Q_{rr}		-	3	-	µC
Peak reverse recovery current	I_{rm}		-	20	-	A

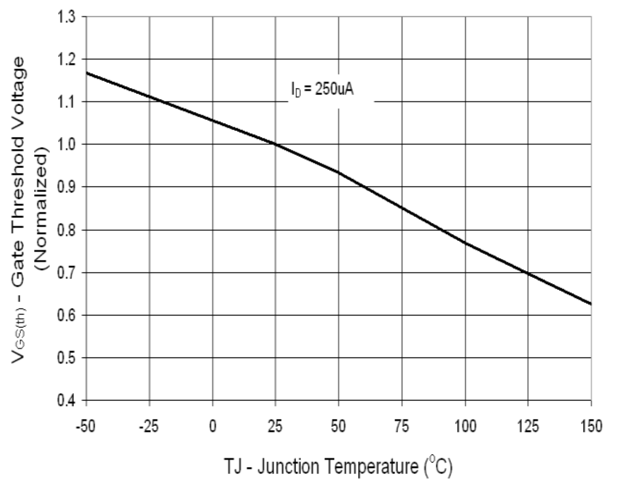

Output Characteristics
V_GS = 10V
8V
7 V
6 V
5 V
I_D - Drain Current (A)
V_DS - Drain-to-Source Voltage (V)
10.00
9.00
8.00
7.00
6.00
5.00
4.00
3.00
2.00
1.00
0.00
0.00
5.00
10.00
15.00
20.00
25.00

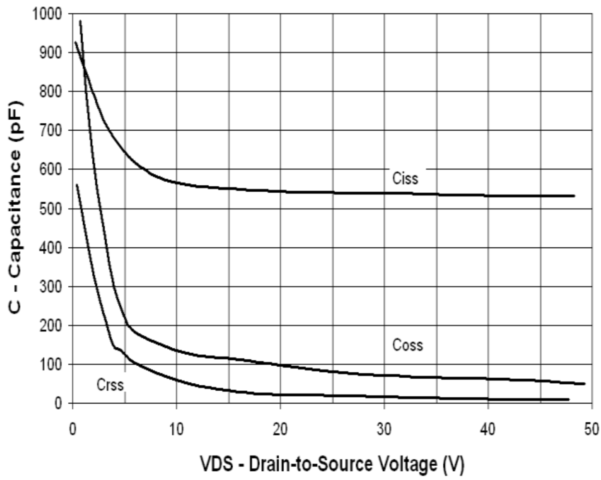

Transfer Characteristics
V_DS = 25V
I_D - Drain Current (A)
V_GS - Gate-to-Source (V)
10.00
8.00
6.00
4.00
2.00
0.00
0.00
2.00
4.00
6.00
8.00
10.00

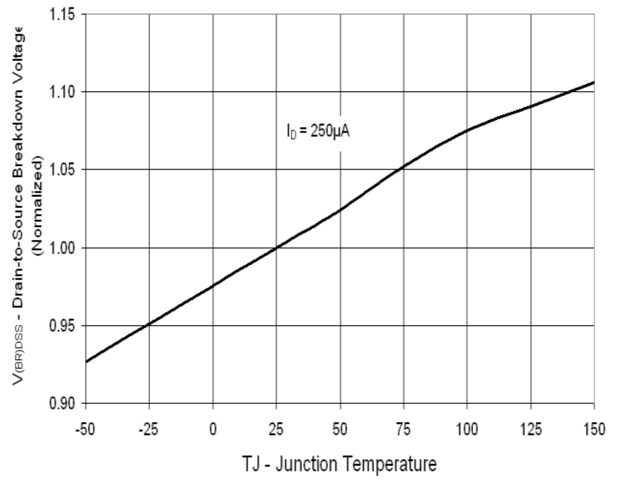

On State Resistance vs. Drain Current
V_GS = 10V
rDS(on) - On State Resistance (Ω)
I_D - Drain Current (A)
2.50
2.00
1.50
1.00
0.50
0.00
0.00
2.00
4.00
6.00
8.00
10.00

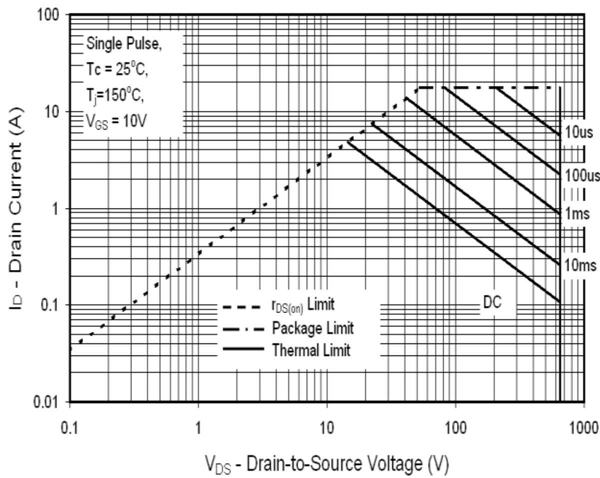

On State Resistance vs. Junction Temperature
V_GS = 10V
I_D = 4.4A
rDS(on) - On State Resistance (Normalized)
T_J - Junction Temperature (°C)
3.0
2.5
2.0
1.5
1.0
0.5
0.0
-50
-25
0
25
50
75
100
125
150

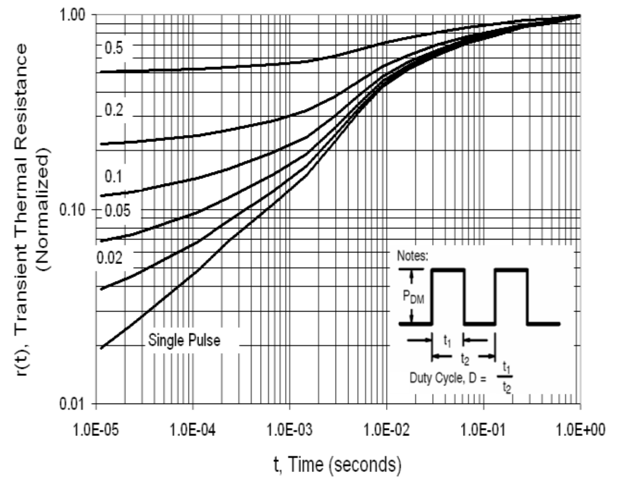

Gate Charge
V_DS = 400V
I_D = 4.4A
V_GS = 10V
V_GS - Gate-to-Source Voltage (V)
Q_g - Total Gate Charge (nC)
10.0
9.0
8.0
7.0
6.0
5.0
4.0
3.0
2.0
1.0
0.0
0
2
4
6
8
10
12
14

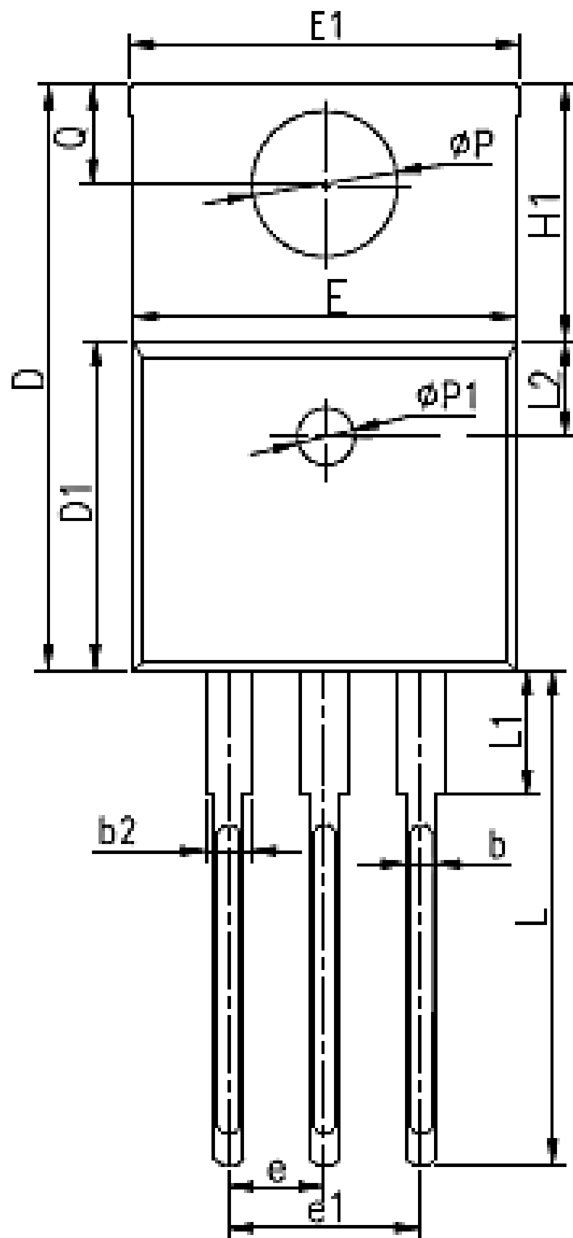

Gate Threshold Voltage vs. Junction Temperature
I_D = 250uA
V_GS(th) - Gate Threshold Voltage (Normalized)
TJ - Junction Temperature (°C)
1.3
1.2
1.1
1.0
0.9
0.8
0.7
0.6
0.5
0.4
-50
-25
0
25
50
75
100
125
150

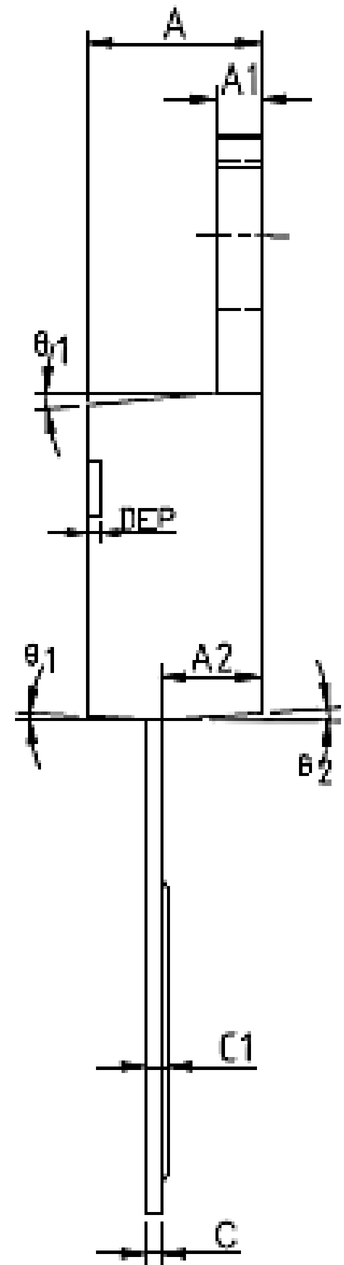

Capacitance
C - Capacitance (pF)
VDS - Drain-to-Source Voltage (V)
Ciss
Coss
Crss
1000
900
800
700
600
500
400
300
200
100
0
0
10
20
30
40
50

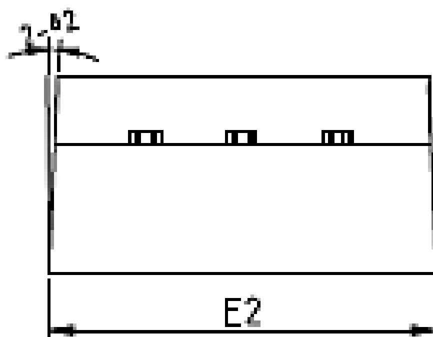

Drain-to-Source Breakdown Voltage vs. TJ
V(BR)DSS - Drain-to-Source Breakdown Voltage (Normalized)
TJ - Junction Temperature
ID = 250µA
1.15
1.10
1.05
1.00
0.95
0.90
-50
-25
0
25
50
75
100
125
150


Maximum Rated Forward Biased Safe Operating Area
ID - Drain Current (A)
VDS - Drain-to-Source Voltage (V)
Single Pulse,
Tc = 25°C,
Tj=150°C,
VGS = 10V
rDS(on) Limit
Package Limit
Thermal Limit
10us
100us
1ms
10ms
DC
100
10
1
0.1
0.01
0.1
1
10
100
1000


Transient Thermal Response, Junction-to-Case
r(t), Transient Thermal Resistance (Normalized)
t, Time (seconds)
0.5
0.2
0.1
0.05
0.02
Single Pulse
Notes:
PDM
t1
t2
Duty Cycle, D = t1/t2
1.00
0.10
0.01
1.0E-05
1.0E-04
1.0E-03
1.0E-02
1.0E-01
1.0E+00


E1
Q
øP
H1
E
D
øP1
L2
D1
L1
b2
b
L
e
e1


A
A1
θ1
DEP
θ1
A2
θ2
C1
C


E2

COMMON DIMENSIONS						
SYMBOL	MM			INCH		
	MIN	NOM	MAX	MIN	NOM	MAX
A	4.35	4.525	4.70	0.171	0.178	0.185
A1	1.20	1.30	1.40	0.047	0.512	0.055
A2	2.35	2.57	2.79	0.093	0.101	0.110
b	0.65	0.775	0.90	0.260	0.031	0.035
b2	1.00	1.18	1.36	0.039	0.046	0.054
c	0.34	0.381	0.47	0.013	0.015	0.019
c1	0.33	0.465	0.60	0.013	0.018	0.024
D	14.70	15.325	15.95	0.579	0.603	0.628
D1	8.60	9.025	9.45	0.339	0.355	0.372
E	9.96	10.16	10.36	0.392	0.400	0.408
E1	10.10	10.25	10.35	0.398	0.404	0.407
E2	10.00	10.10	10.20	0.394	0.398	0.402
e	2.54 BSC			0.100 BSC		
e1	5.08 BSC			0.200 BSC		
H1	6.10	6.30	6.50	0.240	0.248	0.256
L	12.70	13.35	14.00	0.520	0.526	0.551
L1	—	3.75	4.75	—	0.148	0.187
L2	2.50 REF			0.098 REF		
ΦP	3.55	3.715	3.88	0.140	0.146	0.153
Q	2.60	2.743	2.90	0.102	0.108	0.114
θ1	5°	7°	9°	5°	7°	9°
θ2	1°	3°	5°	1°	3°	5°
ΦP1	1.40	1.75	2.10	0.055	0.069	0.083
DEP	0.05	0.10	0.20	0.002	0.004	0.008

ICEMOS SUPERJUNCTION PATENT PORTFOLIO

ICEMOS GRANTED PATENTS

US7,429,772
US7,439,178
US7,446,018
US7,579,607
US7,723,172
US7,795,045
US7,846,821
US7,944,018
US8,012,806
US8,030,133

3D SEMI PATENTS LICENSED TO ICEMOS

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US7,023,069B2
US7,364,994
US7,227,197B2
US7,304,944B2
US7,052,982B2
US7,339,252
US7,410,891
US7,439,583
US7,227,197B2
US6,635,906
US6,936,867
US7,015,104
US9,109,110
US7,271,067
US7,354,818
US7,052,982,
US7,199,006B2

Note: additional patents in China, Korea, Japan, Taiwan, Europe have also been granted to IceMOS and 3D Semi for Superjunction MOSFETs with 70 additional Patent applications in process in the USA and the above listed countries.