FUJITSU

ECL 1024-BIT BIPOLAR RANDOM ACCESS MEMORY

MBM10423LL-6

October 1987
Edition 2.0

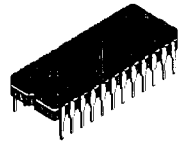
1024-BIT BIPOLAR ECL RANDOM ACCESS MEMORY

The Fujitsu MBM 10423LL is fully decoded 1024-bit ECL read/write random access memory designed for high speed scratch pad, control and buffer storage applications. This device is organized as 256 words by 4 bits with address input and output latches. Generally in the system, preceeding logic IC is needed for the synchronous entry of asynchronous address signal inputs of the RAM. MBM 10423LL contains internal latch circuits so that it can take synchronous address input and output timing, which contribute to higher system performance and save of power dissipation and board area. And it features on-chip voltage compensation for improved noise margin.

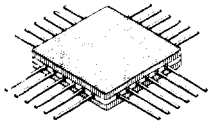
The MBM 10423LL offers extremely small cell and chip size, realized through the use of Fujitsu's patented DOPOS (Doped Polysilicon), as well as IOP-II (Isolation by Oxide and Polysilicon) processing.

Operation for the MBM 10423LL is specified over a temperature range of from 0°C to 75°C (T_A for DIP, T_C for Flat Package and LCC). It also features 24-pin Ceramic DIP, Flat Package, or LCC and is fully compatible with industry standard 10K-series ECL families.

- 256 words x 4 bits organization
- Address input and output latches which can be controlled separately
- On-chip voltage compensation for improved noise margin
- Fully compatible with industry standard 10K-series ECL families
- Latch cycle time: 6 ns max.
- Address access time: 5 ns max.
- Block select access time: 3 ns max.
- Open emitter output for ease of memory expansion
- Low power dissipation of 0.84 mW/bit
- DOPOS and IOP-II



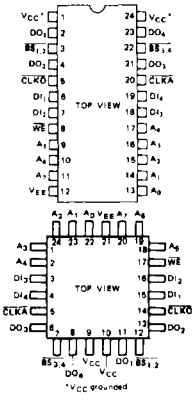
CERAMIC PACKAGE
DIP-24C-C05



CERAMIC PACKAGE
FPT-24C-C02

LCC-24C-F02: See Page 11

PIN ASSIGNMENT



LCC PAD CONFIGURATION: See Page 11

ABSOLUTE MAXIMUM RATINGS (See NOTE)

Rating	Symbol	Value	Unit
V_{EE} Pin Potential to Ground Pin	V_{EE}	+0.5 to -7.0	V
Input Voltage	V_{IN}	+0.5 to V_{EE}	V
Output Current (DC, Output High)	I_{OUT}	-30	mA
Temperature Under Bias	T_A for DIP	-55 to +125	°C
	T_C for Flat Package and LCC	-55 to +125	
Storage Temperature	T_{STG}	-65 to +150	°C

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

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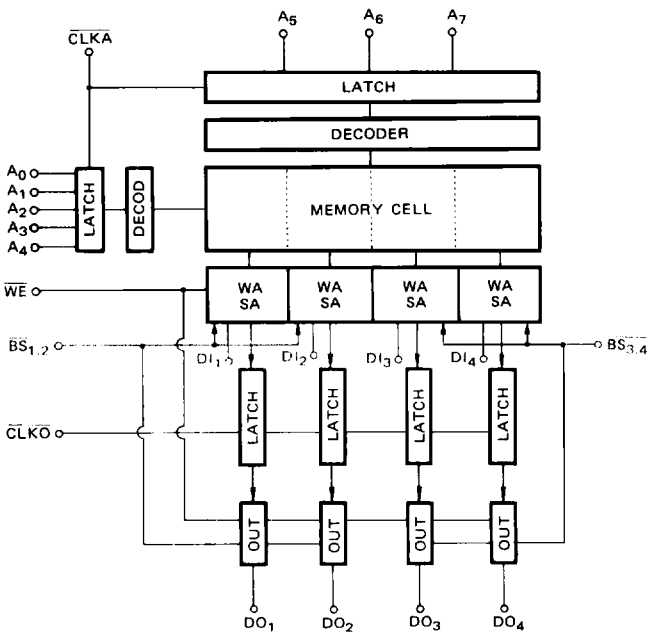
Fig. 1 – MBM 10423LL BLOCK DIAGRAM



Symbol	Pin Name	Symbol	Pin Name
$A_0 \sim A_7$	Address Input	$\overline{CLKA}$	Address Latch Clock
$DI_1 \sim DI_4$	Data Input	$\overline{CLKO}$	Output Latch Clock
$DO_1 \sim DO_4$	Data Output	V_{EE}	Power Supply (-5.2V)
$\overline{WE}$	Write Enable	V_{CC}	Power Supply (0V)
$\overline{BS_{1,2}}, \overline{BS_{3,4}}$	Block Select		

FUNCTIONAL DESCRIPTION

The Fujitsu MBM 10423LL is fully decoded 1024 bit read/write random access memory organized as 256 words by 4 bits with address input and output latches which can be controlled separately by $\overline{CLKA}$ and $\overline{CLKO}$ pins. When clock is in high state, data is latched, while clock is held low, data goes through the latches like as conventional MBM 10422A. Memory cell selection is achieved by means of a 8-bit address designated A_0 through A_7. The active low Block Select inputs are provided for memory expansion. Two separate blocks are selected simultaneously by $\overline{BS_{1,2}}$ or $\overline{BS_{3,4}}$ pin. The read and write operation are controlled by the state of active low Write Enable ($\overline{WE}$) input. With $\overline{WE}$, $\overline{BS_{1,2}}$ and/or $\overline{BS_{3,4}}$ held low, the data at DIN is written into the addressed location. To read, $\overline{WE}$ is held high, while $\overline{BS_{1,2}}$ and/or $\overline{BS_{3,4}}$ is held low. Data at the addressed location is then transferred to D_{OUT} and read out non-inverted Open emitter outputs are provided to allow for maximum flexibility in output wired-OR connection.

GUARANTEED OPERATING CONDITIONS

(Referanced to V_{CC})

Parameter	Symbol	Min	Typ	Max	Unit	Ambient Temperature for DIP, Case Temperature for Flat Package and LCC
Supply Voltage	V_{EE}	-5.46	-5.2	-4.94 V	V	0°C to 75°C

DC CHARACTERISTICS

(V_{CC} = 0 V, V_{EE} = -5.2 V, Output Load = 50 Ω to -2.0V, T_A = 0°C to 75°C for DIP, Airflow ≧ 2.5 m/s, T_C = 0°C to 75°C for flat package and LCC, unless otherwise noted.)

Parameter	Symbol	Min	Typ	Max	Unit	T_A/T_C
Output High Voltage (V_{IN} = $V_{IH\ max}$ or $V_{IL\ min}$)	V_{OH}	-1000 -960 -900		-840 -810 -720	mV	0°C 25°C 75°C
Output Low Vcltage (V_{IN} = $V_{IH\ max}$ or $V_{IL\ min}$)	V_{OL}	-1870 -1850 -1830		-1665 -1650 -1625	mV	0°C 25°C 75°C
Output High Voltage ($V_{IN\ min}$ or $V_{IL\ max}$)	V_{OHC}	-1020 -980 -920			mV	0°C 25°C 75°C
Output Low Voltage (V_{IN} = $V_{IH\ min}$ or $V_{IL\ max}$)	V_{OLC}			-1645 -1630 -1605	mV	0°C 25°C 75°C
Input High Voltage (Guaranteed Input Voltage High for All Inputs)	V_{IH}	-1145 -1105 -1045		-840 -810 -720	mV	0°C 25°C 75°C
Input Low Voltage (Guaranteed Input Voltage Low for All Inputs)	V_{IL}	-1870 -1850 -1830		-1490 -1475 -1450	mV	0°C 25°C 75°C
Input High Current (V_{IN} = $V_{IH\ max}$)	I_{IH}			220	μA	0°C to 75°C
Input Low Current (V_{IN} = $V_{IL\ min}$)	I_{IL}	-50			μA	0°C to 75°C
$\overline{BS}$ and $\overline{CLKA}$ Input Low Current (V_{IN} = $V_{IL\ min}$)	I_{IL}	0.5		170	μA	0°C to 75°C
Power Supply Current (All Inputs and Output Open)	I_{EE}	-220			mA	0°C to 75°C

CAPACITANCE

Parameter	Symbol	Min	Typ	Max	Unit
Input Pin Capacitance	C_{IN}		4	6	pF
Output Pin Capacitance	C_{OUT}		6	7	pF

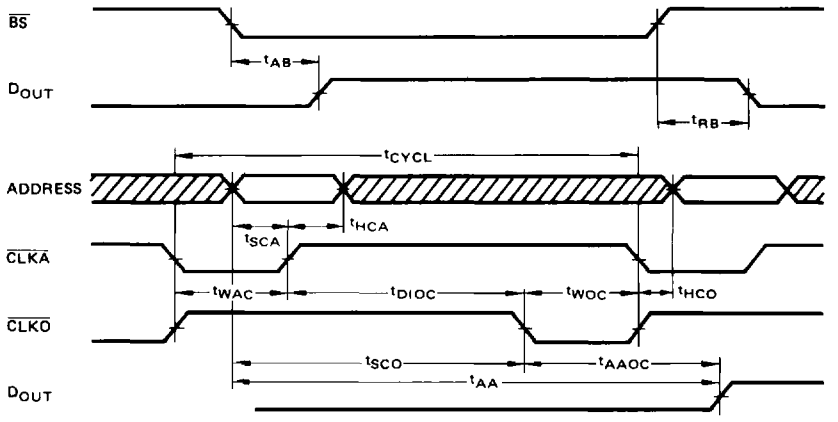
AC CHARACTERISTICS

(V_{CC} = 0V, V_{EE} = −5.2V ± 5%, Output Load = 50Ω to −2.0V and 30pF to GND, T_A = 0°C to 75°C for DIP, Airflow ≥ 2.5m/s, T_C = 0°C to 75°C for Flatpackage and LCC, unless otherwise noted.)

READ CYCLE

Parameter	Symbol	Min	Typ	Max	Unit
Address Access Time	t_{AA}	1.5		5.0	ns
Output Latch Access Time	t_{AAOC}	0.5		3.0	ns
Block Select Access Time	t_{AB}	0.5		3.0	ns
Block Select Recovery Time	t_{RB}	0.5		3.0	ns
Address Latch Clock Pulse Width	t_{WAC}	2.5			ns
Output Latch Clock Pulse Width	t_{WOC}	2.5			ns
Address Latch Clock Setup Time	t_{SCA}	1.5			ns
Address Latch Clock Hold Time	t_{HCA}	2.0			ns
Output Latch Clock Setup Time	t_{SCO}	2.5			ns
Output Latch Clock Hold Time	t_{HCO}	1.0			ns
Delay Time Between Input Clock and Output Clock	t_{DIOC}	1.0			ns
Latch Cycle Time	t_{CYCL}	6.0			ns

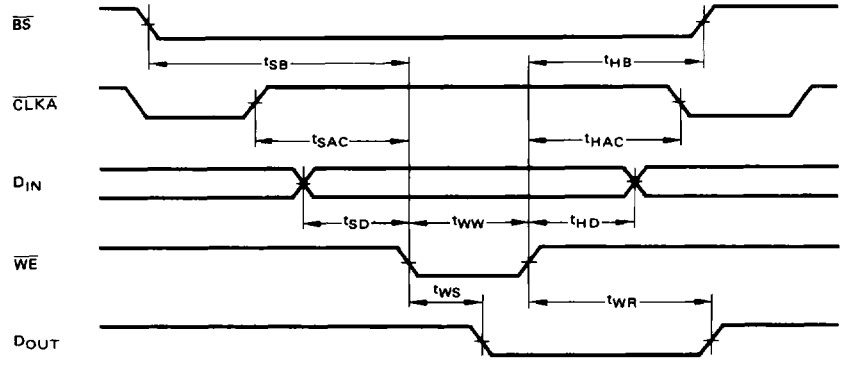
READ CYCLE TIMING DIAGRAM



WRITE CYCLE

Parameter	Symbol	Min	Typ	Max	Unit
Write Pulse Width	t_{WW}	3.5			ns
Write Disable Time	t_{WS}	0.5		3.5	ns
Write Recovery Time	t_{WR}	0.5		3.5	ns
Write Clock Setup Time	t_{SAC}	-1.5			ns
Block Select Setup Time	t_{SB}	0.5			ns
Data Setup Time	t_{SD}	0.5			ns
Write Clock Hold Time	t_{HAC}	1.5			ns
Block Select Hold Time	t_{HB}	1.0			ns
Data Hold Time	t_{HD}	1.0			ns

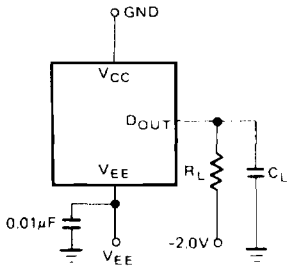
WRITE CYCLE TIMING DIAGRAM

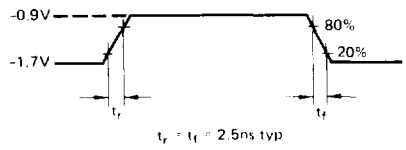


RISE TIME and FALL TIME

Parameter	Symbol	Min	Typ	Max	Unit
Output Rise Time	t_r		1.5		ns
Output Fall Time	t_f		1.5		ns

Fig. 2 – AC TEST CONDITIONS





Output Load: $R_L = 50\Omega$
$C_L = 30$pF
(including jig and stray capacitance)

NOTE: All timing measurements referenced to 50% input levels.

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FUNCTIONAL TRUTH TABLE

$\overline{BS}$	$\overline{WE}$	DI	$\overline{CLKA}$	$\overline{CLKO}$	OUTPUT	MODE
H	X	X	X	X	L	DISABLED
L	L	L	L	L	L	THROUGH, WRITE "L"
L	L	H	L	L	L	THROUGH, WRITE "H"
L	H	X	L	L	DO	THROUGH, READ
L	L	L	H	X	L	LATCHED, WRITE "L"
L	L	H	H	X	L	LATCHED, WRITE "H"
L	H	X	H	L	DO^{-I}	LATCHED, READ
L	H	X	X	H	DO^{-O}	LATCHED, READ

L : Low Voltage Level
H : High Voltage Level
X : Don't care
DO^{-I} : Data Out at the Location Addressed Before $\overline{CLKA}$ Goes From "L" to "H"
DO^{-O} : Data Out at the Location Addressed Before $\overline{CLKO}$ Goes From "L" to "H"

TYPICAL CHARACTERISTICS CURVES

Fig. 3 – OUTPUT HIGH VOLTAGE vs AMBIENT TEMPERATURE

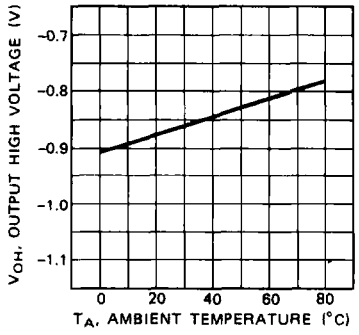

Fig. 4 – OUTPUT HIGH VOLTAGE vs SUPPLY VOLTAGE

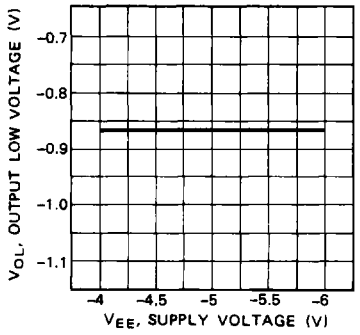

Fig. 5 – OUTPUT LOW VOLTAGE vs AMBIENT TEMPERATURE

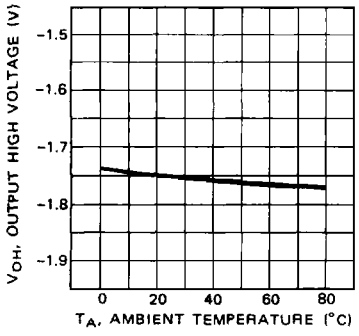

Fig. 6 – OUTPUT LOW VOLTAGE vs SUPPLY VOLTAGE

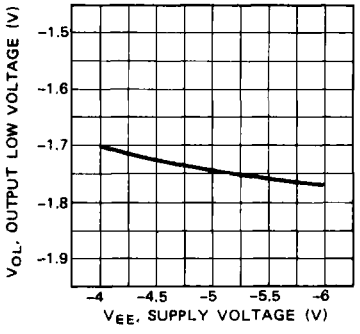

Fig. 7 – SUPPLY CURRENT vs AMBIENT TEMPERATURE

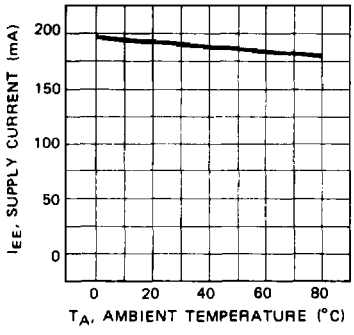

Fig. 8 – SUPPLY CURRENT vs SUPPLY VOLTAGE

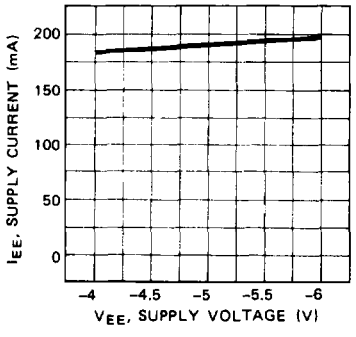

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Fig. 9 – ADDRESS ACCESS TIME vs AMBIENT TEMPERATURE

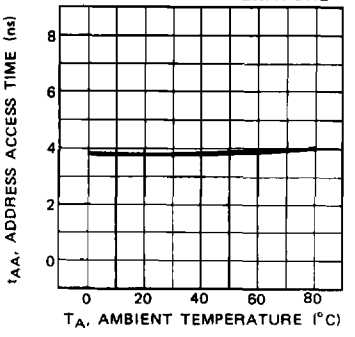


Fig. 10 – ADDRESS ACCESS TIME vs SUPPLY VOLTAGE

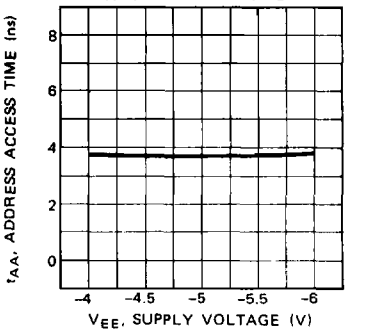


Fig. 11 – WRITE PULSE WIDTH vs AMBIENT TEMPERATURE

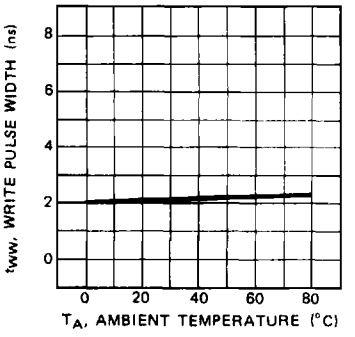
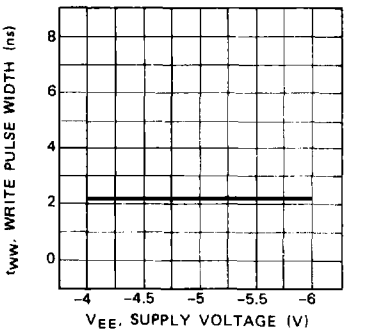


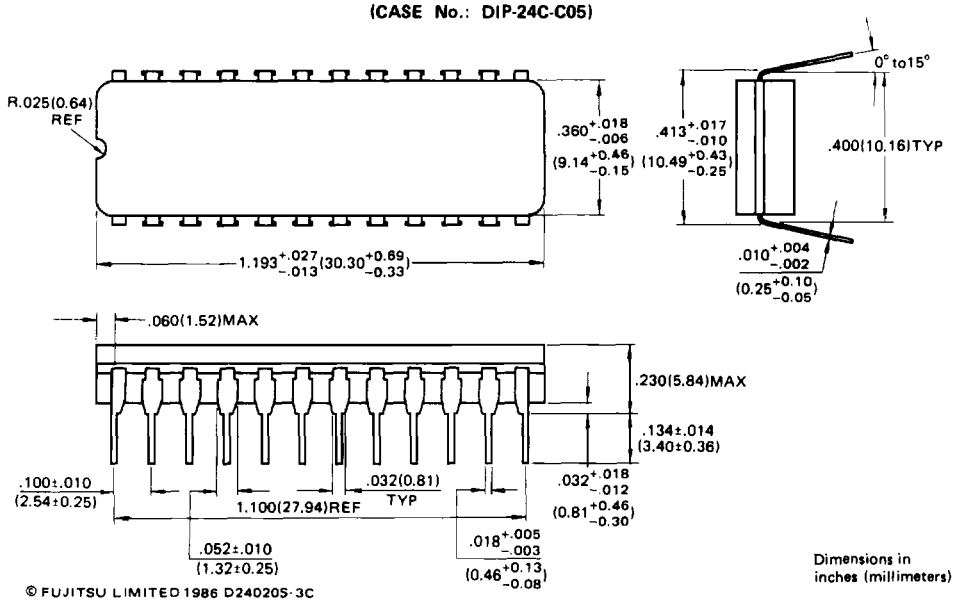
Fig. 12 – WRITE PULSE WIDTH vs SUPPLY VOLTAGE



PACKAGE DIMENSIONS

CERAMIC DIP (: -CZ)

24-LEAD CERAMIC (CERDIP) DUAL IN-LINE PACKAGE
(CASE No.: DIP-24C-C05)



Dimensions in
inches (millimeters)

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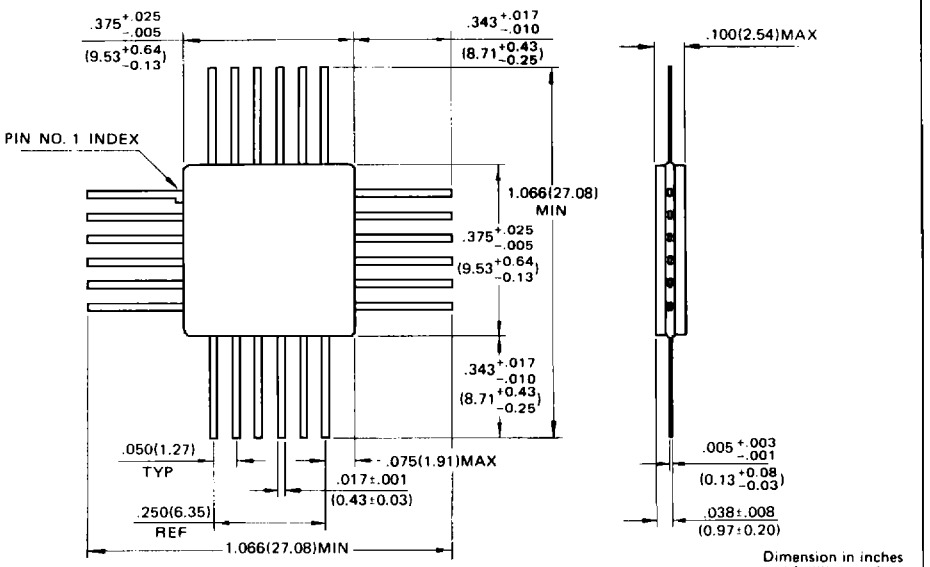
PACKAGE DIMENSIONS

CERAMIC FPT (: -ZF)

24-LEAD CERAMIC AXIAL LEADED FLAT PACKAGE
(CASE No.: FPT-24C-C02)



Dimension in inches
and (millimeters)

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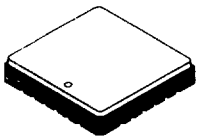
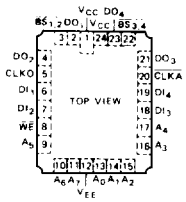
PACKAGE DIMENSIONS

CERAMIC LCC (: -TV)

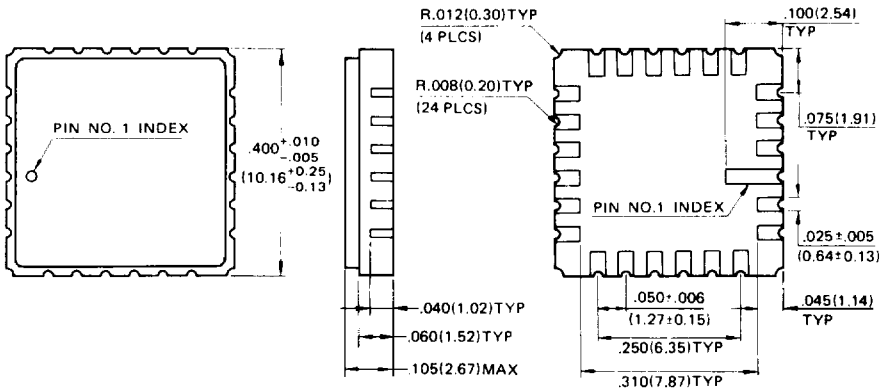


LCC-24C-F02

PAD CONFIGURATION



24-PAD CERAMIC (FRIT SEAL) LEADLESS CHIP CARRIER
(CASE No.: LCC-24C-F02)



Dimensions in inches
(millimeters)

3