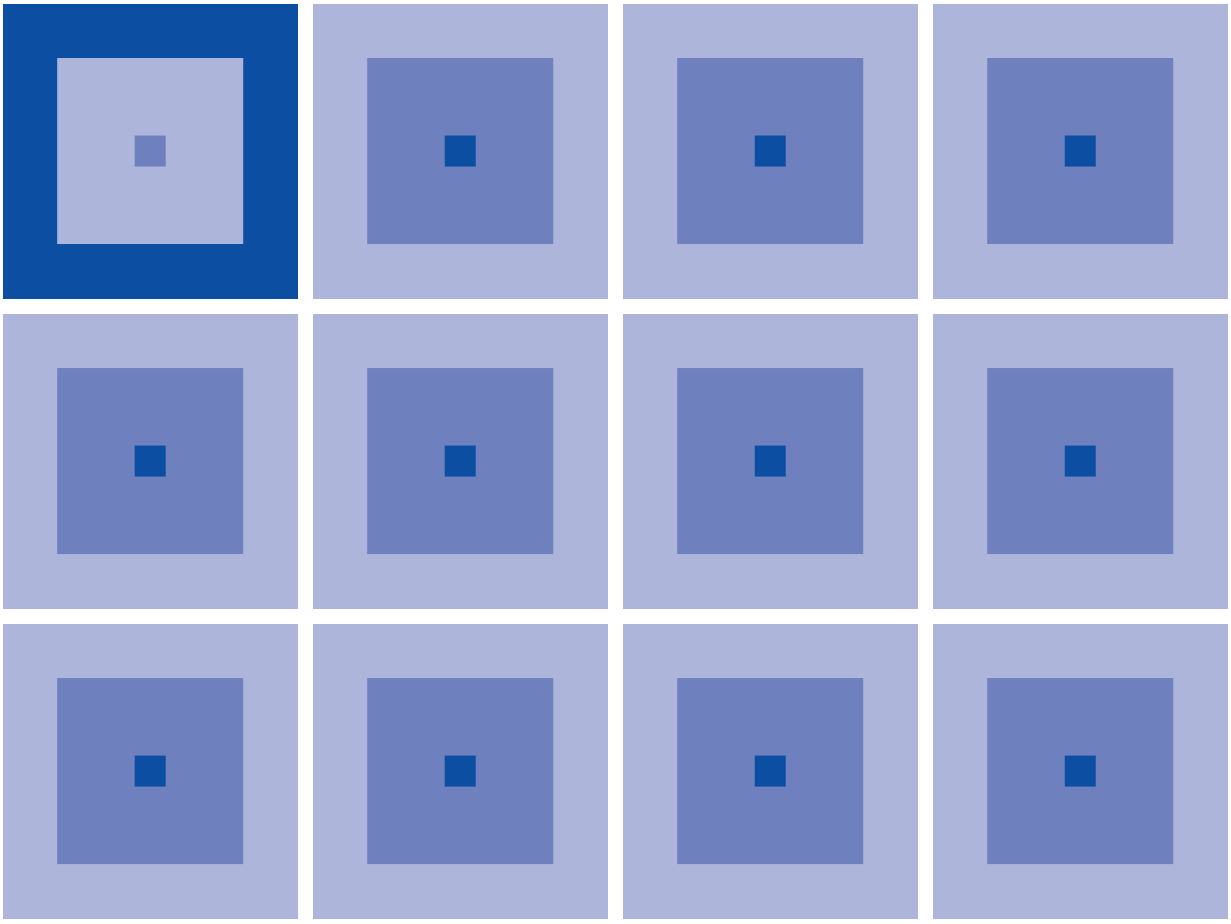
MF1403-01

EPSON

STANDARD CELL

S1K50000 Series
DESIGN GUIDE



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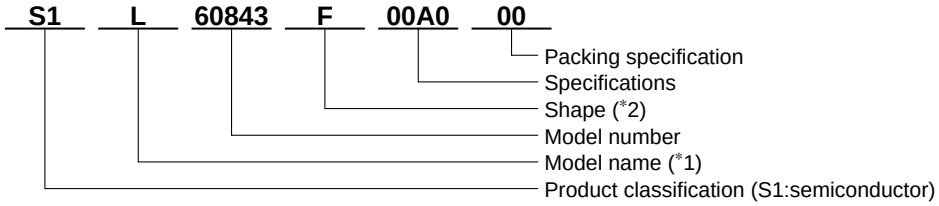
New configuration of product number

Starting April 1, 2001 the configuration of product number descriprions will be changed as listed below. To order from April 1, 2001 please use these product numbers. For further information, please contact Epson sales representative.

Configuration of product number

● DEVICES



*1 : Model name

K	Standard Cell
L	Gate Array
X	Embedded Array

*2 : Shape

B	Assembled on board, COB, BGA
C	Plastic DIP
D	Bare Chip
F	Plastic QFP
H	Ceramic DIP
L	Ceramic QFP

M	Plastic SOP
R	TAB–QFP
T	Tape Carrier (TAB)
2	TSOP (Standard Bent)
3	TSOP (Reverse Bent)

S1K50000 Series Table of Contents

Chapter 1 Overview

Seiko Epson's S1K50000 series consists of high-function, high-integrated CMOS standard cells based on the 0.35-micron process.

1.1 Features

- High degree of integration
  Maximum of 1,456,000 gates (2-input NAND gate equivalents)
- Operating speed
  Internal gate: 136 ps (3.3 V typ.), 224 ps (2.0 V typ.) (2-input POWER NAND, standard wiring load)
  Input buffer: 380 ps (5.0 V typ.) using a level shifter, 400 ps (3.3 V typ.), 1.30 ns (2.0 V typ.) (standard wiring load)
  Output buffer: 2.12 ns (5.0 V typ.) using a level shifter, 2.02 ns (3.3 V typ.), 3.90 ns (2.0 V typ.) (CL = 15 pF)
- Process
  CMOS 0.35-µm Al 3/4-layer metalization
- I/F level
  Input/output TTL-, CMOS-, and LVTTL-compatible
- Input mode
  TTL, CMOS, LVTTL, TTL Schmitt, CMOS Schmitt, LVTTL Schmitt, and PCI
  Internal pull-up and pull-down resistors available (two resistance values each)
- Output mode
  Normal, tri-state, bidirectional, or PCI
- Drive output
  I_{OL} = 0.1 mA, 1 mA, 3 mA, 8 mA, 12 mA, or 24 mA selectable (when a 5.0-V level shifter is used)
  I_{OL} = 0.1 mA, 1 mA, 2 mA, 6 mA, or 12 mA selectable (at 3.3 V)
  I_{OL} = 0.05 mA, 0.3 mA, 0.6 mA, 2 mA, or 4 mA selectable (at 2.0 V)
- Supports dual-power-supply operation using an internal level shifter
  (Internal logic: low-voltage operation; input/output buffers: high- and low-voltage interfaces usable in combination)
- Capable of operating with V_{DD} = 2.0 V ± 0.2 V

1.2 Electrical Characteristics

Table 1-1 Absolute Maximum Ratings (for a Single Power Supply)

Parameter	Symbol	Rated Value	Unit
Power-Supply Voltage	V_{DD}	-0.3 to 4.0	V
Input Voltage	V_I	-0.3 to V_{DD} + 0.5*1	V
Output Voltage	V_O	-0.3 to V_{DD} + 0.5*1	V
Output Current per Pin	I_{OUT}	± 30	mA
Storage Temperature	T_{STG}	-65 to 150	°C

*1: This applies to N-channel open-drain, bidirectional buffers, as well as XIDC and XIDH input buffers. For Fail-Safe cells, a value in the range from -0.3 V to 7.0 V is acceptable.

Table 1-2 Absolute Maximum Ratings (for Dual Power Supplies)

Parameter	Symbol	Rated Value	Unit
Power-Supply Voltage	HV_{DD}*3	-0.3 to 7.0	V
	LV_{DD}*3	-0.3 to 4.0	V
Input Voltage	HV_I	-0.3 to HV_{DD} + 0.5*1	V
	LV_I	-0.3 to LV_{DD} + 0.5*1	V
Output Voltage	HV_O	-0.3 to HV_{DD} + 0.5*1	V
	LV_O	-0.3 to LV_{DD} + 0.5*1	V
Output Current per Pin	I_{OUT}	± 30 (± 50*2)	mA
Storage Temperature	T_{STG}	-65 to 150	°C

*1: This applies to N-channel open-drain bidirectional buffers, as well as XLIDC and XLIDH or XHIDC and XHIDH input buffers. For Fail-Safe cells, a value in the range from -0.3 V to 7.0 V is acceptable.

*2: This applies to buffers with an output current of 24 mA.

*3: $HV_{DD} \geq LV_{DD}$

Table 1-3-1 Recommended Operating Conditions (for a Single Power Supply)

Parameter	Symbol	Min.	Typ.	Max.	Unit
Power-Supply Voltage	V_{DD}	3.00	3.30	3.60	V
Input Voltage	V_I	V_{SS}	—	V_{DD}*1	V
Ambient Temperature	Ta	0 -40	25 25	70*2 85*3	°C
Normal Input Rising Time	t_{ri}	—	—	50	ns
Normal Input Falling Time	t_{fa}	—	—	50	ns
Schmitt Input Rising Time	t_{ri}	—	—	5	ms
Schmitt Input Falling Time	t_{fa}	—	—	5	ms

*1: This applies to N-channel open-drain bidirectional buffers, as well as XIDC and XIDH input buffers. For Fail-Safe cells, a value of 5.25 V or 5.50 V is acceptable.

*2: This temperature range refers to the recommended ambient temperature in cases where Tj = 0 to 85 [°C].

*3: This temperature range refers to the recommended ambient temperature in cases where Tj = -40 to 125 [°C].

Table 1-3-2 Recommended Operating Conditions (for a Single Power Supply)

Parameter	Symbol	Min.	Typ.	Max.	Unit
Power-Supply Voltage	V_{DD}	1.80	2.00	2.20	V
Input Voltage	V_I	V_{SS}	—	V_{DD}*1	V
Ambient Temperature	Ta	0 -40	25 25	70*2 85*3	°C
Normal Input Rising Time	t_{ri}	—	—	100	ns
Normal Input Falling Time	t_{fa}	—	—	100	ns
Schmitt Input Rising Time	t_{ri}	—	—	10	ms
Schmitt Input Falling Time	t_{fa}	—	—	10	ms

*1: This applies to N-channel open-drain bidirectional buffers, as well as XIDC and XIDH input buffers. For Fail-Safe cells, a value of 5.25 V or 5.50 V is acceptable.

*2: This temperature range refers to the recommended ambient temperature in cases where Tj = 0 to 85 [°C].

*3: This temperature range refers to the recommended ambient temperature in cases where Tj = -40 to 125 [°C].

Table 1-4-1 Recommended Operating Conditions (for Dual Power Supplies)

Parameter	Symbol	Min.	Typ.	Max.	Unit
Power-Supply Voltage (High Voltage)	HV_{DD}	4.75 4.50	5.00 5.00	5.25 5.50	V
Power-Supply Voltage (Low Voltage)	LV_{DD}	3.00	3.30	3.60	V
Input Voltage	HV_I	V_{SS}	—	HV_{DD}	V
	LV_I	V_{SS}	—	LV_{DD}*1	
Ambient Temperature	Ta	0 -40	25 25	70*2 85*3	°C
Normal Input Rising Time	t_{ri}	—	—	50	ns
Normal Input Falling Time	t_{fa}	—	—	50	ns
Schmitt Input Rising Time	t_{ri}	—	—	5	ms
Schmitt Input Falling Time	t_{fa}	—	—	5	ms

*1: This applies to N-channel open-drain bidirectional buffers, as well as XLIDC and XLIDH input buffers. For Fail-Safe cells, a value of 5.25 V or 5.50 V is acceptable.

*2: This temperature range refers to the recommended ambient temperature in cases where Tj = 0 to 85 [°C].

*3: This temperature range refers to the recommended ambient temperature in cases where Tj = -40 to 125 [°C].

Table 1-4-2 Recommended Operating Conditions (for Dual Power Supplies)

Parameter	Symbol	Min.	Typ.	Max.	Unit
Power-Supply Voltage (High Voltage)	HV_{DD}	3.00	3.30	3.60	V
Power-Supply Voltage (Low Voltage)	LV_{DD}	1.80	2.00	2.20	V
Input Voltage	HV_I	V_{SS}	—	HV_{DD}*1	V
	LV_I	V_{SS}	—	LV_{DD}*1	
Ambient Temperature	Ta	0 -40	25 25	70*2 85*3	°C
Normal Input Rising Time	Ht_{ri}	—	—	50	ns
	Lt_{ri}	—	—	100	
Normal Input Falling Time	Ht_{fa}	—	—	50	ns
	Lt_{fa}	—	—	100	
Schmitt Input Rising Time	Ht_{ri}	—	—	5	ms
	Lt_{ri}	—	—	10	
Schmitt Input Falling Time	Ht_{fa}	—	—	5	ms
	Lt_{fa}	—	—	10	

*1: This applies to N-channel open-drain bidirectional buffers, as well as XLIDC and XLIDH or XHIDC and XHIDH input buffers. For Fail-Safe cells, a value of 5.25 V or 5.50 V is acceptable.

*2: This temperature range refers to the recommended ambient temperature in cases where Tj = 0 to 85 [°C].

*3: This temperature range refers to the recommended ambient temperature in cases where Tj = -40 to 125 [°C].

Table 1-5 Electrical Characteristics

(HV_{DD} = 5 V common; V_{SS} = 0 V; Ta = -40°C to 85°C)

Parameter	Symbol	Test Conditions		Min.	Typ.	Max.	Unit
Input Leakage Current	I_{LI}	—		-1	—	1	µA
Off-State Leakage Current	I_{OZ}	—		-1	—	1	µA
High-Level Output Voltage	V_{OH}	I_{OH} = -0.1 mA (Type S), -1 mA (Type M) -3 mA (Type 1), -8 mA (Type 2) -12 mA (Type 3, Type 4) HV_{DD} = Min.		HV_{DD} -0.4	—	—	V
Low-Level Output Voltage	V_{OL}	I_{OL} = 0.1 mA (Type S), 1 mA (Type M) 3 mA (Type 1), 8 mA (Type 2) 12 mA (Type 3), 24 mA (Type 4) HV_{DD} = Min.		—	—	0.4	V
High-Level Input Voltage	V_{IH1}	CMOS level, HV_{DD} = Max.		3.5	—	—	V
Low-Level Input Voltage	V_{IL1}	CMOS level, HV_{DD} = Min.		—	—	1.0	V
Positive Trigger Voltage	V_{T1+}	CMOS Schmitt		2.0	—	4.0	V
Negative Trigger Voltage	V_{T1-}	CMOS Schmitt		0.8	—	3.1	V
Hysteresis Voltage	V_{H1}	CMOS Schmitt		0.3	—	—	V
High-Level Input Voltage	V_{IH2}	TTL level, HV_{DD} = Max.		2.0	—	—	V
Low-Level Input Voltage	V_{IL2}	TTL level, HV_{DD} = Min.		—	—	0.8	V
Positive Trigger Voltage	V_{T2+}	TTL Schmitt		1.2	—	2.4	V
Negative Trigger Voltage	V_{T2-}	TTL Schmitt		0.6	—	1.8	V
Hysteresis Voltage	V_{H2}	TTL Schmitt		0.1	—	—	V
High-Level Input Voltage*2	V_{IH3}	PCI level, HV_{DD} = Max.		2.0	—	—	V
Low-Level Input Voltage*2	V_{IL3}	PCI level, HV_{DD} = Min.		—	—	0.8	V
High-Level Output Voltage*2	I_{OH3}	For PCI, V_{OH} = 1.4 V, HV_{DD} = Min. V_{OH} = 3.1 V, HV_{DD} = Max.		-44 —	— —	— -142	mA mA
Low-Level Output Voltage*2	I_{OL3}	For PCI, V_{OL} = 2.20 V, HV_{DD} = Min. V_{OL} = 0.71 V, HV_{DD} = Max.		95 —	— —	— 206	mA mA
Pull-Up Resistance*1	R_{PU}	V_I = 0 V	Type 1	30	60	(120) 144	kΩ
			Type 2	60	120	(240) 288	
Pull-Down Resistance*1	R_{PD}	V_I = V_{DD}	Type 1	30	60	(120) 144	kΩ
			Type 2	60	120	(240) 288	
High-Level Hold Current	I_{BHH}	For bus hold, V_{IN} = 2.0 V HV_{DD} = Min.		—	—	-80	µA
Low-Level Hold Current	I_{BHL}	For bus hold, V_{IN} = 0.8 V HV_{DD} = Min.		—	—	33	µA
High-Level Reversing Current	I_{BHHO}	For bus hold, V_{IN} = 0.8 V HV_{DD} = Max.		-550	—	—	µA
Low-Level Reversing Current	I_{BHLO}	For bus hold, V_{IN} = 2.0 V HV_{DD} = Max.		330	—	—	µA
Input-Pin Capacitance	C_I	f = 1 MHz, HV_{DD} = 0 V		—	—	10	pF
Output-Pin Capacitance	C_O	f = 1 MHz, HV_{DD} = 0 V		—	—	10	pF
Input/Output-Pin Capacitance	C_{IO}	f = 1 MHz, HV_{DD} = 0 V		—	—	10	pF

*1: The values in ( ) apply to cases where Ta = 0°C to 70°C.

*2: Conforms to PCI standard Rev. 2.2

Table 1-6 Electrical Characteristics

(V_{DD} = LV_{DD} = 3.3 V ± 0.3 V, Vss = 0 V, Ta = -40 to 85°C)

Parameter	Symbol	Test Conditions		Min.	Typ.	Max.	Unit
Quiescent Current*1	I_{DDS}	Static state		—	—	170	µA
Input Leakage Current	I_{LI}	—		-1	—	1	µA
Off-State Leakage Current	I_{OZ}	—		-1	—	1	µA
High-Level Output Voltage	V_{OH}	I_{OH} = -0.1 mA (Type S), -1 mA (Type M) -2 mA (Type 1), -6 mA (Type 2) -12 mA (Type 3) V_{DD} = Min.		V_{DD} -0.4	—	—	V
Low-Level Output Voltage	V_{OL}	I_{OL} = 0.1 mA (Type S), 1 mA (Type M) 2 mA (Type 1), 6 mA (Type 2) 12 mA (Type 3) V_{DD} = Min.		—	—	0.4	V
High-Level Input Voltage	V_{IH1}	LVTTL level, V_{DD} = Max.		2.0	—	—	V
Low-Level Input Voltage	V_{IL1}	LVTTL level, V_{DD} = Min.		—	—	0.8	V
Positive Trigger Voltage	V_{T1+}	LVTTL Schmitt		1.1	—	2.4	V
Negative Trigger Voltage	V_{T1-}	LVTTL Schmitt		0.6	—	1.8	V
Hysteresis Voltage	V_{H1}	LVTTL Schmitt		0.1	—	—	V
High-Level Input Voltage*3	V_{IH3}	PCI level, V_{DD} = Max.		1.71	—	—	V
Low-Level Input Voltage*3	V_{IL3}	PCI level, V_{DD} = Min.		—	—	0.98	V
High-Level Output Voltage*3	I_{OH3}	For PCI, V_{OH} = 0.90 V, V_{DD} = Min. V_{OH} = 2.52 V, V_{DD} = Max.		-36 —	— —	— -115	mA
Low-Level Output Voltage*3	I_{OL3}	For PCI, V_{OL} = 1.80 V, V_{DD} = Min. V_{OL} = 0.65 V, V_{DD} = Max.		48 —	— —	— 137	mA
Pull-Up Resistance*2	R_{PU}	V_I = 0 V	Type 1	20	50	(100) 120	kΩ
			Type 2	40	100	(200) 240	
Pull-Down Resistance*2	R_{PD}	V_I = V_{DD}	Type 1	20	50	(100) 120	kΩ
			Type 2	40	100	(200) 240	
High-Level Hold Current	I_{BHH}	For bus hold, V_{IN} = 2.0 V V_{DD} = Min.		—	—	-20	µA
Low-Level Hold Current	I_{BHL}	For bus hold, V_{IN} = 0.8 V V_{DD} = Min.		—	—	17	µA
High-Level Reversing Current	I_{BHHO}	For bus hold, V_{IN} = 0.8 V V_{DD} = Max.		-350	—	—	µA
Low-Level Reversing Current	I_{BHLO}	For bus hold, V_{IN} = 2.0 V V_{DD} = Max.		210	—	—	µA
Input-Pin Capacitance	C_I	f = 1 MHz, V_{DD} = 0 V		—	—	10	pF
Output-Pin Capacitance	C_O	f = 1 MHz, V_{DD} = 0 V		—	—	10	pF
Input/Output-Pin Capacitance	C_{IO}	f = 1 MHz, V_{DD} = 0 V		—	—	10	pF

*1: The quiescent current represents the typical value for each series at Tj = 85°C. For details, see Tables 1-8 through 1-9.

*2: The values in ( ) apply to cases where Ta = 0°C to 70°C. For cases where HV_{DD} = 3.3 V + 0.3 V; V_{SS} = 0 V; Ta = -40°C to 85°C, each value should be doubled.

*3: Conforms to PCI standard Rev. 2.2

Table 1-7 Electrical Characteristics

(V_{DD} = LV_{DD} = 2.0 V ± 0.2 V, Vss = 0 V, Ta = -40 to 85°C)

Parameter	Symbol	Test Conditions		Min.	Typ.	Max.	Unit
Quiescent Current*1	I_{DDS}	Static state		—	—	150	µA
Input Leakage Current	I_{LI}	—		-1	—	1	µA
Off-State Leakage Current	I_{OZ}	—		-1	—	1	µA
High-Level Output Voltage	V_{OH}	I_{OH} = -0.05 mA (Type S), -0.3 mA (Type M) -0.6 mA (Type 1), -2 mA (Type 2) -4 mA (Type 3) V_{DD} = Min.		V_{DD} -0.2	—	—	V
Low-Level Output Voltage	V_{OL}	I_{OL} = 0.05 mA (Type S), 0.3 mA (Type M) 0.6 mA (Type 1), 2 mA (Type 2) 4 mA (Type 3) V_{DD} = Min.		—	—	0.2	V
High-Level Input Voltage	V_{IH1}	CMOS level, V_{DD} = Max.		1.6	—	—	V
Low-Level Input Voltage	V_{IL1}	CMOS level, V_{DD} = Min.		—	—	0.3	V
Positive Trigger Voltage	V_{T1+}	CMOS Schmitt		0.4	—	1.6	V
Negative Trigger Voltage	V_{T1-}	CMOS Schmitt		0.3	—	1.4	V
Hysteresis Voltage	V_{H1}	CMOS Schmitt		0	—	—	V
Pull-Up Resistance	R_{PU}	V_I = 0 V	Type 1	30	120	300	kΩ
			Type 2	60	240	600	
Pull-Down Resistance	R_{PD}	V_I = V_{DD}	Type 1	30	120	300	kΩ
			Type 2	60	240	600	
High-Level Hold Current	I_{BHH}	For bus hold, V_{IN} = 1.6 V V_{DD} = Min.		—	—	-2	µA
Low-Level Hold Current	I_{BHL}	For bus hold, V_{IN} = 0.3 V V_{DD} = Min.		—	—	2	µA
High-Level Reversing Current	I_{BHHO}	For bus hold, V_{IN} = 0.3 V V_{DD} = Max.		-100	—	—	µA
Low-Level Reversing Current	I_{BHLO}	For bus hold, V_{IN} = 1.6 V V_{DD} = Max.		100	—	—	µA
Input-Pin Capacitance	C_I	f = 1 MHz, V_{DD} = 0 V		—	—	10	pF
Output-Pin Capacitance	C_O	f = 1 MHz, V_{DD} = 0 V		—	—	10	pF
Input/Output-Pin Capacitance	C_{IO}	f = 1 MHz, V_{DD} = 0 V		—	—	10	pF

*1: The quiescent current represents the typical value for each series at Tj = 85°C. For details, see Tables 1-8 through 1-9.

Table 1-8 Quiescent Current (for a Single Power Supply)

(Tj = 85°C)

Parameter	3.3 V ± 0.3 V I_{DDS} Max.	2.0 V ± 0.2 V I_{DDS} Max.	Unit
Quiescent Current*1	35 to 260	31 to 230	µA

*1: Varies with the chip size and incorporated macro

Table 1-9 Quiescent Current (for Dual Power Supplies)

(Tj = 85°C)

Parameter	5 V ± 10% HI_{DDS} Max.	3.3 V ± 0.3 V LI_{DDS} Max.	3.3 V ± 0.3 V HI_{DDS} Max.	2.0 V ± 0.2 V LI_{DDS} Max.	Unit
Quiescent Current*1	30 to 80	35 to 260	25 to 60	31 to 230	µA

HI_{DDS}: Quiescent current between HV_{DD} and V_{SS}; LI_{DDS}: Quiescent current between LV_{DD} and V_{SS}

*1: Varies with the chip size and incorporated macro

For the quiescent current in cases where Tj = 85°C, an approximate value can be obtained using the equation below (Tj = -40°C to 85°C, however).

$$I_{DD}(Tj) = I_{DDS}(Tj = 85°C) \times \text{temperature coefficient}$$
$$= I_{DDS}(Tj = 85°C) \times 10^{\frac{Tj - 85}{60}}$$

(For cases where Tj = 125°C, calculate the above using temperature coefficient = 12.)

For dual power supplies, the sum of quiescent currents for the respective voltages used comprises a total quiescent current. (HI_{DDS} + LI_{DDS})

1.3 Outline of Standard-Cell Development Flow

The standard cells were developed through collaboration between Seiko Epson and its customers. Customers perform a range of work, from system and circuit designs to test-pattern design, using the cell libraries and various design materials offered by Seiko Epson.

For interfacing information, customers are expected to conduct preliminary checks based on the data-release checklist included in the appendix herein, and present the necessary data and documentation to Seiko Epson.

Customers are responsible for conducting simulations using the EDA software or Auklet* on hand; the remainder of the work, beginning with placement and routing, is undertaken by Seiko Epson.

Note) *1 : Auklet is Seiko Epson's ASIC design support system and can be run on MS Windows 95/98/NT.

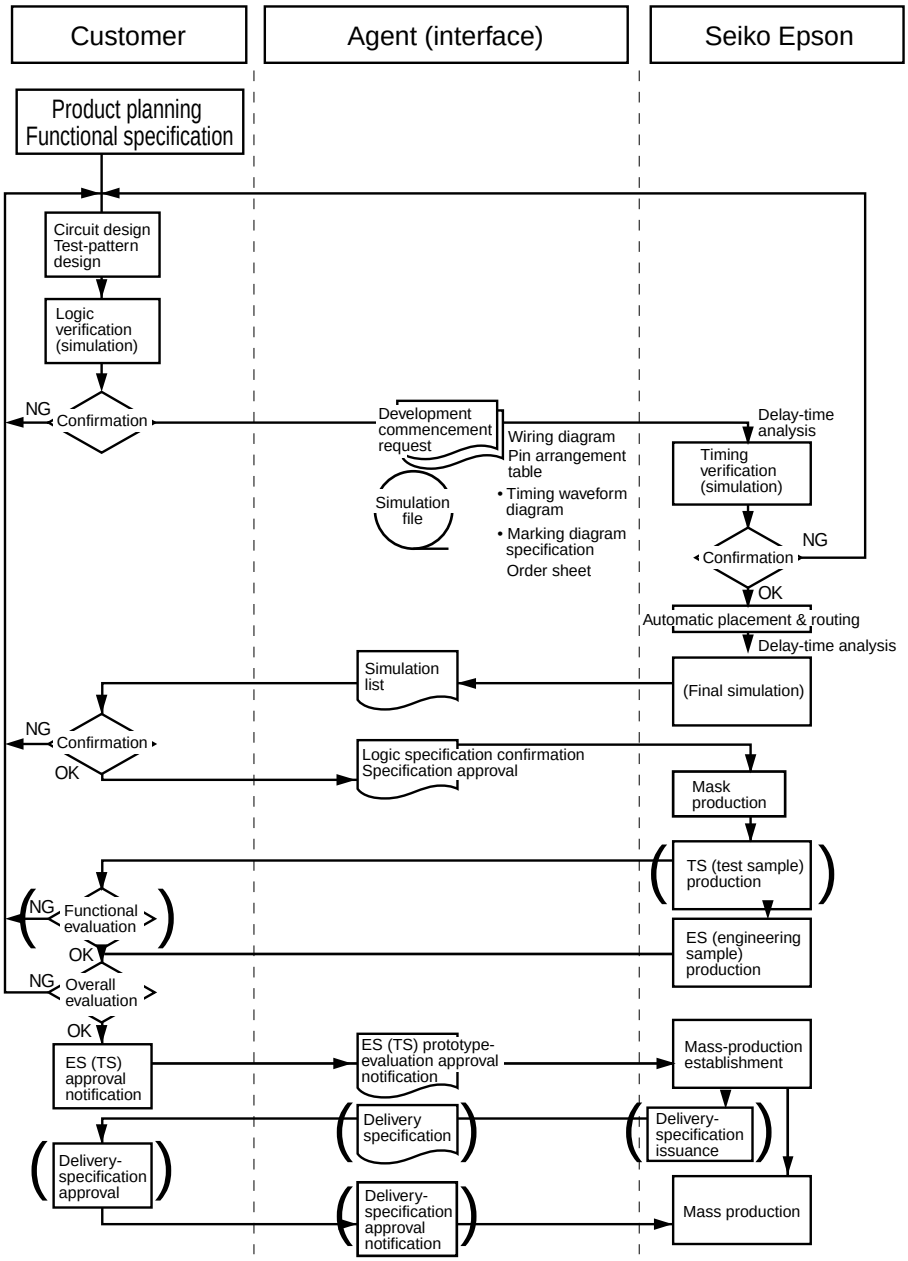
The following EDA software can currently be simulated:

- Verilog-XL (*1)
- VSS (*2)
- ModelSim (*3)

Note) *1 : Verilog-XL is a registered trademark of Cadence Design Systems of the U.S.
Note) *2 : VSS is a registered trademark of Synopsys of the U.S.
Note) *3 : ModelSim is a registered trademark of Model Technology of the U.S.

For details, please contact Seiko Epson or its distributor.

The diagram below shows the flow of the standard cell development procedure.



Those tasks enclosed in ( ) are undertaken when requested by the customer.

Chapter 2 Precautions on Circuit Design

2.1 Insertion of Input/Output Buffers

In the design of your circuit, always be sure to use input/output buffers to exchange signals with external devices. Because CMOS ICs are extremely susceptible to damage by static electricity, the input/output buffers contain protective circuits.

2.2 Use of Differentiating Circuits Inhibited

In LSIs, the tpd of each gate varies depending on the process dispersions during mass production or the operating environment. Therefore, differentiating circuits using the relative time difference of tpd like the one shown in Figure 2-1 cannot obtain a sufficient pulse width, causing the circuit to operate erratically.

When it is necessary to use a differentiating circuit, be sure to use one that utilizes flip-flops, rather than the one shown in Figure 2-1.

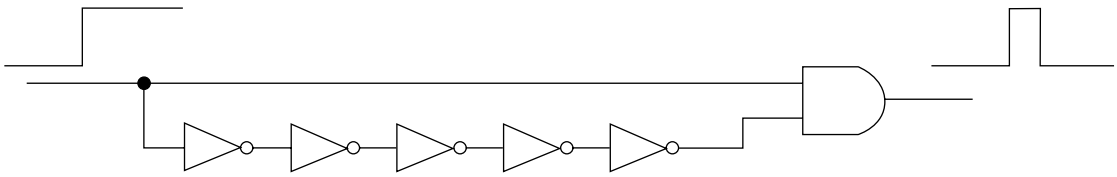


Figure 2-1 Example of a Differentiating Circuit

2.3 Wired Logic Inhibited

Because CMOS transistors are used, wired logic cannot be configured as in bipolar transistors. Therefore, the output pins of cells cannot be connected together, as shown in Figure 2-2. Output pins can only be connected together in a bus-circuit configuration.

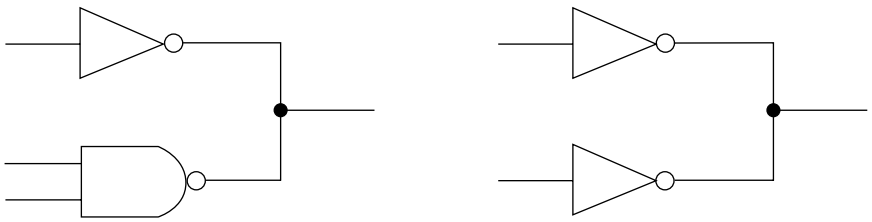


Figure 2-2 Example of Inhibited Wired Logic

2.4 Hazard Protection

In circuits or decoders configured by combining gates such as NAND or NOR gates, a very short pulse may be generated due to the difference in delay times between gates. This short pulse is known as a hazard, and it causes malfunction when fed into the clock or reset pins of flip-flips.

Therefore, circuits where such a hazard is likely to occur must be configured so as to prevent the hazard from propagating. For decoders, it may be necessary to use a circuit that has an enable pin.

2.5 Fan-Out Limitations

The tpd of logic gates is determined by the load capacitance of their output pin. An excessively large load capacitance may not only cause the tpd to become large, but may also cause malfunction. Therefore, there are limitations on the number of loads that can be connected to the output pins of each logic gate. These are known as “fan-out” limitations.

The input-pin capacitance of each logic gate, however, tends to differ depending on the logic-gate input. The input capacitance of each logic gate, in terms of the input capacitance of an inverter (KINI) = 1, is known as “fan-in.”

In the design of your circuit, make sure the total number of fan-ins connected to the output pins of each logic gate does not exceed the fan-out limitations of those output pins.

Furthermore, for logic gates operating at high speed, such as high-speed clock lines (fmax = 40 MHz or more), make sure the output-pin capacitance of those gates is approximately half the fan-out limitation.

2.6 Internal Bus Circuits

A bus circuit is configured with 3-state logic circuits, so one of the outputs connected to the bus can be driven active (while the other outputs are placed in the high-impedance state) by turning the bus control signals on or off.

In this way, a transmission-signal line on the bus is shared by dividing it in time. Although bus circuits are very effective for logic design, note the following when using a bus circuit.

Precautions on the use of bus circuits

(1) Bus cells can only be used for bus circuits (for the S1K50000-series bus cells, see Table 2-1).

(2) When using bus cells, add bus definition cells KBLT to the bus in the configuration of your circuit.

(3) Up to 32 bus cells can be connected to one length of bus.

(4) Of the bus cells connected to one length of bus, only one output can be active (0 or 1) at one time, and all other bus cell outputs must be placed in the high-impedance state (Z).

(5) Even when all of the bus cells connected to one length of bus are in the high-impedance state (Z), data may be retained by a bus latch cell. However, the retained data should be left floating, and should not be used as logic signals.

(6) In the creation of your test pattern, make sure the bus' initial state will settle easily, to ensure improved testability. In addition, add one or more test pins to make the bus easily controllable.

(7) The bus control signals within the same event rate can be switched only once.

(8) Excessive fan-out of the bus circuit may cause the propagation delay time to increase, making high-speed operation difficult.

The usable bus cells in the S1K50000 series are listed in Table 2-1.

Table 2-1 S1K50000-Series Bus Cells

Cell Type	Cell Name		
	1 BIT	4 BIT	8 BIT
Bus latches	KBLT 1	KBLT 4	KBLT 8
Bus driver	KTSB, KTSB4, KTSB8, KTSBP	KT244H	KT244
Inverting bus driver	KTSV, KTSV4, KTSV8, KTSVP	KT240H	KT240
Transparent latches with reset and 3-state output	—	KT373H	KT373
D-flip flops with rest and 3-state output	—	KT374H	KT374
1-bit RAM	KRM1	—	—

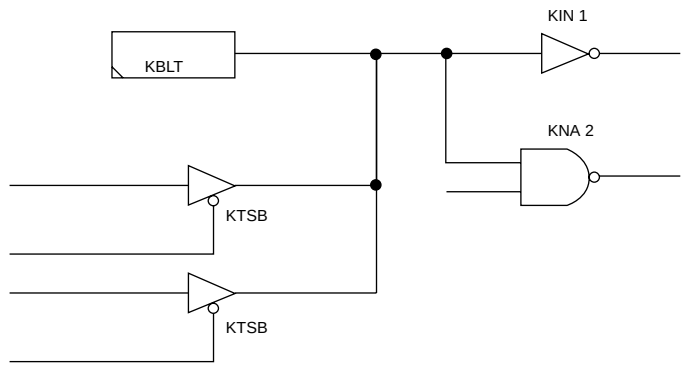


Figure 2-3 Typical Configuration of a Bus Cell Circuit

2.7 Bus Hold Circuits

Available with the S1K50000 series are input/output buffers with a bus hold function to hold the input/output-pin data in order to prevent the output pins or bidirectional pins from entering a high-impedance state.

However, because the retention capability of the bus hold circuit is repressed so as not to adversely affect normal bus operation, do not use the retained output as valid data. If any data is fed from an external device, the state of the data may change easily.

For details on the bus hold circuit's output retention current, see Tables 1-5 through 1-7.

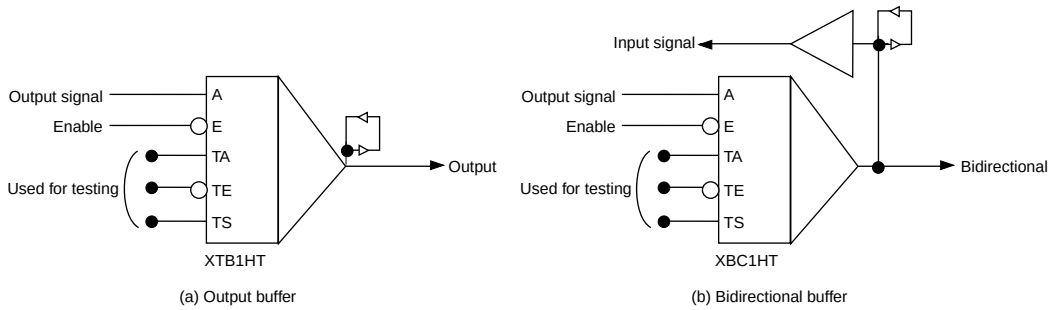


Figure 2-4 Typical Bus Hold Circuit Symbol

2.8 Precautions on Creating Circuit Diagrams (Logic Diagrams)

For diagram interfaces, circuit diagrams are normlly presented to Seiko Epson by the customer. In the creation of your circuit diagrams, note the following:

- For the Seiko Epson format, use the logic symbols listed in “Standard Cell S1K50000-Series MSI Cell Library.”
- Do not use the aslant wiring shown in the circuit diagram.
- To write input/output and bidirectional pin names, use 2 to 32 alphanumeric characters beginning with an English letter.

2.9 Clock Tree Synthesis

(1) Outline

Clock Tree Synthesis is a service that automatically inserts a tree of a set of buffers with optimized clock line skew and delay. In some cases, clock trees are inserted by the customers themselves for the purpose of clock line fan-out adjustment or the like. However, because in such a case trees are automatically placed and routed by P&R tools, the clock line may, in effect, have an increased clock skew. In addition, wiring delay may eventually be increased to a greater extent than predicted, as placement & routing and cell delays are often imbalanced. Clock Tree Synthesis solves all of these problems efficiently.

(2) Method of practice

Before a clock tree can be automatically inserted, the clock line must have a dedicated buffer inserted by the customer for the following three purposes:

- Determination of the location at which to apply Clock Tree Synthesis
- Performance of a preliminary routing-level simulation (pre-simulation) through estimation of the delay in the inserted clock tree
- Back annotation of the delay in the inserted clock tree to allow the performance of precise post-simulation

Choose the dedicated buffer for Clock Tree Synthesis from the table of dedicated buffers provided later. When inserting the selected dedicated buffer, handle it the same way as with ordinary cells by referring to the “image diagram,” in consideration of the “restrictions and precautions.” In addition, for logic-synthesis-based design, because the dedicated buffer cannot be automatically inserted, write the procedure using description language directly. At that time, execute the command specified below to ensure that another buffer will not be synthesized on the clock line in which the dedicated buffer has been inserted:

set_dont_touch_net *net_name*

[Dedicated buffers]

Choose the dedicated buffer from among those listed below, in accordance with the fan-out.

S1K50000 Series		
Cell Name	To Max. (ns)	Approximate Fan-Out Count
KCRBF2	2.00	0 to 500
KCRBF3	3.00	500 to 3000
KCRBF4	4.00	3000 to 10000
KCRBF5	5.00	Over 10000
KCRBF6	6.00	
KCRBF7	7.00	
KCRBF8	8.00	

Note 1: The K value of these cells (delay due to fan-out) is set to 0 in pre-simulation.

Note 2: The fan-out counts for these cells are set to infinity.

Note 3: The delay relative to the fan-out counts is only an approximate value for use as a guideline.

[Restrictions and precautions]

- Applicable series: S1L9000F, S1L30000, S1L35000, S1L50000, S1K50000
- The dedicated buffers can only be used for the purpose of Clock Tree Synthesis.
- Clock Tree Synthesis can also be applied to data lines or other control signals. However, if the number of nets to which Clock Tree Synthesis is applied increases, a large skew or delay may result. Therefore, limit the number of synthesized nets to 10, and limit the application of synthesis to critical nets with a large fan-out.
- The application of Clock Tree Synthesis to nets with a small fan-out may result in increased delay or skew. Apply synthesis only to nets that have a fan-out of several tens or more.
- Clock Tree Synthesis may also help to adjust the skew between multiple clock lines. In such a case, consult Seiko Epson after presenting a detailed block diagram (clearly showing the clock-line structure).
- For a set of clock lines that have the same clock root and are divided into multiple clock lines by gates or the like, “Gated Clock-Tree Synthesis Explanation Data” is separately required. In such a case, contact Seiko Epson.

[Required information]

To ensure the efficient use of Clock Tree Synthesis, please send the information specified below to Seiko Epson by the time data is released.

Instance Name of KCRBF*	Target Skew Value	Target Delay Value (Min./Max.)

Note 1: The target values are only approximate for use as guidelines in the application of synthesis, and it is not guaranteed that the values will be satisfied.

Note 2: If you do not have definite target values, specify your desired values by entering a comment (e.g., “as small as possible”).

[Image diagram]

Shown below is an example of a logic-circuit diagram to be presented by the customer and a layout-circuit diagram derived from it through the application of Clock Tree Synthesis at Seiko Epson.

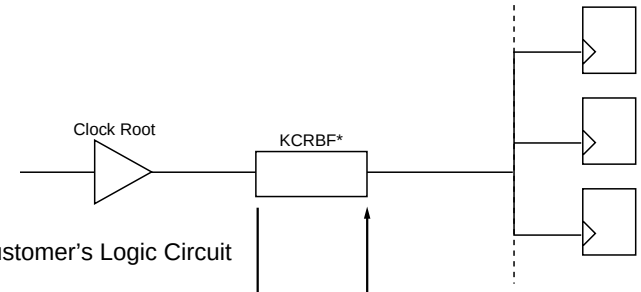


Figure 2-5 Customer's Logic Circuit

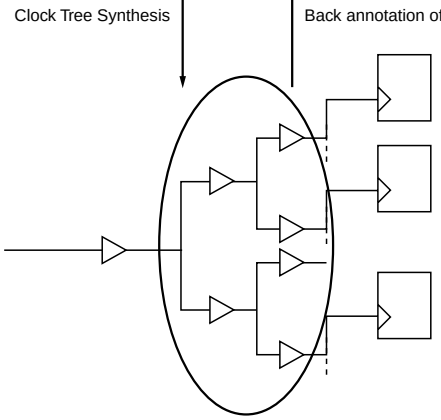


Figure 2-6 Layout Diagram Derived by Applying Clock Tree Synthesis at Seiko Epson

2.10 ATPG (Auto Test-Pattern Generation)

(1) Introduction

ATPG refers to automatic pattern generation, for which tools are released from each tool vendor. Testgen from Synopsys is used for ASIC design by Seiko Epson. Use of Testgen helps to automatically generate a test pattern following the insertion of scan circuits into the original circuit.

The word “control” as used in this manual means that any level can be applied to the target pin without being routed via a sequential circuit. That is, it does not refer to clocks, such as divided-by-N clocks, that require several cycles for status settings. For example, the description, “Each flip-flop can have its clock controlled from the outside” refers to a circuit in which an external input clock (clocking source) can reach each flip-flop.

(2) Outline

Scan insertion is executed on circuits that conform to the design rules required for ATPG support, and fault detection by ATPG is performed. In addition, because ATPG tools operate the internal nodes forcibly from external pins through a scan circuit, the test patterns output by ATPG tools cannot be used to observe operation of the user circuit. Therefore, customers are requested to create the test pattern necessary to verify the basic operation of the circuit. In other words, keep in mind that the test patterns generated by ATPG tools are used only for the purpose of increasing the fault detection rate. The use of ATPG tools helps to generate a test pattern that, for full-scan circuits, can attain a high fault detection rate of close to 100%, except for untestable nodes in which logical fault detection is impossible. Note that ATPG uses the full-scan method based on MUXSCAN-type flip-flops.

(3) Definition of the fault detection rate

The single-degeneracy fault mode is used.

SA0: Fixed (shorted) to 0
SA1: Fixed (shorted) to 1

The ATPG tool (TestGen) generates the test pattern shown below.

A test pattern is generated in such a way that SA1 and SA0 are set for each node and that, when they are fixed to the observable logic level of 0 or 1, a functional failure results.

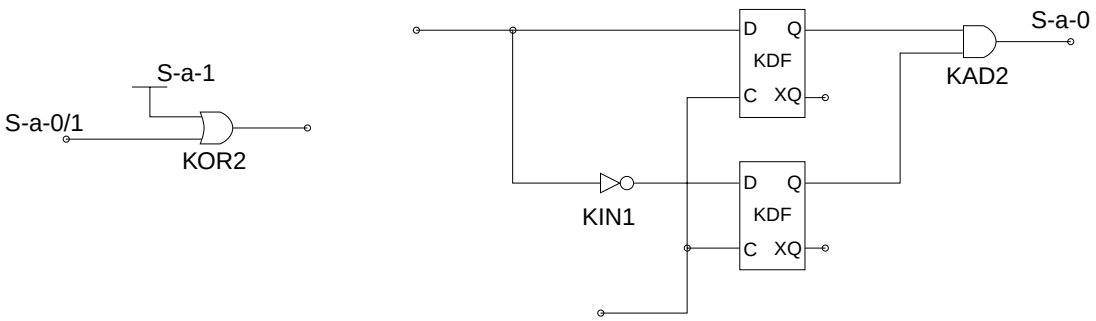


Figure 2-7 Example of an Untestable Fault

(4) Design flow (1/2)

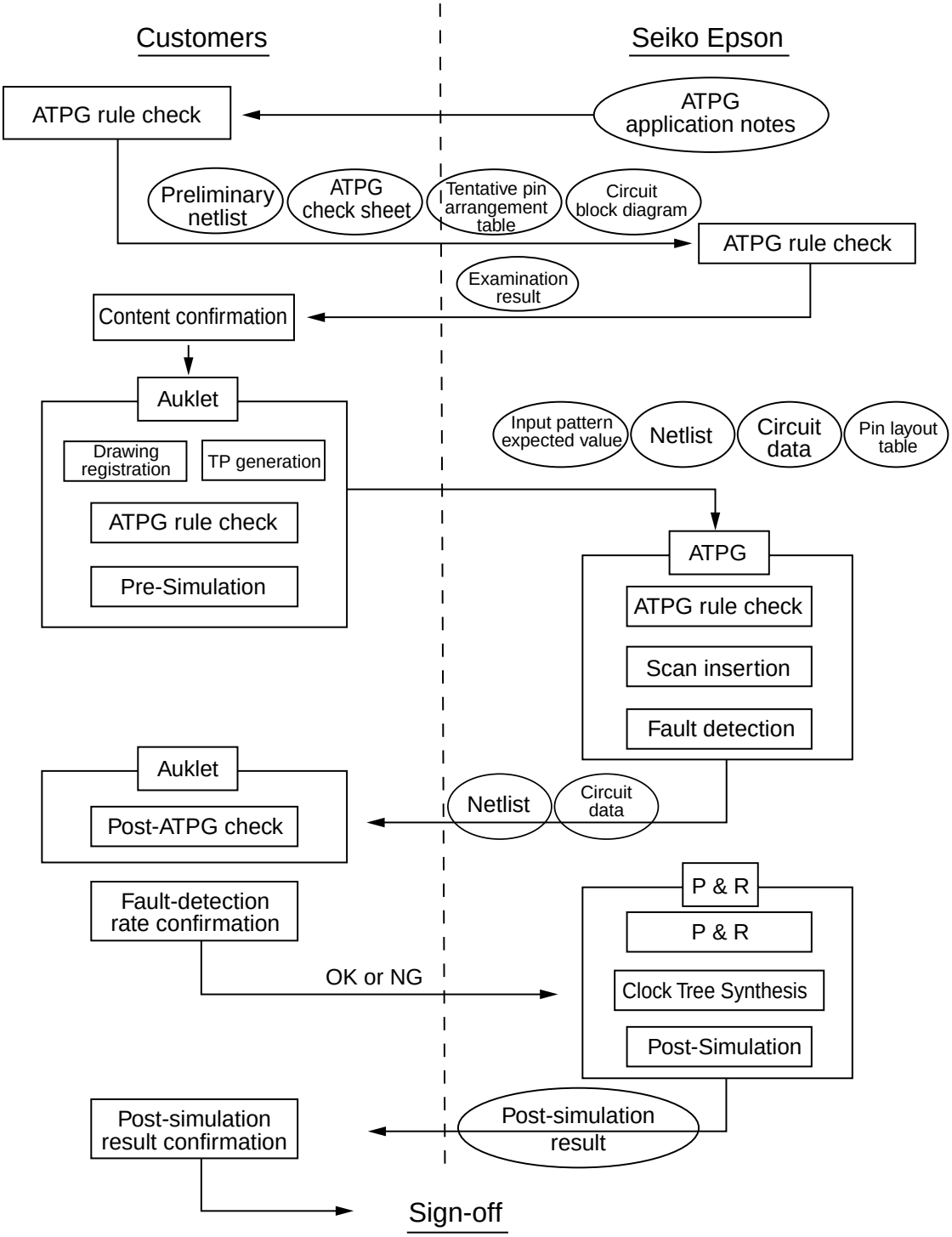


Figure 2-8 ATPG Flow for Development by Auklet

(4) Design flow (2/2)

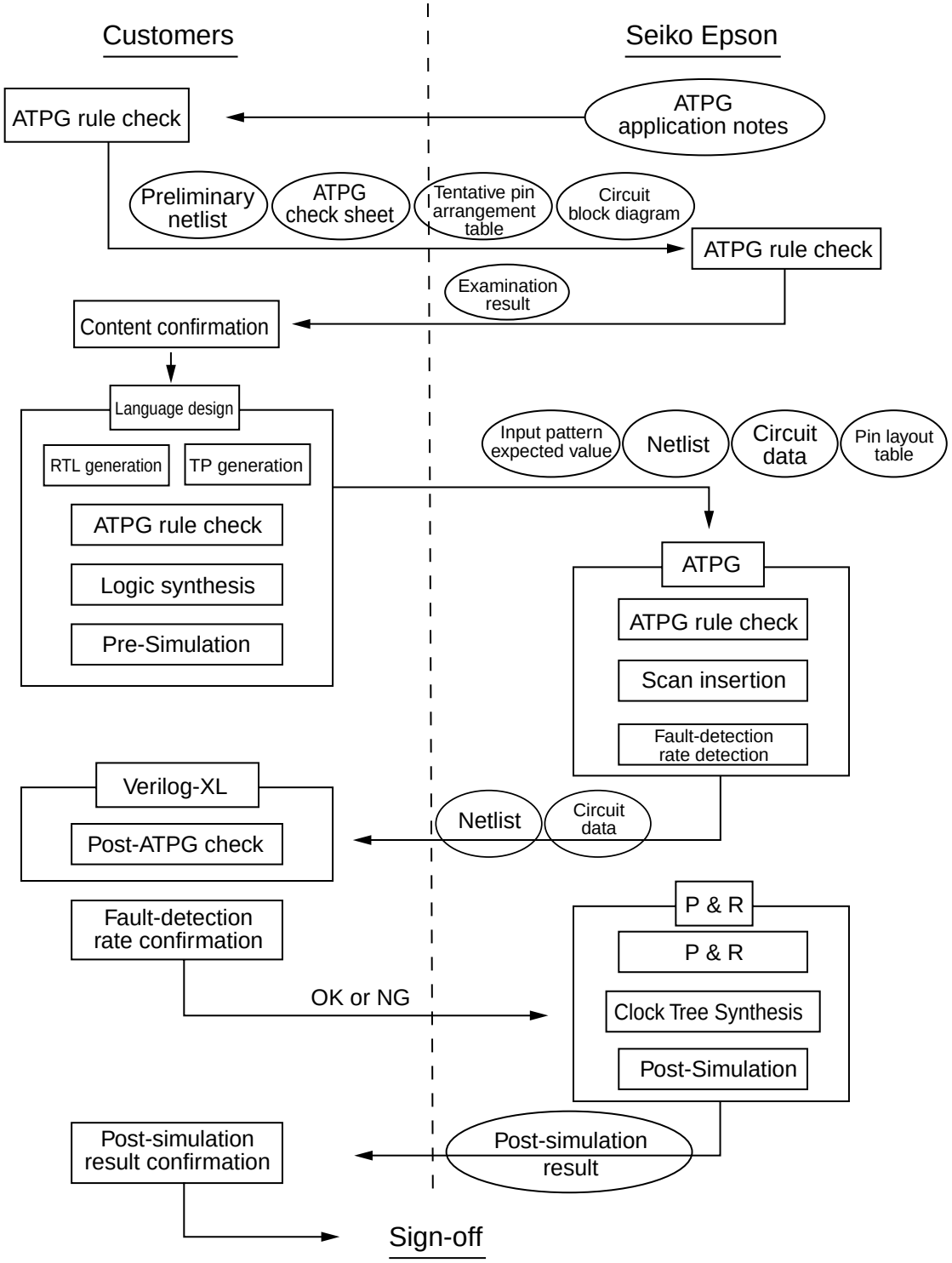


Figure 2-9 ATPG Flow for Development by Logic Synthesis

(5) Configuration of test patterns generated by ATPG

The test patterns generated by ATPG have the two modes specified below, and these two modes must be switched over using a scan enable input pin (SCANEN). Because the SCANEN pin is connected for circuit scanning, make sure your circuits have this pin prepared as a dedicated input pin.

- Scan shift mode

  In this mode, data is input and output to and from the circuit's internal storage device (flip-flop) configured as a shift register.

- Scan test mode

  In this mode, the data applied to the storage device in scan shift mode is operated internally through the entry of a clock.

(6) Input/output pins for ATPG

The pins needed for ATPG are described below. Of these, the provision of two pins, SCANEN and ATPGEN, is sufficient for ATPG to be run efficiently. This may result in a reduced delivery period and an increased fault detection rate, however.

- Scan enable input pin (SCANEN)

  This pin is used to switch between scan-shift and scan-test modes. It also is used to reset or set the flip-flop, and to fix the bidirectional input/output select signal during scan shift. Because this pin is always necessary for scanning, be sure to prepare it as a dedicated input pin.

- ATPG test input pin (ATPGEN)

  This pin makes the circuit suitable for ATPG, and is used to fix the circuit's internal asynchronous parts or for switchover to make clock lines controllable that cannot be controlled from the outside. This pin is unnecessary if the ATPG rules were taken into consideration in the design of the original circuit. Prepare this pin as a dedicated input pin.

- Scan data input pin

  This input pin is used to set data in the shift register generated by scanning. Two or more of these pins may exist, depending on the number of scan flip-flops, and this pin may be shared with other pins. However, it cannot be shared with the control pins that reset/set the clock, nor can it be shared with other pins employed for scanning. If it is shared with bidirectional pins, make sure the pin is always in input state through the use of the ATPGEN pin, for example.

- Scan data output pin

  This pin is used to read data from the shift register generated by scanning. Two or more of these pins may exist, depending on the number of scan flip-flops, and this pin may be shared with other pins. However, if it is shared with bidirectional pins, make sure the pin is always in output state through the use of the ATPGEN pin, for example.

- Scan clock input pin

  This clock input pin is in the test pattern generated by ATPG. In most cases, this pin uses the system clock during normal operation.

(7) Logic circuit design rules for ATPG support (DFT)

In order for ATPG to be performed, the logic circuit is scanned. In the creation of the original circuit, be sure to follow the rules specified below to ensure that it will have good observability. Practical examples are shown below. If these measures are difficult to implement or there are any uncertainties about them, contact Seiko Epson.

- Applicable series: S1L50000, S1L30000, S1L9000F, S1X50000, S1K50000
- Prepare one scan enable input pin (SCANEN) as a dedicated input pin.
- Submit “trial data” to Seiko Epson one week prior to the release of the formal data. This trial data is necessary to preliminarily check your circuit prior to formal data-in, in order to increase the efficiency of work following formal data-in and achieve a high fault detection rate.
- The clock, reset, and set inputs of all flip-flops to be scanned must be controllable directly from the external pins.

  → If not controllable, configure a controllable circuit by attaching an ATPG test input pin (ATPGEN) separately from the SCANEN pin.

  → If the flip-flops are configured to have multiple clocks fed from external pins, make sure all of the flip-flops to be scanned basically operate with a single clock input when ATPGEN is active. However, if two or more of such circuit configurations exist, consult Seiko Epson.

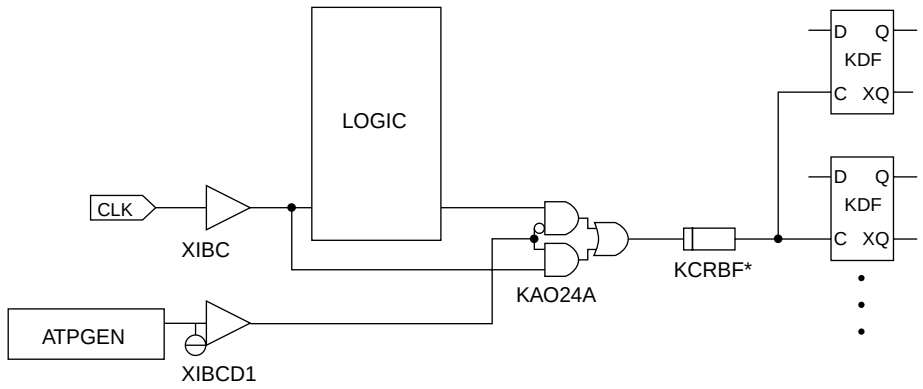


Figure 2-10 Example of Processing of the Clock Line

- Circuit design using scan flip-flops in the original circuit is inhibited.
- Skew consideration for clock nets by Clock Tree Synthesis must be supported.
- I/O cells must be placed on the top hierarchical level.

- Do not use internal tri-state buses.

  → Correct the circuit to configure internal tri-state buses with multiplexers or the like. If it is unavoidable to use internal tri-state buses, use the ATPGEN pin to ensure that those bus circuits will not contend for bus control. However, because this measure is detrimental to increasing the fault detection rate, do not use such a circuit configuration if a high fault detection rate is desired.

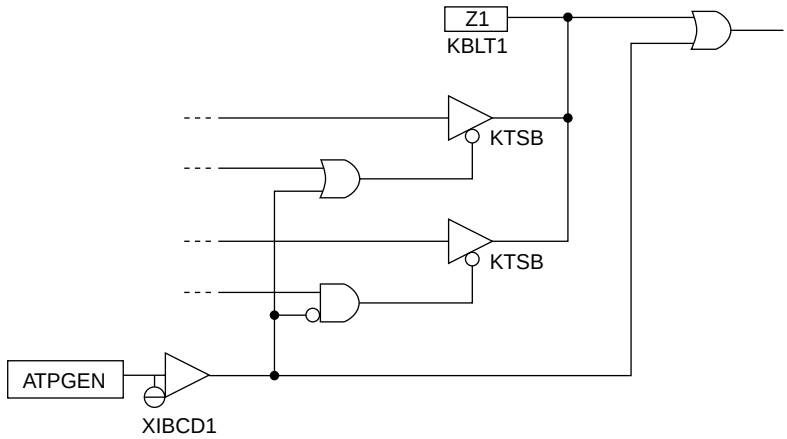


Figure 2-11 Example of the Processing of Internal Tri-State Buses

- When using macro cells such as RAM, ROM, or megacells, include the flip-flops to be scanned in your circuit configuration before and after the input/output ports of those macro cells.

  → Without such a circuit configuration, fault detection before and after the macro cells may not be guaranteed.

- Avoid the use of MSI macros that include flip-flops (e.g., KT175 or KA161).

  → MSI cells are not scanned. If a high fault detection rate is desired, do not use MSI cells.

- The use of circuits that tend to cause racing, such as RS latches and differentiating circuits, as well as the use of asynchronous circuits, are inhibited.

  → When using such circuits, be sure to fix the circuit outputs with the ATPGEN pin. However, because this measure is detrimental to increasing the fault detection rate, do not use these circuits if a high fault detection rate is desired.

- Fix the latch cells with the ATPGEN pin to ensure that they will always be in a through state.

  → Because this measure is detrimental to increasing the fault detection rate, avoid using latch cells whenever possible if a high fault detection rate is desired.

- Make sure the bidirectional pins are set for input during scan shift mode.

  → If it is unavoidable for the bidirectional pins to be assigned for scan data input or scan data output, fix the pins for input or output, respectively.

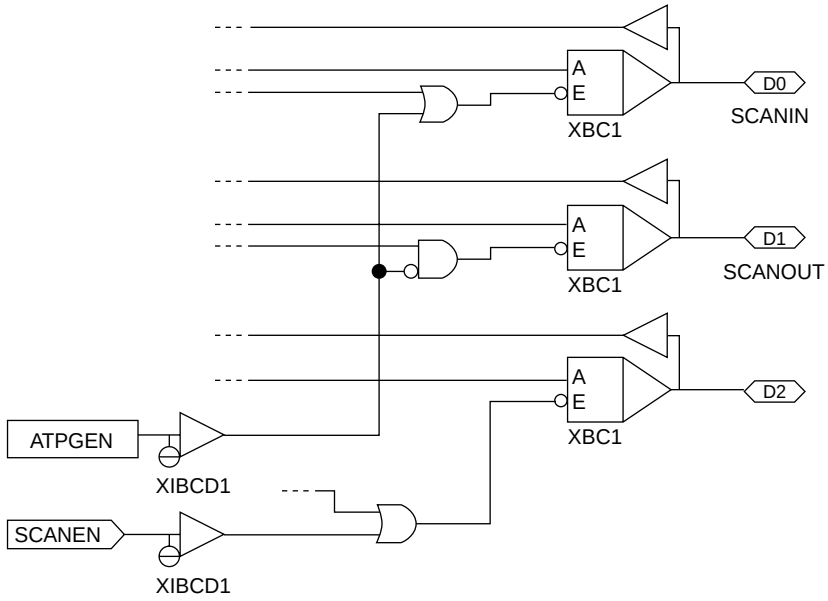


Figure 2-12 Example of the Processing of Bidirectional Pins

- Fix the outputs of non-scanned flip-flops.

  → The outputs of MSI macros that include T-flip-flops or flip-flops, as well as those of non-scanned flip-flops, cause malfunction in the ATPG test pattern or hinder fault detection. Therefore, fix their outputs using the ATPGEN pin as much a as possible.

(8) Other

- Depending on the number of scanned flip-flops, the number of gates increases by approximately 15% to 20% compared to that in the original circuit.
- The period required for DFT and ATPG depends on the circuit configuration and gate size. The DFT and ATPG work at Seiko Epson requires at least three days, which should be taken into account in your plan. (In some cases, depending on the circuit configuration, approximately 10 days may be required. Therefore, please carefully examine the presented materials when designing your circuit.)
- Prior to data-in, please send the "ATPG check sheet" and "external pin information" to Seiko Epson. If circuit changes are required, you will be requested to make them. The test pattern interfaced to Seiko Epson should include definitions of the external pins (e.g., ATPGEN and SCANEN) for scan purposes.
  For ATPG support, CTS (Clock Tree Synthesis) is essential during placement and routing. Therefore, please submit the necessary information for Clock Tree Synthesis specified on page 15, along with said information.

(9) ATPG check sheet

Please be sure to submit this sheet one week prior to data-in. Encircle the appropriate answer for each question.

1.	Interface netlist format for Seiko Epson (gate level)	Verilog or EDIF
2.	Are scan flip-flops used in the original circuit? (Note 1)	Yes or No
3.	Is any macro cell, MSI cell, or intermittently oscillating cell used?	Yes or No
4.	If Yes, enter the cell name:_____	
5.	Is any internal tri-state bus used?	Yes or No
6.	Does any RS latch, differentiating circuit, or asynchronous circuit exist?	Yes or No
7.	Are latch cells used?	Yes or No
8.	Are bidirectional pins included?	Yes or No
9.	Is there any clock that cannot be controlled directly from the outside?	Yes or No
10.	Are there any reset/set pins for flip-flops or latch cells that cannot be controlled directly from the outside?	Yes or No
11.	If you answered Yes to any of questions 3 through 10 above, is your circuit designed in conformity with the DFT rules? (Note 2)	Yes or No
12.	Are I/O cells placed at the top level?	Yes or No
13.	Are measures taken to correct the skew problems of clock nets by Clock Tree Synthesis?	Yes or No

Note 1: If Yes, please correct your circuit, as the circuit cannot be scanned.

Note 2: If No, please insert DFT, as the circuit cannot be scanned. In addition, if you would like to request DFT insertion by Seiko Epson because detailed circuit information is required in addition to this sheet, contact Seiko Epson.

- **External pin information**

Enter the names of pins that match those in the pin arrangement table. The necessary pins vary with the circuit configuration. (Always be sure to specify the necessary pins.)

- Clock input pins

Pin name:_____ Active edge: rise • fall

Pin name:_____ Active edge: rise • fall

Pin name:_____ Active edge: rise • fall

Pin name:_____ Active edge: rise • fall

Pin name:_____ Active edge: rise • fall

- Scan enable input pin (Note 3) ..... Included • Not included

Pin name:_____ Active level: High • Low

- ATPG test input pin ..... Included • Not included

Pin name:_____ Active level: High • Low

- Clear/preset input pin..... Included • Not included

Pin name:_____ Active level: High • Low

- Other ATPG mode control pins ..... Included • Not included

a. Pin name:_____

Content of control, active level, etc.

: _____

b. Pin name:_____

Content of control, active level, etc.

: _____

c. Pin name:_____

Content of control, active level, etc.

: _____

d. Pin name:_____

Content of control, active level, etc.

: _____

• Input pins that cannot be assigned for scan data input (Note 4)

_____

_____

• Output pins that cannot be assigned for scan data output (Note 4)

_____

_____

• Remarks

_____

_____

_____

_____

_____

_____

_____

_____

<Other>

- Number of gates (BC) prior to scan cell insertion : _____
- Total number of D and JK flip-flops : _____
- Expected date of trial data presentation: (_____Month, _____day, _____year)

  (Trial data: Check sheet, preliminary netlist, tentative pin arrangement table, circuit block diagram)
- Desired fault detection rate : ____ %
- Along with this sheet, materials that will help to confirm circuit blocks, hierarchical levels (module and instance names), and data paths between clock lines and blocks are requested.

Note 3: If not inserted in the original circuit, please specify your desired contents.

Note 4: Unless a specific request to the contrary is made, pins will be assigned by Seiko Epson.

2.11 Limitations and Restrictions on VHDL and Verilog-HDL Netlists

The VHDL and Verilog-HDL netlists to be interfaced to Seiko Epson must be in the form of pure gate-level netlists (not including an operational description). The following specifies the limitations and restrictions to which the development of Seiko Epson ASICs by VHDL or Verilog-HDL is subject.

2.11.1 Common

(1) External pin names (I/O pins)
- To be written entirely in uppercase letters.
- Number of charactersLimited to between 2 and 32 characters.
- Usable characters Only alphanumeric characters and underscore '_' can be used. The string must always begin with a letter, however.
- Examples of unusable characters and strings:

  2INPUT: The string begins with a number.

  \2INPUT: The string is prefixed by a backslash '\'.

  InputA: The string includes lowercase letters.

  INPUTA: The string begins with an underscore ''.

  INA[3:0]: A bus is used for an external pin name.

  INA[3]: A bus is used for an external pin name.

(2) Internal pin names (including a bus' net names)
- Although a combination of uppercase and lowercase letters is permitted, the use specified below is prohibited.
  Example: Mixed use of _RESET_ and _Reset_, etc.
- Number of characters: Limited to between 2 and 32 characters
- Usable characters: Only alphanumeric characters, underscore '_', _[]_ (Verilog bus bracket), and _()_ (VHDL bus bracket) can be used. The string must always begin with a letter, however.

(3) Bus description at the top of modules is prohibited.
Example: DATA[3:0], DATA[3], DATA[2], and the like are prohibited. DATA0, DATA1, DATA2, and the like are all permitted.

(4) Input/output cells must use the same library series. No cells can be used in a combination of different series.

(5) Operational descriptions using behavior or C language are not permitted. Such descriptions in netlists have no effect.

(6) All time scales in each library series are expressed to an accuracy of 1 ps.

2.11.2 Limitations and Restrictions on Verilog-HDL Netlists

(7) Descriptions using assign and tran in gate-level Verilog netlists are prohibited.

(8) For connecting descriptions in Verilog netlists, connections using the pin names of cells are recommended.
Examples: Pin-name connection: IN2 inst_1 (.A(inst_2),.X(inst_3)); recommended
Net-name connection: IN2 inst_1 (net1,net2);

(9) Verilog commands such as force cannot be used in the operational description of flip-flops.
(Example: logic.signal = 0;)

(10) A time-scale description must be added at the beginning of gate-level netlists generated by a Synopsys design compiler. This time scale must have the same value as that specified in the Seiko Epson Verilog library. For the time scales in each series, see (6).
Example: `timescale 1 ps / 1 ps

(11) Seiko Epson prohibited the mixed use of a bus' single port and the name escaped by attaching __ to that port within the same module, as follows:
input A[0];
wire \A[0] ;

(12) The strings listed below are Verilog's reserved words. Use of these strings as user-defined names is prohibited.
always, and, assign, begin, buf, bufif0, bufif1, case, design,default, defparam, disable, else, end, endcase, endfunction, endmodule, endtask, event, for, force, forever, fork, function, highz0, highz1, if, initial, inout, input, integer, join, large, medium, module, nand, negedge, nor, not, notif0, notif1, or, output, parameter, posedge, pull0, pull1, reg, release, repeat, scalared, small, specify, strong0, strong1, supply0, supply1, task, time, tri, tri0, tri1, trinand, trior, trireg, vectored, wait, wand, weak0, weak1, while, wire, wor, xor, xnor

2.11.3 Limitations and Restrictions on VHDL Netlists

(13) In addition to the restrictions specified in (1), use of the following strings is also prohibited.

INPUTA_ : The string ends with an underscore '_'.

INPUT_ _A : The string has two consecutive underscores.

read : Used by the system

write : Used by the system

(14) The strings listed below are VHDL's reserved words. Use of these strings as user-defined names is prohibited.
abs, access, after, alias, all, and, architecture, array, assert, attribute, begin, block, body, buffer, bus, case, component, configuration, constant, disconnect, downto, else, elsif, end, entity, exit, file, for, function, generate, generic, guarded, if, in, inout, is, label, library, linkage, loop, map, mod, nand, new, next, nor, not, null, of, on, open, or, others, out, package, port, procedure, process, range, record, register, rem, report, return, select, severity, signal, subtype, then, to, transport, type, units, until, use, variable, wait, when, while, with, xor

(15) Before the Seiko Epson tools and utilities can be used, the VHDL format must be converted into Verilog format. For this reason, the Verilog reserved words specified in (12) also cannot be used in VHDL.

Chapter 3 Types of Input/Output Buffers and Usage Precautions

3.1 Types of Input/Output Buffers

The S1K50000 series is available for many and varied types of cells, which can be chosen depending on the input interface level, the presence of Schmitt trigger inputs or pull-up/pull-down resistors, the output drive capability, and the noise protection measures used. In accordance with the descriptions below, choose the input/output buffers best suited for your circuit. There are two methods for using the input/output buffers, one for single power supplies (3.3 V or 2.0 V) and one for dual power supplies (5.0 V and 3.3 V, or 3.3 V and 2.0 V).

3.1.1 Selecting Input/Output Buffers

(1) Selecting input buffers

a) Whether the required interface level is the CMOS or TTL level
b) Whether a Schmitt trigger input is needed (need for hysteresis characteristics)
c) Whether internal pull-up/pull-down resistors are required

(2) Selecting output buffers

a) The magnitude of the required output drive current (ILO and IOH)
b) Whether a noise protection measure is required
c) Whether a bus hold circuit is required

(3) Selecting bidirectional buffers

Refer to paragraphs (1) and (2) in the selection of bidirectional buffers.

• Input/output interface level

1) For dual 5.0-V power supplies

Input level
TTL level, CMOS level, TTL Schmitt, CMOS Schmitt, PCI*

Output level
CMOS level, PCI*

2) For single power supplies and dual 3.3-V power supplies

Input level
LVTTL level, LVTTL Schmitt, PCI*

Output level
LVTTL level, PCI*

3) For single power supplies and dual 2.0-V power supplies

Input level
CMOS level, TTL Schmitt

Output level
CMOS level

Note: For single power supplies (3.3 V or 2.0 V), TTL-level inputs cannot be used.
* For details on the PCI interface, contact Seiko Epson or its distributor.

- **Output drive capability**

  See Electrical Characteristics (Tables 1-5 through 1-7).

- **Pull-up/pull-down resistors**

  See Electrical Characteristics (Tables 1-5 through 1-7).

Beginning with the following Section 3.2, “Input/Output Buffer Configuration with a Single Power Supply,” we will describe in detail the procedure for configuring the input and output buffers or bidirectional buffers with a single power supply. For details on the procedure for configuring the input and output buffers with dual power supplies, see Chapter 9, “Precautions on the Use of Dual Power Supplies.”

3.2 Input/Output-Buffer Configuration with a Single Power Supply

When input/output buffers with a single power supply are used, the power-supply voltage is either 3.3 V or 2.0 V (input/output buffers cannot be used at 5.0 V).

3.2.1 Input/Output-Buffer Configuration with a Single Power Supply

3.2.1.1 Input-Buffer Configuration with a Single Power Supply

Table 3-1-1 Input Buffers

(V_{DD} = 3.3 V)

Cell Name	Input Level	Function	With or without pull-up/pull-down resistors
XIBC	LVTTL	Buffer	Without
XIBCP*	LVTTL	Buffer	Pull-up resistor (50 kΩ, 100 kΩ)
XIBCD*	LVTTL	Buffer	Pull-down resistor (50 kΩ, 100 kΩ)
XIBH	LVTTL Schmitt	Buffer	Without
XIBHP*	LVTTL Schmitt	Buffer	Pull-up resistor (50 kΩ, 100 kΩ)
XIBHD*	LVTTL Schmitt	Buffer	Pull-down resistor (50 kΩ, 100 kΩ)
XIBPB	PCI-3V	Buffer	Without
XIBPBP*	PCI-3V	Buffer	Pull-up resistor (50 kΩ, 100 kΩ)
XIBPBD*	PCI-3V	Buffer	Pull-down resistor (50 kΩ, 100 kΩ)

Note: When * value is 1 or 2, the pull-up/pull-down resistance values correspond to 1:50 kΩ, 2:100 kΩ respectively.

Table 3-1-2 Input Buffers

(V_{DD} = 2.0 V)

Cell Name	Input Level	Function	With or without pull-up/pull-down resistors
XIBC	CMOS	Buffer	Without
XIBCP*	CMOS	Buffer	Pull-up resistor (120 kΩ, 240 kΩ)
XIBCD*	CMOS	Buffer	Pull-down resistor (120 kΩ, 240 kΩ)
XIBH	CMOS Schmitt	Buffer	Without
XIBHP*	CMOS Schmitt	Buffer	Pull-up resistor (120 kΩ, 240 kΩ)
XIBHD*	CMOS Schmitt	Buffer	Pull-down resistor (120 kΩ, 240 kΩ)

Note: When * value is 1 or 2, the pull-up/pull-down resistance values correspond to 1:120 kΩ, 2:240 kΩ respectively.

3.2.1.2 Output-Buffer Configuration with a Single Power Supply

Tables 3-2-1 and 3-2-2 list the S1K50000-series output buffers.

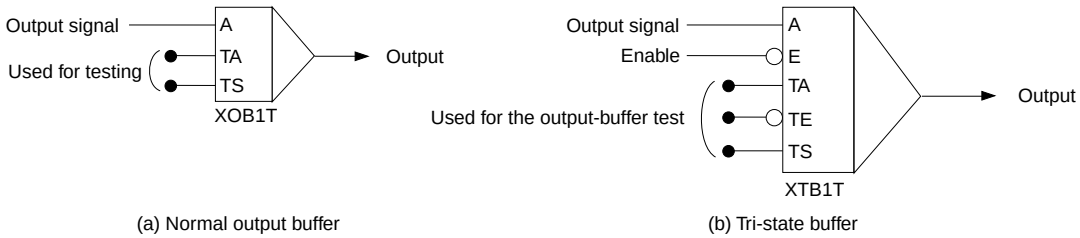


Figure 3-1 Example of an Output-Buffer Symbol

Table 3-2-1 Output Buffers

(V_{DD} = 3.3 V)

Function	I_{OL}* / I_{OH}**	Cell Name***
Normal output	0.1 mA / -0.1 mA 1 mA / -1 mA 2 mA / -2 mA 6 mA / -6 mA 12 mA / -12 mA	XOBST XOBMT XOB1T XOB2T XOB3T
Output for PCI	PCI-3V	XOBPBT
Normal output for high speed	2 mA / -2 mA 6 mA / -6 mA 12 mA / -12 mA	XOB1CT XOB2CT XOB3AT
Normal output for low noise	12 mA / -12 mA	XOB3BT
3-state output	0.1 mA / -0.1 mA 1 mA / -1 mA 2 mA / -2 mA 6 mA / -6 mA 12 mA / -12 mA	XTBST XTBMT XTB1T XTB2T XTB3T
3-state output for PCI	PCI-3V	XTBPBT
3-state output for high speed	2 mA / -2 mA 6 mA / -6 mA 12 mA / -12 mA	XTB1CT XTB2CT XTB3AT
3-state output for low noise	12 mA / -12 mA	XTB3BT
3-state output (Bus hold circuit)	1 mA / -1 mA 2 mA / -2 mA 6 mA / -6 mA 12 mA / -12 mA	XTBMHT XTB1HT XTB2HT XTB3HT
3-state output for high speed (Bus hold circuit)	2 mA / -2 mA 6 mA / -6 mA 12 mA / -12 mA	XTB1CHT XTB2CHT XTB3AHT
3-state output for low noise (Bus hold circuit)	12 mA / -12 mA	XTB3BHT

Notes: * V_{OL} = 0.4 (V_{DD} = 3.3 V)

** V_{OH} = V_{DD} - 0.4 V (V_{DD} = 3.3 V)

*** In addition to the output buffers specified in Table 3-2-1, a configuration without test pins may be considered. If such a configuration is desired, contact Seiko Epson or its distributor.

Table 3-2-2 Output Buffers

(V_{DD} = 2.0 V)

Function	I_{OL}* / I_{OH}**	Cell Name***
Normal output	0.05 mA / -0.05 mA 0.3 mA / -0.3 mA 0.6 mA / -0.6 mA 2 mA / -2 mA 4 mA / -4 mA	XOBST XOBMT XOB1T XOB2T XOB3T
Normal output for high speed	0.6 mA / -0.6 mA 2 mA / -2 mA 4 mA / -4 mA	XOB1CT XOB2CT XOB3AT
Normal output for low noise	4 mA / -4 mA	XOB3BT
3-state output	0.05 mA / -0.05 mA 0.3 mA / -0.3 mA 0.6 mA / -0.6 mA 2 mA / -2 mA 4 mA / -4 mA	XTBST XTBMT XTB1T XTB2T XTB3T
3-state output for high speed	0.6 mA / -0.6 mA 2 mA / -2 mA 4 mA / -4 mA	XTB1CT XTB2CT XTB3AT
3-state output for low noise	4 mA / -4mA	XTB3BT
3-state output (Bus hold circuit)	0.3 mA / -0.3 mA 0.6 mA / -0.6 mA 2 mA / -2 mA 4 mA / -4 mA	XTBMHT XTB1HT XTB2HT XTB3HT
3-state output for high speed (Bus hold circuit)	0.6 mA / -0.6 mA 2 mA / -2 mA 4 mA / -4 mA	XTB1CHT XTB2CHT XTB3AHT
3-state output for low noise (Bus hold circuit)	4 mA / -4 mA	XTB3BHT

Notes: * V_{OL} = 0.2 (V_{DD} = 2.0 V)

** V_{OH} = V_{DD} - 0.2 V (V_{DD} = 2.0 V)

*** In addition to the output buffers specified in Table 3-2-2, a configuration without test pins may be considered. If such a configuration is desired, contact Seiko Epson or its distributor.

3.2.1.3 Bidirectional-Buffer Configuration with a Single Power Supply

Tables 3-3-1 and 3-3-2 list the S1K50000-series bidirectional buffers.

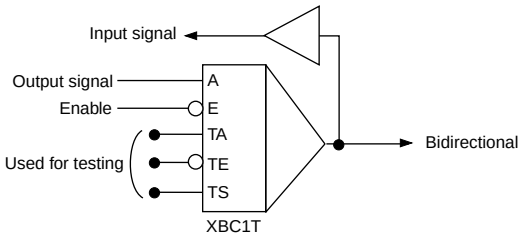


Figure 3-2 Example of a Bidirectional-Buffer Symbol

Table 3-3-1 Bidirectional Buffers

(V_{DD} = 3.3 V)

Input Level	Function	I_{OL}* / I_{OH}**	Cell Name***
LVTTL	Bi-directional output	0.1 mA / -0.1 mA 1 mA / -1 mA 2 mA / -2 mA 6 mA / -6 mA 12 mA / -12 mA	XBCST XBCMT XBC1T XBC2T XBC3T
	Bi-directional output for high speed	2 mA / -2 mA 6 mA / -6 mA 12 mA / -12 mA	XBC1CT XBC2CT XBC3AT
	Bi-directional output for low noise	12 mA / -12 mA	XBC3BT
PCI-3V	Bi-directional output for PCI	PCI-3V	XBPBT
LVTTL Schmitt	Bi-directional output	0.1 mA / -0.1 mA 1 mA / -1 mA 2 mA / -2 mA 6 mA / -6 mA 12 mA / -12 mA	XBHST XBHMT XBH1T XBH2T XBH3T
	Bi-directional output for high speed	2 mA / -2 mA 6 mA / -6 mA 12 mA / -12 mA	XBH1CT XBH2CT XBH3AT
	Bi-directional output for low noise	12 mA / -12 mA	XBH3BT
LVTTL	Bi-directional output (Bus hold circuit)	1 mA / -1 mA 2 mA / -2 mA 6 mA / -6 mA 12 mA / -12 mA	XBCMHT XBC1HT XBC2HT XBC3HT
	Bi-directional output for high speed (Bus hold circuit)	2 mA / -2 mA 6 mA / -6 mA 12 mA / -12 mA	XBC1CHT XBC2CHT XBC3AHT
	Bi-directional output for low noise (Bus hold circuit)	12 mA / -12 mA	XBC3BHT
LVTTL Schmitt	Bi-directional output (Bus hold circuit)	1 mA / -1 mA 2 mA / -2 mA 6 mA / -6 mA 12 mA / -12 mA	XBHMHT XBH1HT XBH2HT XBH3HT
	Bi-directional output for high speed (Bus hold circuit)	2 mA / -2 mA 6 mA / -6 mA 12 mA / -12 mA	XBH1CHT XBH2CHT XBH3AHT
	Bi-directional output for low noise (Bus hold circuit)	12 mA / -12 mA	XBH3BHT

Notes: * V_{OL} = 0.4 (V_{DD} = 3.3 V)

** V_{OH} = V_{DD} - 0.4 V (V_{DD} = 3.3 V)

*** In addition to the bidirectional buffers specified in Table 3-3-1, a configuration with pull-up/pull-down resistors or without test pins may be considered. If such a configuration is desired, contact Seiko Epson or its distributor.

Table 3-3-2 Bidirectional Buffers

(V_{DD} = 2.0 V)

Input Level	Function	I_{OL}* / I_{OH}**	Cell Name***
CMOS	Bi-directional output	0.05 mA / -0.05 mA 0.3 mA / -0.3 mA 0.6 mA / -0.6 mA 2 mA / -2 mA 4 mA / -4 mA	XBCST XBCMT XBC1T XBC2T XBC3T
	Bi-directional output for high speed	0.6 mA / -0.6 mA 2 mA / -2 mA 4 mA / -4 mA	XBC1CT XBC2CT XBC3AT
	Bi-directional output for low noise	4 mA / -4 mA	XBC3BT
CMOS Schmitt	Bi-directional output	0.05 mA / -0.05 mA 0.3 mA / -0.3 mA 0.6 mA / -0.6 mA 2 mA / -2 mA 4 mA / -4 mA	XBHST XBHMT XBH1T XBH2T XBH3T
	Bi-directional output for high speed	0.6 mA / -0.6 mA 2 mA / -2 mA 4 mA / -4 mA	XBH1CT XBH2CT XBH3AT
	Bi-directional output for low noise	4 mA / -4 mA	XBH3BT
CMOS	Bi-directional output (Bus hold circuit)	0.3 mA / -0.3 mA 0.6 mA / -0.6 mA 2 mA / -2 mA 4 mA / -4 mA	XBCMHT XBC1HT XBC2HT XBC3HT
	Bi-directional output for high speed (Bus hold circuit)	0.6 mA / -0.6 mA 2 mA / -2 mA 4 mA / -4 mA	XBC1CHT XBC2CHT XBC3AHT
	Bi-directional output for low noise (Bus hold circuit)	4 mA / -4 mA	XBC3BHT
CMOS Schmitt	Bi-directional output (Bus hold circuit)	0.3 mA / -0.3 mA 0.6 mA / -0.6 mA 2 mA / -2 mA 4 mA / -4 mA	XBHMHT XBH1HT XBH2HT XBH3HT
	Bi-directional output for high speed (Bus hold circuit)	0.6 mA / -0.6 mA 2 mA / -2 mA 4 mA / -4 mA	XBH1CHT XBH2CHT XBH3AHT
	Bi-directional output for low noise (Bus hold circuit)	4 mA / -4 mA	XBH3BHT

Notes: * V_{OL} = 0.2 (V_{DD} = 2.0 V)

** V_{OH} = V_{DD} - 0.2 V (V_{DD} = 2.0 V)

*** In addition to the bidirectional buffers specified in Table 3-3-2, a configuration with pull-up/pull-down resistors or without test pins may be considered. If such a configuration is desired, contact Seiko Epson or its distributor.

3.2.2 Fail-Safe Cells

(1) Outline

Seiko Epson's S1K50000 series of Fail-Safe cells allows signals operating at levels higher than the power-supply voltage in a single-power-supply design to be interfaced without the installation of a dedicated interfacing power supply. Therefore, it is not necessary for customers to install the operating power supply or an interfacing power supply in the LSI, as is conventionally required. In addition, signals operating at levels equal to the power-supply voltage can also be interfaced without modifying the circuit. This provides customers with greater freedom in circuit design.

(2) Features

- With no limitations on the number of cells used or their placement, the Fail-Safe cells can be placed as desired by customers, providing freedom in circuit design.
- In a single-power-supply design, signals operating at levels higher than the power-supply voltage can be interfaced from the outside without the installation of a dedicated interfacing power supply equal to or greater than the power-supply voltage.
- The supported input levels are the LVTTL and LVTTL Schmitt levels (when V_{DD} = 3.3 V), as well as the CMOS and CMOS Schmitt levels (when V_{DD} = 2.0 V).
- Because the Fail-Safe cells are entirely of a CMOS structure, they help to reduce the chip's power consumption.

(3) Usage precautions

- The Fail-Safe cells cannot determine Seiko Epson's standard input level for reasons of circuit configuration. Therefore, if it is necessary for the input level to be determined by a tester, a test circuit must be configured separately. In such a case, refer to the example of a test circuit on page 54 (Figure 3-6) in the creation of a test circuit.
- The Fail-Safe cells are characterized in that when the output pins are in High-Z state, i.e., in input mode, no DC current will flow into the LSI even when signals exceeding the power-supply voltage are fed into the pins. However, if signals equal to or greater than the power-supply voltage are fed into the pins when the cell is in output mode and outputting a high-level signal, DC current will flow into the LSI as with a conventional Fail-Safe cell. This occurs in a situation in which, while the Fail-Safe cell is outputting a high-level (3.3 V) signal, another device is also outputting a high-level (5.0 V) signal at the same time. Note that the other device referred to here includes a pull-up resistor.
- Although signals with a voltage level equal to or greater than the LSI's operating voltage can be accepted, in no case can the signal voltages applied to the Fail-Safe cell exceed the Absolute Maximum Rated Voltage.

(4) List of Fail-Safe cells

- **Fail-Safe input buffers**

  This is an input cell with the protective diode on the V_{DD} side eliminated. This input buffer is used in cases in which, in a single power-supply system, high-voltage signals above V_{DD} are entered (for example, 5-V signals when V_{DD} = 3.3 V, or 3.3-V signals when V_{DD} = 2.0 V). The input level of this buffer when V_{DD} = 2.0 V is the CMOS level.

Table 3-4-1 Fail-Safe Input Buffers

(V_{DD} = 3.3 V)

Input Level	Without Resistor	Pull-down*		Pull-up*	
		50 kΩ	100 kΩ	50 kΩ	100 kΩ
LVTTL	XIDC	XIDCD1	XIDCD2	XIBBP1	XIBBP2
LVTTL Schmitt	XIDH	XIDHD1	XIDHD2	—	—

Note: The indicated resistance values apply to the case where V_{DD} = 3.3 V.

- **Fail-Safe output buffers**

  1) N-channel open-drain type
     This output buffer is used in cases in which, in a 3-V single-power-supply system, 5.0-V signals are output. With the P-channel removed, this type of buffer can only output a low-level signal but, by tying the pull-up resistors external to the standard cell to 5 V, it can send 5-V signals to external 5-V devices.

  2) Tri-state type
     In ordinary tri-state output buffers, if a 5-V system voltage propagates while their outputs are disabled (Hi-Z state), DC current flows into the internal part of the ASIC chip. The Fail-Safe cell, however, is constructed so as to prevent such a current from flowing in. Furthermore, it can output a 3-V-system full-swing signal. Unlike the N-channel open-drain type, however, this type of Fail-Safe cell cannot have its output pulled high to 5 V through the addition of a pull-up resistor external to the standard cell.

Table 3-4-2 Fail-Safe Output Buffers

(V_{DD} = 3.3 V)

Function	I_{OL}*	Cell Name	
		N-channel open-drain**	Tri-state
Normal Output	2 mA	XOD1T	XTBF1
	6 mA	XOD2T	XTBF2
	12 mA	XOD3T	—
HIGH SPEED Output	2 mA	XOD1CT	XTBF1C
	6 mA	XOD2CT	XTBF2C
	12 mA	—	XTBF3A

Notes: * V_{OL} = 0.4 V (V_{DD} = 3.3 V)

** In addition to those specified in Table 3-4-2, cells without test pins are also available. If such cells are desired, contact Seiko Epson or its distributor.

- **Fail-Safe bidirectional buffers**

  1) N-channel open-drain type

Table 3-4-3 N-channel Open-Drain Bidirectional Buffers

(V_{DD} = 3.3 V)

Input Level	Function	I_{OL}*	Cell Name**
LVTTL	Bi-directional output	2 mA 6 mA 12 mA	BDC1T BDC2T BDC3T
	Bi-directional output for high speed	2 mA 6 mA	BDC1CT BDC2CT
LVTTLSchmitt	Bi-directional output	2 mA 6 mA 12 mA	BDH1T BDH2T BDH3T
	Bi-directional output for high speed	2 mA 6 mA	BDH1CT BDH2CT

Notes: * V_{OL} = 0.4 V (V_{DD} = 3.3 V)

** In addition to the N-channel open-drain bidirectional buffers specified in Table 3-4-3, a bidirectional-buffer configuration without test pins may be considered. If such a test-pinless configuration is desired, contact Seiko Epson or its distributor.

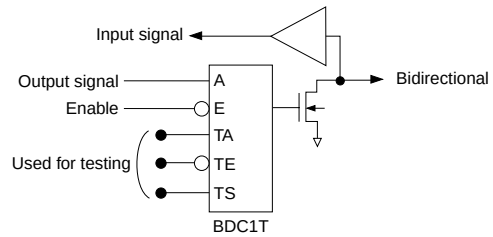


Figure 3-3 Example of an N-channel Open-Drain Bidirectional-Buffer Symbol

2) Tri-state type
As with tri-state output buffers, this type of cell cannot have its output pulled high to 5 V through the addition of a pull-up resistor external to the standard cell.

Table 3-4-4 Fail-Safe Cell Bidirectional Buffers

(V_{DD} = 3.3 V)

Input Level	Drain Type	Test Function	Output Latch Function	Speed	Output Current (mA) *1	Without a Resistor	Pull-down*1		Pull-up*1	
							50 kΩ	100 kΩ	50 kΩ	100 kΩ
LVTTL	Fail-Safe	N/A	N/A	Normal	-2 / 2	BB1	BB1D1	BB1D2	BB1P1	BB1P2
					-6 / 6	BB2	BB2D1	BB2D2	BB2P1	BB2P2
				HIGH-SPEED	-2 / 2	BB1C	BB1CD1	BB1CD2	BB1CP1	BB1CP2
					-6 / 6	BB2C	BB2CD1	BB2CD2	BB2CP1	BB2CP2
					-12 / 12	BB3A	BB3AD1	BB3AD2	BB3AP1	BB3AP2
LVTTL Schmitt	Fail-Safe	N/A	N/A	Normal	-2 / 2	BG1	BG1D1	BG1D2	—	—
					-6 / 6	BG2	BG2D1	BG2D2	—	—
				HIGH-SPEED	-2 / 2	BG1C	BG1CD1	BG1CD2	—	—
					-6 / 6	BG2C	BG2CD1	BG2CD2	—	—
					-12 / 12	BG3A	BG3AD1	BG3AD2	BG3AP1	BG3AP2

*1: The indicated resistance values apply to cases where V_{DD} = 3.3 V.

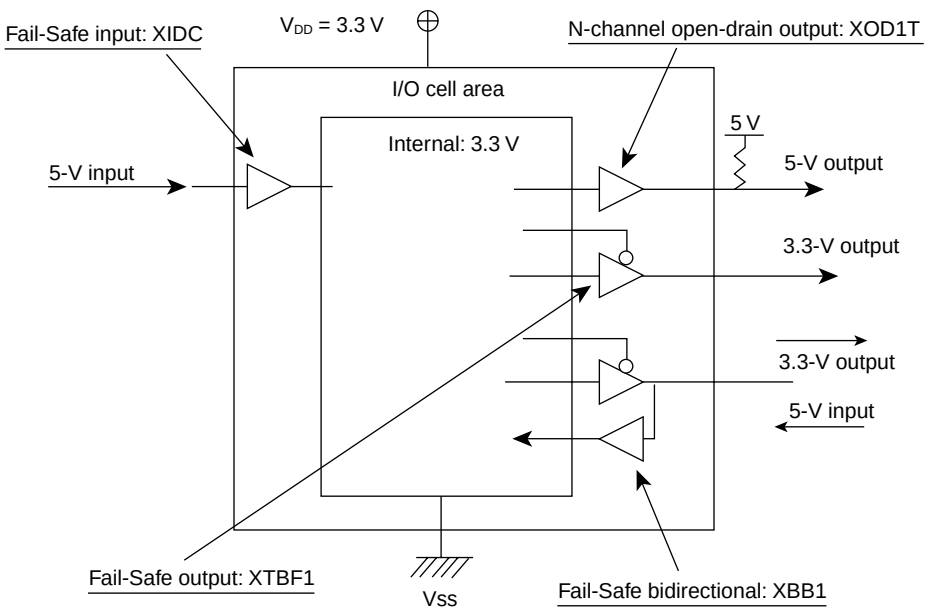


Figure 3-4 Typical Configuration of a Fail-Safe Cell

3.3 Configuration of Oscillator Circuits

3.3.1 When Configuring an Oscillator Circuit

In the configuration of an oscillator circuit, one of the configurations shown in Figure 3-5 applies, depending on the oscillator cell used. The input and output cells used in this case are a combination of XLIN and XLOUT.

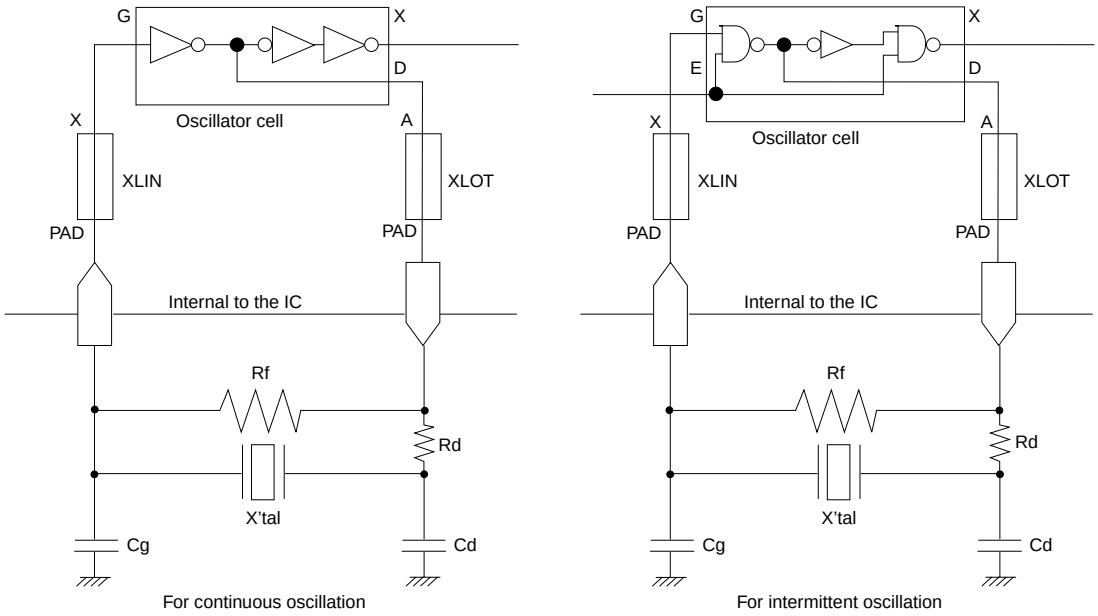


Figure 3-5 Method for Configuration of an Oscillator Circuit

3.3.2 Precautions on the Use of Oscillator Circuits

(1) Pin arrangement

- Position the oscillator circuit's input/output pins adjacent to each other, and position the power-supply pins (V_{DD} and V_{SS}) on either side of those input/output pins.
- Do not position other output pins adjacent to the oscillator circuit's input/output pins. In particular, outputs in phase or out of phase with the oscillator's waveform cannot be positioned close to the input/output pins. Make sure these outputs are positioned on the opposite side of the package.
- Try to position the oscillator circuit's input/output pins as close to the center as possible on the side of the package.

(2) Guide to selection of the oscillator cell

The possible oscillation frequencies are on the order of several 10 kHz to several 10 MHz. For details, contact Seiko Epson or its distributor.

(3) Setting external resistor and capacitor values

The oscillation characteristics depend on the various components (IC, X'tal, Rf, Rd, Cg, Cd, and the circuit board) that comprise the circuit. Therefore, be sure to choose the most suitable values for Rf, Rd, Cg, and Cd after carefully evaluating the performance of each part while mounted on the actual board.

(4) Guaranteed level

The oscillation characteristics depend on the various components (IC, X'tal, Rf, Rd, Cg, Cd, and the circuit board) that comprise the circuit. Therefore, Seiko Epson cannot guarantee the operation and characteristics of the oscillator. Customers are requested to verify the oscillation characteristics by performing careful evaluation using an ES sample.

(5) Oscillator-circuit configuration with dual power supplies

The oscillator-circuit configuration in this case is basically the same as in the case of a single-power-supply configuration. Because the oscillator cell is connected to the LV_{DD}-system power supply, use the input and output cells labeled "XLLIN" and "XLLOT," with the letter "L" prefixed to XLIN and XLOT.

3.4 Gated I/O Cells

3.4.1 Outline of Gated I/O Cells

Seiko Epson's S1K50000 series of Gated I/O cells make it possible to provide input to pins in the floating or Hi-Z state without the use of pull-up or pull-down circuits, an operation that was conventionally impossible. They also make it possible to cut off the high-voltage-side (HV_{DD}) power supply in a multi-power-supply design. Two types are available: one in which the power supply is cut off when the control-signal level is high, and another in which the power supply is cut off when the control-signal level is low, allowing the level for cutting off the power supply to be chosen in accordance with the circuit design.

3.4.2 Features of Gated I/O Cells

(1) Without limitations on the number of cells used or their placement, the Gated I/O cells can be positioned as desired by customers, providing freedom in circuit design.

(2) In a multi-power-supply design, the high-voltage-side (HV_{DD}) power supply can be cut off. However, because special measures are needed, if such a cut-off function is desired, contact Seiko Epson or its distributor.

(3) Inputs can be placed in the Hi-Z state without the use of pull-up or pull-down circuits.

(4) The supported input levels are the TTL level (when HV_{DD} and LV_{DD} = 5.0 V and 3.3 V) or the LVTTL level (when HV_{DD} and LV_{DD} = both 3.3 V; or V_{DD} = 3.3 V).

(5) Two types are available: one in which the power supply is cut off when the control-signal level is high, and another in which the power supply is cut off when the control-signal level is low.

(6) Because the Gated I/O cells are entirely of a CMOS structure, they help to reduce the chip's power consumption.

3.4.3 Precautions on the Use of Gated I/O Cells

(1) The Gated I/O cells cannot be subjected to Seiko Epson's standard input-level determination due to the circuit configuration. Therefore, if it is necessary for the input level to be determined by a tester, a test circuit must be configured separately. For an example of a test circuit, see Figure 3-6.

(2) When inputs are placed in the Hi-Z state using Gated I/O cells, the power supply must be cut off through control of the Gated I/O cell before the pin inputs float to a Hi-Z state. If inputs are placed in the Hi-Z state without the performance of this cut-off, a large current flows into the LSI as with ordinary cells, causing the device to malfunction. The same applies to the performance of connecting operations using control of the Gated I/O cell while inputs are left floating. In such a case, the logic levels latched into the device's internal logic cannot be guaranteed. Before you cut off the power to the high-voltage side (HV_{DD}), first contact EPSON's marketing division, as a special procedure is also required in this case.

(3) The same processing as specified in (2) is also necessary when the high-voltage-side (HV_{DD}) power supply is cut off through the use of a Gated I/O cell. Unless this processing is performed, the logic levels latched into the device's internal logic cannot be guaranteed. In addition, because special measures are required, if such a cut-off operation is desired, please contact Seiko Epson or its distributor.

Table 3-5-1 Gated Input Cells

(V_{DD} = 3.3 V, 2.0 V)

Drain Type	Input Level		Without a Resistor	Pull-down*1		Pull-up*1	
				50 kΩ	100 kΩ	50 kΩ	100 kΩ
Normal	CMOS	AND	XIBA	XIBAD1	XIBAD2	XIBAP1	XIBAP2
		OR	XIBO	XIBOD1	XIBOD2	XIBOP1	XIBOP2

*1: The indicated resistance values apply to cases where V_{DD} = 3.3 V.

Table 3-5-2 Gated Input Cells

(HV_{DD} = 5.0 V, 3.3 V, 2.0 V)

Drain Type	Input Level		Without a Resistor	Pull-down*1		Pull-up*1	
				60 kΩ	120 kΩ	60 kΩ	120 kΩ
Normal	CMOS	AND	XHIBA	XHIBAD1	XHIBAD2	XHIBAP1	XHIBAP2
		OR	XHIBO	XHIBOD1	XHIBOD2	XHIBOP1	XHIBOP2

*1: The indicated resistance values apply to cases where HV_{DD} = 5.0 V.

Table 3-5-3 Gated Bidirectional Cells

(AND Type, V_{DD} = 3.3 V, 2.0 V)

Input Level	Drain Type	Test Function	Output Latch Function	Speed	Output Current (mA)*1	Without a Resistor	Pull-down*1		Pull-up*1	
							50 kΩ	100 kΩ	50 kΩ	100 kΩ
CMOS	Normal	Available	N/A	NORMAL	-2 / 2	XBA1T	XBA1D1T	XBA1D2T	XBA1P1T	XBA1P2T
					-6 / 6	XBA2T	XBA2D1T	XBA2D2T	XBA2P1T	XBA2P2T
					-12 / 12	XBA3T	XBA3D1T	XBA3D2T	XBA3P1T	XBA3P2T
				HIGH SPEED	-2 / 2	XBA1CT	XBA1CD1T	XBA1CD2T	XBA1CP1T	XBA1CP2T
					-6 / 6	XBA2CT	XBA2CD1T	XBA2CD2T	XBA2CP1T	XBA2CP2T
					-12 / 12	XBA3AT	XBA3AD1T	XBA3AD2T	XBA3AP1T	XBA3AP2T
				LOW NOISE	-12 / 12	XBA3BT	XBA3BD1T	XBA3BD2T	XBA3BP1T	XBA3BP2T
		N/A	N/A	NORMAL	-2 / 2	XBA1	XBA1D1	XBA1D2	XBA1P1	XBA1P2
					-6 / 6	XBA2	XBA2D1	XBA2D2	XBA2P1	XBA2P2
					-12 / 12	XBA3	XBA3D1	XBA3D2	XBA3P1	XBA3P2
				HIGH SPEED	-2 / 2	XBA1C	XBA1CD1	XBA1CD2	XBA1CP1	XBA1CP2
					-6 / 6	XBA2C	XBA2CD1	XBA2CD2	XBA2CP1	XBA2CP2
					-12 / 12	XBA3A	XBA3AD1	XBA3AD2	XBA3AP1	XBA3AP2
				LOW NOISE	-12 / 12	XBA3B	XBA3BD1	XBA3BD2	XBA3BP1	XBA3BP2

*1: The indicated resistance values apply to cases where V_{DD} = 3.3 V.

Table 3-5-4 Gated Bidirectional Cells

(OR Type, V_{DD} = 3.3 V, 2.0 V)

Input Level	Drain Type	Test Function	Output Latch Function	Speed	Output Current (mA)*1	Without a Resistor	Pull-down*1		Pull-up*1	
							50 kΩ	100 kΩ	50 kΩ	100 kΩ
CMOS	Normal	Available	N/A	NORMAL	-2 / 2	XBO1T	XBO1D1T	XBO1D2T	XBO1P1T	XBO1P2T
					-6 / 6	XBO2T	XBO2D1T	XBO2D2T	XBO2P1T	XBO2P2T
					-12 / 12	XBO3T	XBO3D1T	XBO3D2T	XBO3P1T	XBO3P2T
				HIGH SPEED	-2 / 2	XBO1CT	XBO1CD1T	XBO1CD2T	XBO1CP1T	XBO1CP2T
					-6 / 6	XBO2CT	XBO2CD1T	XBO2CD2T	XBO2CP1T	XBO2CP2T
					-12 / 12	XBO3AT	XBO3AD1T	XBO3AD2T	XBO3AP1T	XBO3AP2T
				LOW NOISE	-12 / 12	XBO3BT	XBO3BD1T	XBO3BD2T	XBO3BP1T	XBO3BP2T
		N/A	N/A	NORMAL	-2 / 2	XBO1	XBO1D1	XBO1D2	XBO1P1	XBO1P2
					-6 / 6	XBO2	XBO2D1	XBO2D2	XBO2P1	XBO2P2
					-12 / 12	XBO3	XBO3D1	XBO3D2	XBO3P1	XBO3P2
				HIGH SPEED	-2 / 2	XBO1C	XBO1CD1	XBO1CD2	XBO1CP1	XBO1CP2
					-6 / 6	XBO2C	XBO2CD1	XBO2CD2	XBO2CP1	XBO2CP2
					-12 / 12	XBO3A	XBO3AD1	XBO3AD2	XBO3AP1	XBO3AP2
				LOW NOISE	-12 / 12	XBO3B	XBO3BD1	XBO3BD2	XBO3BP1	XBO3BP2

*1: The indicated resistance values apply to cases where V_{DD} = 3.3 V.

Table 3-5-5 Gated Bidirectional Cells

(AND Type, HV_{DD} = 5.0 V, 3.3 V, 2.0 V)

Input Level	Drain Type	Test Function	Output Latch Function	Speed	Output Current (mA)*1	Without a Resistor	Pull-down*1		Pull-up*1	
							60 kΩ	120 kΩ	60 kΩ	120 kΩ
CMOS	Normal	Available	N/A	NORMAL	-3 / 3	XHBA1T	XHBA1D1T	XHBA1D2T	XHBA1P1T	XHBA1P2T
					-8 / 8	XHBA2T	XHBA2D1T	XHBA2D2T	XHBA2P1T	XHBA2P2T
					-12 / 12	XHBA3T	XHBA3D1T	XHBA3D2T	XHBA3P1T	XHBA3P2T
				HIGH SPEED	-12 / 12	XHBA3AT	XHBA3AD1T	XHBA3AD2T	XHBA3AP1T	XHBA3AP2T
				LOW NOISE	-12 / 12	XHBA3BT	XHBA3BD1T	XHBA3BD2T	XHBA3BP1T	XHBA3BP2T
		N/A	N/A	NORMAL	-3 / 3	XHBA1	XHBA1D1	XHBA1D2	XHBA1P1	XHBA1P2
					-8 / 8	XHBA2	XHBA2D1	XHBA2D2	XHBA2P1	XHBA2P2
					-12 / 12	XHBA3	XHBA3D1	XHBA3D2	XHBA3P1	XHBA3P2
				HIGH SPEED	-12 / 12	XHBA3A	XHBA3AD1	XHBA3AD2	XHBA3AP1	XHBA3AP2
				LOW NOISE	-12 / 12	XHBA3B	XHBA3BD1	XHBA3BD2	XHBA3BP1	XHBA3BP2

*1: The indicated resistance values apply to cases where HV_{DD} = 5.0 V.

Table 3-5-6 Gated Bidirectional Cells

(AND Type, HV_{DD} = 5.0 V Only)

Input Level	Drain Type	Test Function	Output Latch Function	Speed	Output Current (mA)*1	Without a Resistor	Pull-down*1		Pull-up*1	
							60 kΩ	120 kΩ	60 kΩ	120 kΩ
CMOS	Normal	Available	N/A	NORMAL	-12 / 24	XHBA4T	XHBA4D1T	XHBA4D2T	XHBA4P1T	XHBA4P2T
				HIGH SPEED	-12 / 24	XHBA4AT	XHBA4AD1T	XHBA4AD2T	XHBA4AP1T	XHBA4AP2T
				LOW NOISE	-12 / 24	XHBA4BT	XHBA4BD1T	XHBA4BD2T	XHBA4BP1T	XHBA4BP2T
		N/A	N/A	NORMAL	-12 / 24	XHBA4	XHBA4D1	XHBA4D2	XHBA4P1	XHBA4P2
				HIGH SPEED	-12 / 24	XHBA4A	XHBA4AD1	XHBA4AD2	XHBA4AP1	XHBA4AP2
				LOW NOISE	-12 / 24	XHBA4B	XHBA4BD1	XHBA4BD2	XHBA4BP1	XHBA4BP2

*1: The indicated resistance values apply to cases where HV_{DD} = 5.0 V.

Table 3-5-7 Gated Bidirectional Cells

(OR Type, HV_{DD} = 5.0 V, 3.3 V, 2.0 V)

Input Level	Drain Type	Test Function	Output Latch Function	Speed	Output Current (mA)*1	Without a Resistor	Pull-down*1		Pull-up*1	
							60 kΩ	120 kΩ	60 kΩ	120 kΩ
CMOS	Normal	Available	N/A	NORMAL	-3 / 3	XHBO1T	XHBO1D1T	XHBO1D2T	XHBO1P1T	XHBO1P2T
					-8 / 8	XHBO2T	XHBO2D1T	XHBO2D2T	XHBO2P1T	XHBO2P2T
					-12 / 12	XHBOT	XHBO3D1T	XHBO3D2T	XHBO3P1T	XHBO3P2T
				HIGH SPEED	-12 / 12	XHBO3AT	XHBO3AD1T	XHBO3AD2T	XHBO3AP1T	XHBO3AP2T
				LOW NOISE	-12 / 12	XHBO3BT	XHBO3BD1T	XHBO3BD2T	XHBO3BP1T	XHBO3BP2T
		N/A	N/A	NORMAL	-3 / 3	XHBO1	XHBO1D1	XHBO1D2	XHBO1P1	XHBO1P2
					-8 / 8	XHBO2	XHBO2D1	XHBO2D2	XHBO2P1	XHBO2P2
					-12 / 12	XHBO3	XHBO3D1	XHBO3D2	XHBO3P1	XHBO3P2
				HIGH SPEED	-12 / 12	XHBO3A	XHBO3AD1	XHBO3AD2	XHBO3AP1	XHBO3AP2
				LOW NOISE	-12 / 12	XHBO3B	XHBO3BD1	XHBO3BD2	XHBO3BP1	XHBO3BP2

*1: The indicated resistance values apply to cases where HV_{DD} = 5.0 V.

Table 3-5-8 Gated Bidirectional Cells

(OR Type, HV_{DD} = 5.0 V Only)

Input Level	Drain Type	Test Function	Output Latch Function	Speed	Output Current (mA)*1	Without a Resistor	Pull-down*1		Pull-up*1	
							60 kΩ	120 kΩ	60 kΩ	120 kΩ
CMOS	Normal	Available	N/A	NORMAL	-12 / 24	XHBO4T	XHBO4D1T	XHBO4D2T	XHBO4P1T	XHBO4P2T
				HIGH SPEED	-12 / 24	XHBO4AT	XHBO4AD1T	XHBO4AD2T	XHBO4AP1T	XHBO4AP2T
				LOW NOISE	-12 / 24	XHBO4BT	XHBO4BD1T	XHBO4BD2T	XHBO4BP1T	XHBO4BP2T
		N/A	N/A	NORMAL	-12 / 24	XHBO4	XHBO4D1	XHBO4D2	XHBO4P1	XHBO4P2
				HIGH SPEED	-12 / 24	XHBO4A	XHBO4AD1	XHBO4AD2	XHBO4AP1	XHBO4AP2
				LOW NOISE	-12 / 24	XHBO4B	XHBO4BD1	XHBO4BD2	XHBO4BP1	XHBO4BP2

*1: The indicated resistance values apply to cases where HV_{DD} = 5.0 V.

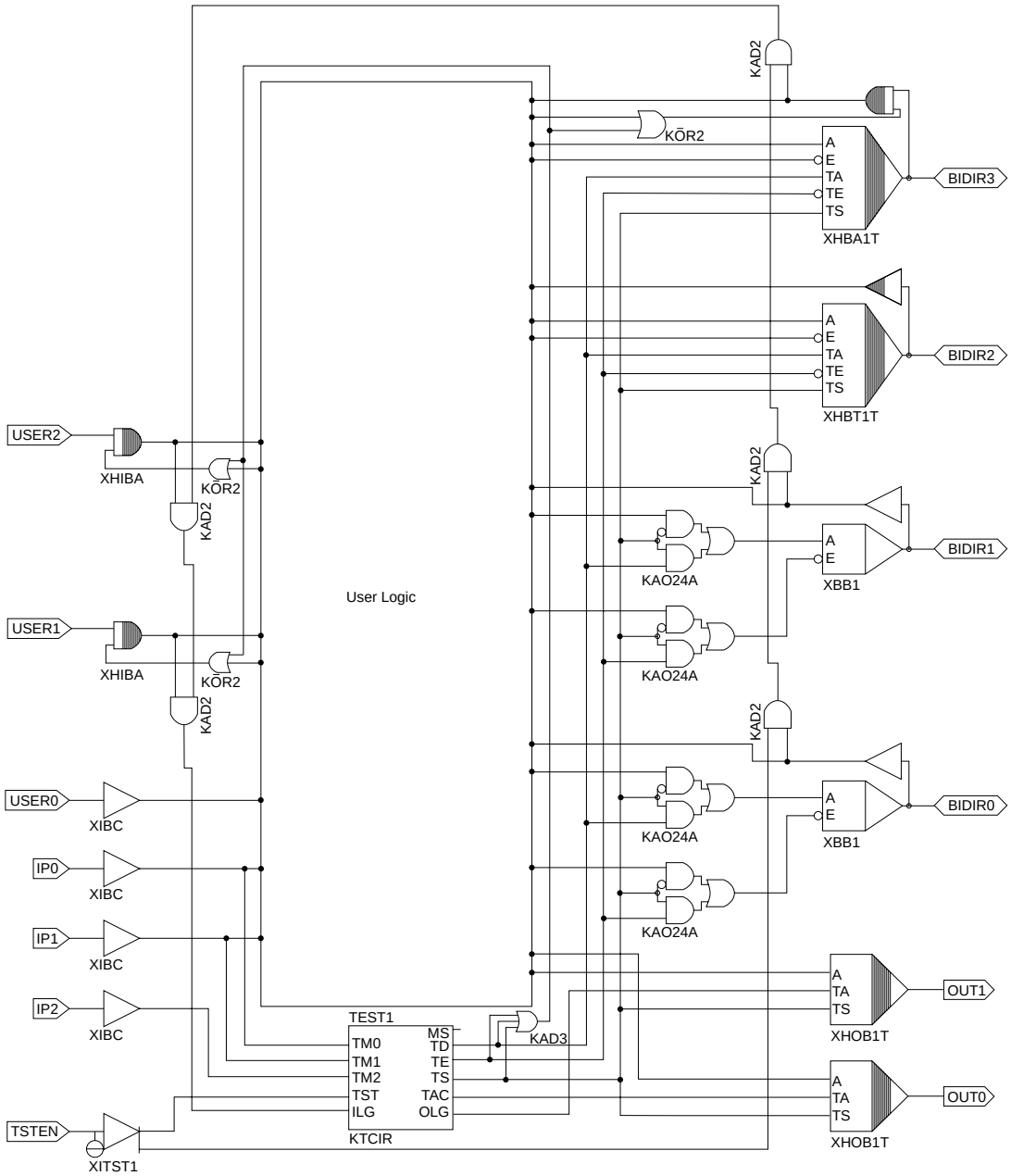


Figure 3-6 Typical Test Circuit for Fail-Safe and Gated Cells

In the example circuit shown above, single-power-supply and dual-power-supply I/O cells coexist for reasons of convenience. Please be aware that in actual circuits these two types of cells cannot coexist.

Chapter 4 Circuit Design Taking Testability into Account

Prior to the shipment of standard cells from the factory, a product test is conducted through the use of an LSI tester.

Therefore, testability must fully be taken into account in the circuit design. Consider the following points in the design of a circuit.

4.1 Consideration for Circuit Initialization

Many flip-flops are used in a circuit. However, when tests are conducted using an LSI tester or a circuit is simulated, all of the flip-flops in the initial state are in an X (indeterminate) state.

Therefore, depending on the circuit configuration, it will be impossible to initialize the circuit, or a huge test pattern may be required for initialization.

Therefore, in the design of a circuit, use flip-flops with a reset input or take other similar measures to ensure that the circuit can be initialized easily.

4.2 Consideration for Reduction of the Test-Pattern Size

As the circuit size increases, so does the size of the test pattern. However, test patterns are subject to the following limitations imposed by an LSI tester.

Number of events per test pattern	:	Up to 256K
Number of test patterns	:	Up to 30
Total number of events in test patterns	:	Within 1M

These limitations apply to all types of test patterns, such as those for DC testing, for Z inspection, for a test circuit, and ROM or megacell test patterns prepared by Seiko Epson. For details on the number of ROM and megacell test patters and the number of events in those test patterns, contact Seiko Epson or its distributor. Regarding test patterns for RAM testing, please note that although the reference patterns prepared by customers are included in those that are subject to said limitations, the full test patterns for RAM to be prepared by Seiko Epson are not included.

In the design of a circuit, incorporate measures to increase its testability, thereby reducing the size of the test patterns required for it by, for example, installing a test pin that allows a clock to be fed into the middle of multistage counters or adding a test pin that allows the LSI's internal signals to be monitored.

4.3 Circuit Configuration to Facilitate DC and AC Tests

4.3.1 Configuration of a Test Circuit

The S1K50000 series requires a test-circuit configuration allowing DC and AC tests to be conducted efficiently.

If such a test circuit is not configured in your circuit design, contact Seiko Epson or its distributor for confirmation.

Figure 4-1 shows an example of a test circuit. Use this circuit for reference purposes in the design of a test circuit.

Note that several input and output pins are required for use with a test circuit.

(1) Adding and selecting pins used for testing

Add and select the following four types of test pins.

- Test-mode switch pin : 1 pc.
- Test-mode select input pin : 3 pcs.
- AC test monitor output pin : 1 pc.
- DC test monitor output pin : 1 pc.

Table 4-1 Restrictions on Test Pins

Type of Test Pin	Number of Pins	Pin Name (example)	Restrictions, etc.
Test-mode switch pin	1 pc.	TSTEN	Dedicated input pin. Use XITST1 for the input buffer. High: test mode; Low: normal mode
Test-mode select input pin	3 pcs.	INP0 INP1 INP2	Shareable input pin. This pin cannot be shared with bidirectional pins. Avoid sharing this pin with input pins that have a critical path.
AC test monitor output pin	1 pc.	OUT3	Shareable output pin. This pin cannot be shared with bidirectional 3-state pins or N-channel open-drain cells. Output buffers TYPE S and TYPE M cannot be used.
DC test monitor output pin	1 pc.	OUT4	Shareable output pin. This pin cannot be shared with bidirectional 3-state pins or N-channel open-drain cells.
Output and input/output pins	—	—	Use an input/output buffer with a test mode.

(2) DC test

Measurement is conducted to determine whether all of the input and output pins satisfy the specifications associated with DC characteristics. If a test circuit is not available, customers will be requested to create a test pattern that makes it possible to measure DC characteristics. Many man-hours may be required to create this test pattern. Use of a test circuit makes it easy to create a test pattern and measure DC characteristics.

(3) AC test

Measurement is made of the pin-to-pin (input pin to output pin) speed. In cases in which the actual operating frequency cannot be inspected by an LSI tester, the operating speed can be guaranteed by measuring the delay in a specific path.

The AC test monitor output pin is used to evaluate lot-to-lot dispersion at Seiko Epson by measuring a dedicated AC path (cell name: KACP1). (When using a test circuit, be sure to insert KACP1 in its design.)

(4) Adding a test-mode control circuit

An example circuit in cases in which you configure a test circuit is shown below. Refer to the example test circuit shown in Figure 4-1.

a. Select four test input pins and two output pins.

Test-mode switch pin	: 1 pc.
Test-mode select input pin (shared input pin)	: 3 pcs.
AC test monitor output pin (shared output pin)	: 1 pc.
DC test monitor output pin (shared output pin)	: 1 pc.

b. Use the input cell XITST1 for the test-mode select input pins (INP0, 1, 2).

c. The input buffers for the test-mode select input pins (INP0, 1, 2) vary depending on the input buffers of the user application. However, avoid sharing these pins with input pins that have a critical path.

d. The output buffers of the test monitor output pins (OUT3, OUT4) vary depending on the output buffers of the user application. However, avoid sharing these pins with output pins that have a critical path.

e. For all output and bidirectional pins, be sure to use input/output buffers with a test mode.

f. Create a test-mode control circuit (KTCIR), and include it in the circuit design.

g. Make sure the input buffer (XITST1) for the test-mode switch pin has its output pins X and LG connected to the TST and ILG pins of the KTCIR.

h. Make sure the input buffers for the test-mode select input pins have their outputs connected to the input pins of the KTCIR.

Connect the INP0 input buffer's output to the TM0 pin of the KTCIR.
Connect the INP1 input buffer's output to the TM1 pin of the KTCIR.
Connect the INP2 input buffer's output to the TM2 pin of the KTCIR.

i. Make sure the output pins of the test-mode control circuit (KTCIR) are connected to the input pins of the input/output buffers.

Connect the KTCIR's output pin (TAC) to the TA pin of the AC test monitor output pin (OUT3)'s input/output buffer.

Connect the KTCIR's output pin (TS) to the TS pins of all input/output buffers.

Connect the KTCIR's output pin (TD) to the TA pins of all input/output buffers, except for the test monitor output pins (OUT3, OUT4).

Connect the KTCIR's output pin (TE) to the TE pins of the input/output buffers of the tri-state pin (OUT2) and bidirectional pin (BID1).

Connect the KTCIR's output pin (OLG) to the TA pin of the DC test monitor output pin (OUT4)'s input/output buffer.

j. Use the KTCIR's output pin (MS) to control each macro when RAM and functional cells are included.

k. Adjust the signals to the input/output buffer's TA, TE, and TS pins, to ensure that their fan-out limits will not be exceeded.

(5) Setting the test mode

a. DC test

- Quiescent-current measurement mode

TSTEN	. . .	High

- Output-characteristic (V_{OH}/V_{OL}) measurement mode

TSTEN	. . .	High
INP0	. . .	Low
INP1	. . .	High/low input
INP2	. . .	Low

- Input-characteristic (V_{IH}/V_{IL}) measurement mode

TSTEN	. . .	High
Measured pin *1	. . .	High/low input
Unmeasured pin	. . .	High

*1: Apply to all input and bidirectional pins, except for TESTEN.

b. Dedicated AC path measurement mode

TSTEN	. . .	High
INP0	. . .	Low
INP1	. . .	Low
INP2	. . .	High/low input

Table 4-2 Test-Circuit Truth Table

INPUT					OUTPUT					
TST	ILG	TM2	TM1	TM0	TS	TD	TE	TAC	OLG	MS
0	X	X	X	X	0	0	0	0	0	0
1	1	X	X	X	1	X	X	X	1	X
1	0	X	X	X	1	X	X	X	0	X
1	X	1	1	1	1	1	1	1	X	0
1	X	1	1	0	1	1	1	1	X	0
1	X	1	0	1	1	1	1	1	X	0
1	X	0	1	1	1	1	1	1	X	0
1	X	0	0	1	1	1	0	1	X	1
1	X	0	1	0	1	1	0	1	X	0
1	X	1	0	0	1	0	0	1	X	0
1	X	0	0	0	1	0	0	0	X	0

6) Creating test patterns

In order for AC and DC tests to be conducted efficiently, customers are requested to design a test circuit as well as a test pattern.

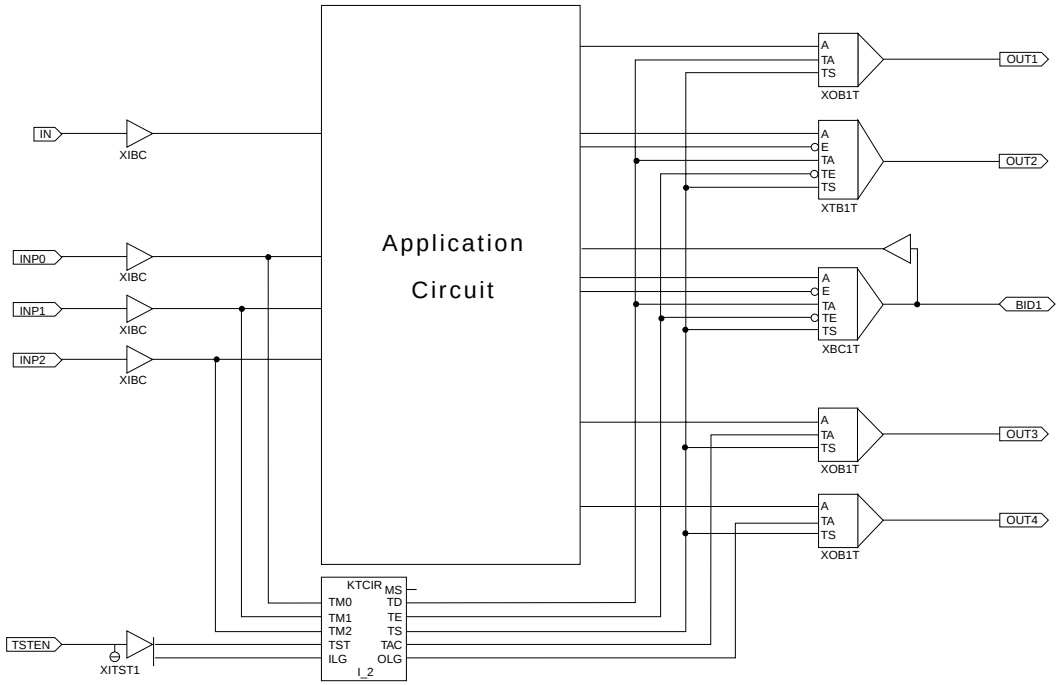
Figure 4-2 shows an example test pattern for the example test circuit shown in Figure 4-1. Note the following in the design of a test pattern:

a. Create a test pattern like the one shown in the example separately from the patterns used to verify the circuit's functionality. Seiko Epson creates only the test patterns of the input logic level inspection mode.

b. All pins used in the circuit must be written in this test pattern.

c. Also write test pins (e.g., TSTEN) in the patterns used to verify the circuit's functionality. In such a case, make sure the input level of the test pin (e.g., TSTEN) is low (= 0).

d. When the input level of the test pin (e.g., TSTEN) is high (= 1), all of the pull-up/pull-down resistors are disabled (inactive).



<Internal circuit of the KTCIR>

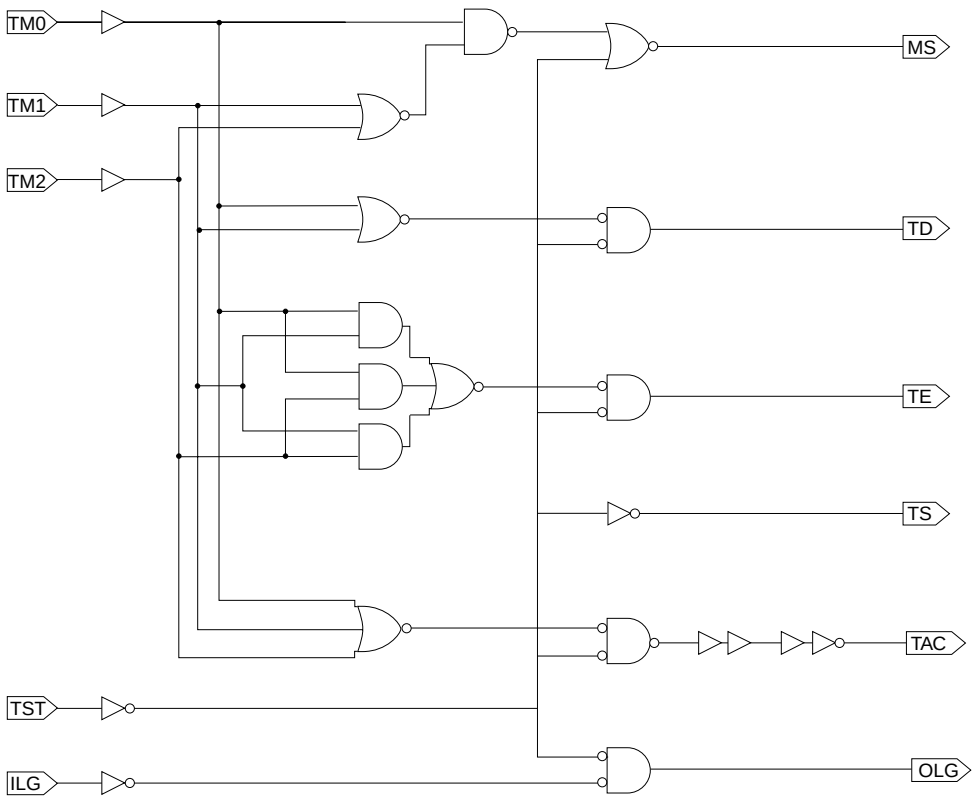


Figure 4-1 Example of a Test Circuit

<Example of APF format>

```
* EXAMPLE  of Test Patterr forAC  & DC  Test

  $RATE  200000
  $STROBE  185000
  $RESOLUTIO N  0.001ns

  $NODE
  TSTEN    I   0
  INP0     I   0
  INP1     I   0
  INP2     I   0
  IN       I   0
  BID1     BU  0
  OUT1     0
  OUT2     0
  OUT3     0
  OUT4     0
  $ENDNODE

  $PATTERN                                                    (High) (Input low)

  #            TIIIIBOOOO
  #            SNNNNIUUUU
  #            TPPP  DTTTT
  #            E012 11234
  #            N
  #
  #            IIIIIBOOOO
  #                 U
  #

           0   0000.XXXXX
           1   1000.LLLLX ; Pull-up/down off                          →Measures the dedicated AC path
           2   1000.LLLLX ; AC path output (high), other outputs (low) →As above
           3   1001.LLLHX ; AC path output (low), other outputs (low)  →      ↑
           4   1000.LLLLX ; AC path output (low), other outputs (low)  →      ↑
           5   1101.0HZHX ; Off state, normal output (high) (input low) →Measures the off-state leakage curren
           6   1101.1HZHX ; Off state, normal output (high) (input high) →      ↑
           7   1000.LLLLX ; Output (low)                              →Measures the output characteristics
           8   1010.HHHHX ; Output (high)                             →      ↑

  $ENDPATTERN

  #
  # EOF
```

Note: A period (.) denotes a 1 or 0.

Figure 4-2 Example of a Test Pattern Created for a Test Option

4.4 Test Circuit for Functional Cells

When functional cells are used, huge numbers of test patterns and large amounts of time are required to verify the operation of the entire circuit (including the user circuit). Therefore, customers are requested to design a test circuit in such a way that operation of the functional cells and user circuit can be verified as single units.

In the design of a test circuit, note the following.

4.4.1 Configuration of a Test Circuit

(1) Add a test circuit so that each functional cell and the user circuit can be separated and measured individually for each block, with the pins of the functional cells leading out to external pins.

(2) Even when fixing the inputs of the functional cells to V_{SS} or V_{DD}, install a test circuit to enable test input.

(3) Even when not using the output pins of the functional cells, install a test circuit to allow all outputs of the functional cells to be observed from external pins.

(4) Do not use multiple output or input pins of the functional cells collectively as one test-shareable pin.

(5) Do not use a sequential circuit in a test circuit that is used to test the functional cells.

(6) Do not feed an input signal from the test input pin into the function cells after inverting its logic level. In addition, do not forward the output signals of the functional cells to the test output pin after inverting their logic level.

(7) If the functional cell's input and output pins are led out directly as pins of the IC, it is not necessary to attach a test circuit.

(8) Do not use bidirectional buffers with a pull-up for the test-mode switch pin. Bidirectional buffers with a pull-down are acceptable.

4.4.2 Test Patterns

Broadly classified, there are the following three types of test patterns:

1) Test pattern for testing only the user circuit
2) Test pattern for testing the entire circuit
3) Test pattern for testing only the functional cells

The test patterns that must be created by customers are items 1) and 2) above. The test pattern in item 3) does not need to be created by customers. Existing test patterns at Seiko Epson are used.

Please note, however, that the test patterns for the functional cells (i.e., the existing test patterns) cannot be disclosed to customers.

4.4.3 Test-Circuit Information

Customers are requested to provide the following information regarding a test circuit, as it is necessary to test the functional cells during simulation and shipment inspection:

(1) Clearly indicate which pins of the function cells are connected to which pins of the IC in test mode.

(2) If a test circuit is configured to allow multiple functional cells to be tested from a single test pin, clearly indicate the relationship between the test mode and the selected functional-cell names.

(3) Particularly when using two or more of the same functional cell, assign the functional-cell names a sequential number in the drawing, clearly indicating for which functional cell the test pin is used.

(4) Clearly indicate the method for switching to test mode.

Chapter 5 Propagation Delay Time and Timing Design

The delay time in an LSI is determined by the delay time in each cell itself, and by delays caused by capacitive loads such as wiring and input capacitances connected to the outputs of those cells.

The delay time fluctuates depending on the power-supply voltage, ambient temperature, and process conditions. It also fluctuates in accordance with factors associated with the circuit configuration, such as input waveforms, input logic levels, and mirror effects. The S1K50000 series offers a highly accurate delay calculation environment in which these fluctuating factors are taken into account. Therefore, please note that the delay calculations differ from those performed using the values listed in the “Standard Cell S1K50000-Series MSI Cell Library” described later.

5.1 Precautions Regarding the Relationship between Ta and Tj

The delay in a CMOS IC basically fluctuates with Tj (junction temperature). IC specifications, on the other hand, are generally represented by Ta (ambient temperature). However, the relationship between Tj and Ta is not constant; it varies depending on the package’s thermal resistance and the power consumption of that IC. (For details, see Section 7.2, “Power-Consumption Limitations.”)

For ASICs, the package’s thermal resistance and the power consumption vary with each circuit and application. Therefore, strictly speaking, specification examination based on Ta is difficult. As a result, delay libraries are available with Seiko Epson’s S1K50000 series to help you verify the circuit design at its early stage with respect to the approximate guidelines given below.

* Tj = 0 to 85 [°C] library for Ta = 0 to 70 [°C]
* Tj = -40 to 125 [°C] library for Ta = -40 to 85 [°C]

Of course, if the relationship between Ta and Tj varies significantly when the package’s thermal resistance and the power consumption are estimated, customers will be recommended to use the Tj = -40 to 125 [°C] library for Ta = 0 to 70 [°C], or requested to have other conditions added.

5.2 Simplified Delay Models

The propagation delay time, tpd, is obtained using the equation shown below.

$$t_{pd} = T_0 + K \times (\sum \text{Load A} + \text{Load B})$$

where T_0 : nonloaded delay [ps]
K : coefficient of loaded delay [ps/LU]
Load A : input load capacitance of the connected cell [LU]
Load B : wiring load capacitance [LU]

Note: The values of T_0 and K vary depending on the operating voltage, ambient temperature, and process conditions. Use the values listed in the cell library.

The Typ. values of T_0 and K (V_{DD} = center value; Ta = 25°C, process = center value) are listed in the "Standard Cell S1K50000-Series MSI Cell Library." Choose the Typ. values of T_0 and K in accordance with the intended power-supply voltage.

The Min. values of T_0 and K (V_{DD} = highest value; Ta = lowest value; process = Fast) and Max. values (V_{DD} = lowest value; Ta = highest value; process = Slow) can be obtained by multiplying said Typ. values by a dispersion coefficient of delay, M. (These Min. and Max. values are important in verifying that the delay in the circuit is within the desired specifications, even in the presence of dispersions in V_{DD}, Ta, or the process.)

The dispersion coefficient of delay, M, is calculated as follows:

$$M = MV \times MT \times MP$$

where MV : coefficient of power-supply-voltage fluctuation
MT : coefficient of ambient-temperature fluctuation
MP : coefficient of process fluctuation

Although MV and MT can be read out from the characteristic graphs shown in the "Standard Cell S1K50000-Series MSI Cell Library," we recommend use of the standard dispersion coefficients of delay, M, listed in Table 5-1 below. For the dispersion coefficients of delay outside the standard power-supply-voltage and ambient-temperature ranges, contact Seiko Epson or its distributor.

Note 1: The delay in a predriver with a level shifter cannot be obtained simply by multiplying the Typ. value by a dispersion coefficient of delay, as described above. Precalculated Min. and Max. values are listed along with the Typ. values in the "Standard Cell S1K50000-Series MSI Cell Library." See Section 9.4, "Calculating the Delay Time in a Dual-Power-Supply System," in this manual.

Table 5-1 Dispersion Coefficient of Delay, M (Ordinary Functional Cells)

Conditions	M Value			Usage
	Min.	Typ.	Max.	
Power-supply voltage: 5.0 V ± 5% Ta : 0 to 70°C*1	(0.70)	(1.00)	(1.48)	Use this to multiply the Typ. values of T_0 and K at HV_{DD} = 5.0 V.
Power-supply voltage: 5.0 V ± 10% Ta : -40 to 85°C*2	(0.62)	(1.00)	(1.64)	
Power-supply voltage: 3.3 V ± 0.3 V Ta : 0 to 70°C*1	0.60 (0.65)	1.00 (1.00)	1.60 (1.51)	Use this to multiply the Typ. values of T_0 and K at V_{DD} = 3.3 V.
Power-supply voltage: 3.3 V ± 0.3 V Ta : -40 to 85°C*2	0.58 (0.62)	1.00 (1.00)	1.67 (1.57)	
Power-supply voltage: 2.0 V ± 0.2 V Ta : 0 to 70°C*1	0.42 (0.39)	1.00 (1.00)	2.49 (2.94)	Use this to multiply the Typ. values of T_0 and K at V_{DD} = 2.0 V.
Power-supply voltage: 2.0 V ± 0.2 V Ta : -40 to 85°C*2	0.42 (0.39)	1.00 (1.00)	2.68 (3.38)	

Values enclosed in ( ) are those for I/O buffers; otherwise, the values are for MSI cells.

*1: This temperature range assumes Tj = 0°C to 85°C.

*2: This temperature range assumes Tj = -40°C to 125°C.

5.3 Load Due to Input Capacitance (Load A)

The delay time in a logic gate depends on the sum total of the input capacitances of the logic gates (fan-in) connected to the output pin of that gate. The input capacitance of each gate (fan-in) and the loading limits of their output pin (fan-out) are listed in the "Standard Cell S1K50000-Series MSI Cell Library."

In the design of a circuit, make sure the sum total of fan-in will not exceed the output pin's fan-out.

- Example of the calculation of Load A

  The following shows an example of the calculation of Load A using the circuit diagram shown in Figure 5-1 and the data given in Table 5-2.

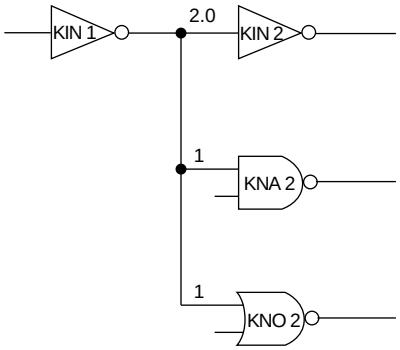


Figure 5-1 Circuit for Example Load-A Calculation

Table 5-2 Data Used for Example Load-A Calculation

cell	Input		Output	
	Pin	Fan-in	Pin	Fan-out
KIN1	A	1.0	X	17.7
KIN2	A	2.0	X	36.9
KNA2	A1 A2	1.0 1.0	X	15.4
KNO2	A1 A2	1.0 1.0	X	8.9

The fan-in values for KIN2, KNA2, and KNO2 are given in Table 5-2. Their sum is the value of ∑ Load A.

$$\sum \text{Load A (N1)} = (\text{Fan-in of KIN2}) + (\text{Fan-in of KNA2}) + (\text{Fan-in of KNO2})$$
$$= 2.0 + 1 + 1 = 4.0$$

5.4 Load Due to Wiring Capacitance (Load B)

The load due to the wiring capacitance between cells (Load B) is characteristic, in that exact values for it cannot be calculated until placement & routing are actually performed. However, there is a certain correlationship between Load B and the number of wiring branches (number of nodes) connected to the outputs of cells, making it possible to statistically predict an assumed value. The assumed wiring capacitance of each master is listed in the "Standard Cell S1K50000-Series MSI Cell Library."

5.5 Calculating the Propagation Delay Time

The following shows an example of the calculation of the propagation delay time using the circuit shown in Figure 5-2 (operating at 3.3 V) and the data given in Table 5-3.

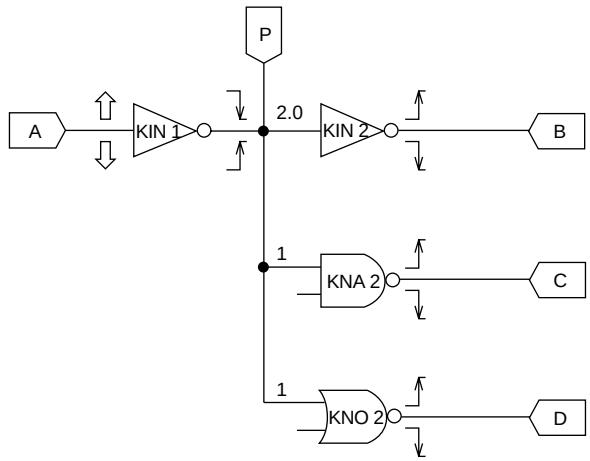


Figure 5-2 Circuit for Example Calculation of the Propagation Delay Time

Table 5-3 Characteristics of Cells (Power-Supply Voltage of 3.3 V)

Cell	Input		Output		t_{pd} (Typ.)				
	Pin	Fan-in	Pin	Fan-out	From	To	Edge	T_0 (ps)	K (ps/LU)
KIN1	A	1.0	X	17.7	A	X	↑	42	20.9
							↓	41	15.0
KIN2	A	2.0	X	36.9	A	X	↑	32	10.1
							↓	32	7.1
KNA2	A1	1.0	X	15.4	A1	X	↑	57	20.1
							↓	59	25.2

Table 5-3 Characteristics of Cells (Power-Supply Voltage of 3.3 V)

Cell	Input		Output		t_{pd} (Typ.)				
	Pin	Fan-in	Pin	Fan-out	From	To	Edge	T_0 (ps)	K (ps/LU)
KNO2	A1	1.0	X	8.9	A1	X	↑	75	40.6
							↓	51	14.2

Here, calculation is performed assuming that Load B for NODE P is 2 [LU]. It should be noted that the nonloaded delay time is added to the propagation delay time, and that the rise and fall of each output must also be taken into conside ration.

- Example calculation for paths A → B, A → C, A → D (t_{pd} = Typ.)

(1) Path A → P : $t_{pd} = t_{pd}$ (KIN1)

t_{pd} (A ↑ → P ↓) = $T_0 + K \times$ (Load A + Load B)
= 41 + 15.0 × (4+2)
= 131 (ps)

t_{pd} (A ↓ → P ↑) = $T_0 + K \times$ (Load A + Load B)
= 42 + 20.9 × (4+2)
= 167.4 (ps)

(2) Path A → B : $t_{pd} = t_{pd}$ (KIN1) + t_{pd} (KIN2)

t_{pd} (A ↑ → P ↑) = t_{pd} (A ↑ → P ↓) + t_{pd} (P ↓ → B ↑)
= 131.0 + T_0
= 131.0 + 32
= 163 (ps)

t_{pd} (A ↓ → P ↓) = t_{pd} (A ↓ → P ↑) + t_{pd} (P ↑ → B ↓)
= 167.4 + T_0
= 167.4 + 32
= 199.4 (ps)

(3) Path A → C : $t_{pd} = t_{pd}$ (KIN1) + t_{pd} (KNA2)

t_{pd} (A ↑ → C ↑) = t_{pd} (A ↑ → P ↓) + t_{pd} (P ↓ → C ↑)
= 131.0 + T_0
= 131.0 + 57
= 188.0 (ps)

t_{pd} (A ↓ → C ↓) = t_{pd} (A ↓ → P ↑) + t_{pd} (P ↑ → C ↓)
= 167.4 + T_0
= 167.4 + 59
= 226.4 (ps)

(4) Path A → D : $t_{pd} = t_{pd}$ (KIN1) + t_{pd} (KNO2)

t_{pd} (A ↑ → D ↑) = t_{pd} (A ↑ → P ↓) + t_{pd} (P ↓ → D ↑)
= 131.0 + T_0
= 131.0 + 75
= 206.0 (ps)

t_{pd} (A ↓ → D ↓) = t_{pd} (A ↓ → P ↑) + t_{pd} (P ↑ → D ↓)
= 167.4 + T_0
= 167.4 + 51
= 218.4 (ps)

5.6 Calculating the Output-Buffer Delay Time

Letting the load capacitance connected to the output buffer be CL, the delay time tpd is obtained using the equation shown below.

$t_{pd} = T_0$ (output cell) + K (output cell) x $C_L/10$

where T_0 (output cell)	:	nonloaded delay of output cell	[ps]
K (output cell)	:	loaded delay coefficient of output cell	[ps/10 pF]
C_L	:	connected load capacitance	[pF]

For details on the nonloaded and loaded delay coefficients of output cells, see the “Standard Cell S1K50000-Series MSI Cell Library.”

5.7 Flip-Flop Setup and Hold Times

The signal timing applied by flip-flops and an MSI sequential circuit consisting of flip-flops play an important role in the proper operation of the configured circuit with the intended logic. The flip-flop’s setup and hold times are closely associated with this signal timing. Data which, when entered or changed in state, failed to meet the timing requirements regulated by the setup and hold times cannot be written correctly to the flip-flop circuit. Therefore, the signal timing must be designed in consideration of these setup and hold times.

(1) Minimum pulse width

In flip-flops and MSIs consisting of flip-flops, this refers to the minimum width of an input pulse between the leading and trailing edges of its waveform. Pulses applied in widths smaller than this value are not only ineffective as signals, but may also cause malfunction.

The following three minimum pulse widths are defined:

- Minimum pulse width of a clock signal
- Minimum pulse width of a set signal
- Minimum pulse width of a reset signal

(2) Setup time

In flip-flops and MSIs consisting of flip-flops, if data is to be read correctly, it must be set to the valid state before a change in the active clock edge occurs. The time required for it is referred to as the “setup time.”

(3) Hold time

In flip-flops and MSIs consisting of flip-flops, if data is to be read correctly, it should be held in the valid state after the active clock edge is entered. The time required for this is referred to as the “hold time.”

(4) Release time (setup)

In flip-flops and MSIs consisting of flip-flops, the time before the clock pulse can change state after a set/reset input has been deasserted is referred to as the “release time.”

(5) Release time (hold)

In flip-flops and MSIs consisting of flip-flops, the set/reset input state must be maintained after an active clock pulse is entered. This time is referred to as the “release time (hold).”

(6) Set/reset setup time

In flip-flops and MSIs consisting of flip-flops, the time before a reset input can be asserted after a set input has been deasserted is referred to as the “set/reset setup time.”

(7) Set/reset hold time

In flip-flops and MSIs consisting of flip-flops, a reset signal once asserted must be held active until the next time a set signal is asserted. This time is referred to as the “set/reset hold time.”

For details on the timing error messages output during simulation, see the user’s manual of each tool.

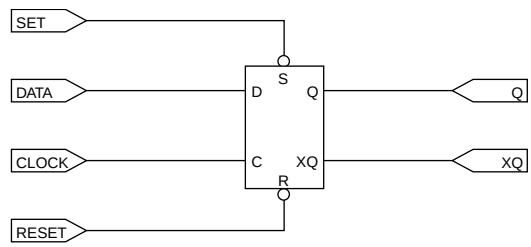


Figure 5-3 KDFSR

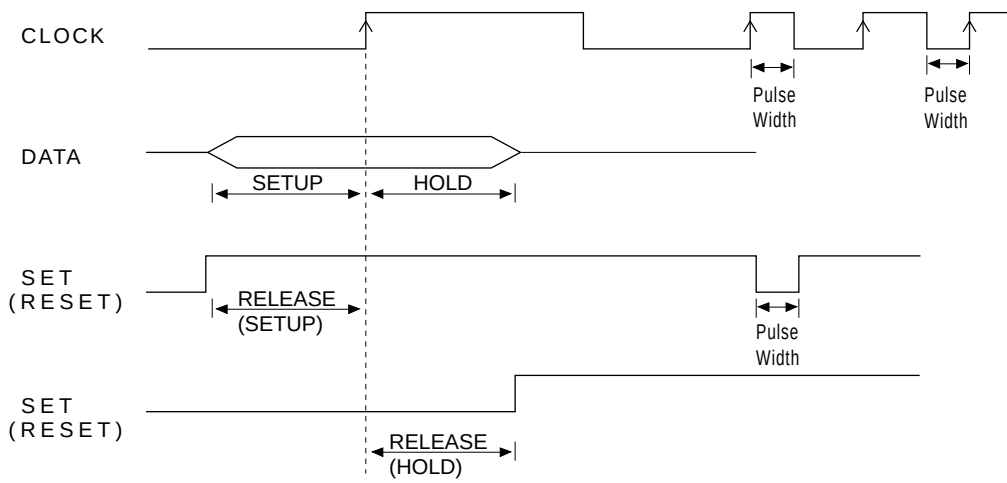


Figure 5-4 Timing Waveform Diagram 1 (explanation diagram for (1) through (5))

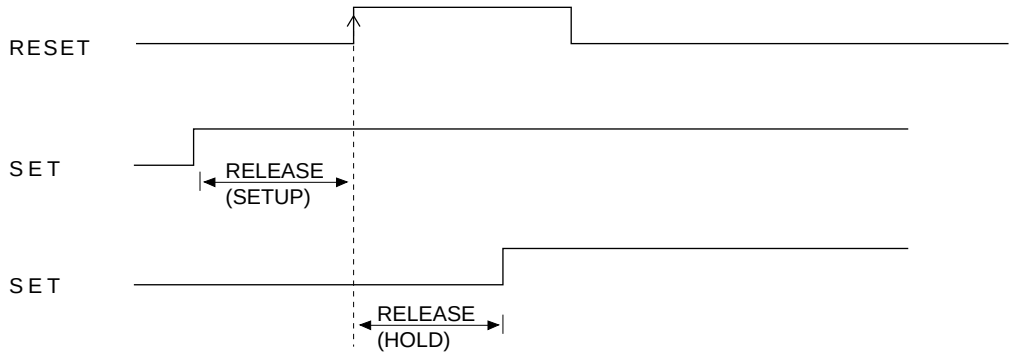


Figure 5-5 Timing Waveform Diagram 2 (explanation diagram for (6) through (7))

The flip-flop setup/hold times of the S1K50000 series are listed in cell libraries in the form shown in Table 5-4 below. During actual use, please see the timing characteristics of each individual cell.

Table 5-4 Timing Characteristics of KDFSR (Reference)

Pin	Setup time (ps)	Hold time (ps)	Pulsewidth (ps)
	Typ. (V_{DD} = 3.3 V)	Typ. (V_{DD} = 3.3 V)	Typ. (V_{DD} = 3.3 V)
C(P) to D	610	291	—
C(P) to R	367	468	—
C(P) to S	415	437	—
R(P) to S(P)	643	—	—
C(P)	—	—	1022
C(N)	—	—	1031
R(N)	—	—	991
S(N)	—	—	891

Note: P = transition from 0 to 1 level or Positive pulse
N = transition from 1 to 0 level or Negative pulse

5.8 Differentiating Cell Usage

(1) Cells with names suffixed by *P, *V, *O, *X2, or *X3

These cells have enhanced drive capability compared to that of ordinary cells.

(2) Cells with names suffixed by *C or *X0

These cells have reduced drive capability compared to that of ordinary cells.

5.9 Intra-Chip Skew

Inside an LSI, due to varying transistor characteristics between lots or makes and other reasons, tpd varies even for the same type of gate. Therefore, tpd may have relative drifts between multiple signals. This is known as the “skew.” This skew may make it impossible for the setup or hold time to be met. Take this skew into consideration in the design of a circuit, to ensure a sufficient timing allowance.

The intra-chip skews in the S1K50000 series are listed in Table 5-5 below.

Table 5-5 Intra-Chip Skew

Cell	Location	Skew
Internal cell	All areas	5%
I/O cell	All areas	5%

Chapter 6 Creating Test Patterns

Upon completion of logic design, create test patterns. Not only are test patterns used for simulations to verify operation of the designed circuit, they are also used for product inspection at shipment.

To increase the quality of shipped products, note the following in the creation of a test pattern.

6.1 Testability Consideration

Because test patterns are used for product inspection at shipment, they must be created so as to allow the entire internal circuit of an LSI to be tested. If any part of the internal circuit of an LSI remains untested, that part cannot be tested at product shipment, which may result in the shipment of NG products.

Generally speaking, not all parts of the internal circuit of an LSI can be tested. This requires that testability be taken into consideration from the circuit design stage.

DC test and various other conditions required for test patterns can be set easily through the insertion of a Seiko Epson-recommended test circuit. For details, see Section 4.4, “Test Circuit for Functional Cells.”

6.2 Usable Waveform Modulation

A test pattern normally consists of sequences of 0s and 1s. They allow a delay to be inserted in the input waveform or the waveform itself to be altered during a simulation or testing using an LSI tester. The following two waveforms can be used in the creation of a test pattern:

- NRZ (Non-Return to Zero)
  This waveform is normally used for signals other than the clock. This waveform can change state once within a test rate period, making it possible to insert a delay.
- RZ (Return to Zero)
  This waveform is used primarily for the clock signal. Because this waveform can generate a positive or negative pulse within one test rate period, it aids in the efficient creation of a clock signal. It also allows a delay to be inserted, as with NRZ.

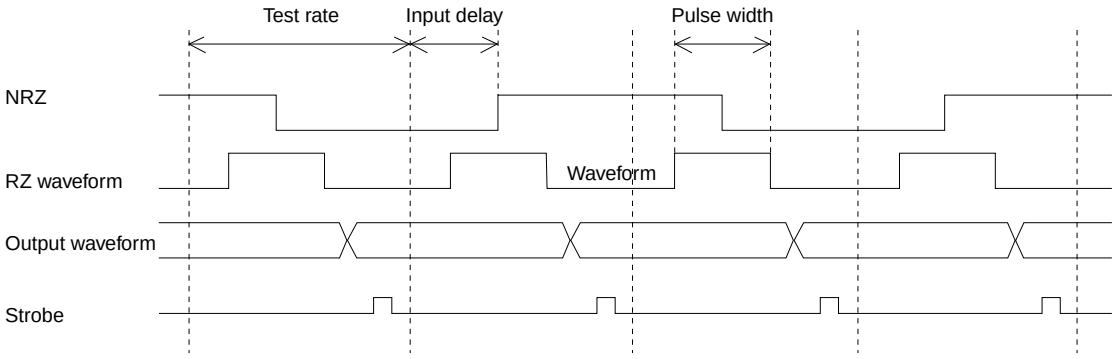


Figure 6-1 Limitations on Timing Settings

6.3 Limitations on Test Patterns

A test pattern set for the actual operating frequency is used for simulation during timing design. Because this test pattern is also used for product inspection at shipment, it must be suited for the limitations on LSI testers. Observe the limitations described below in the creation of a test pattern.

6.3.1 Test Rate and the Number of Events

The test rate must be 100 ns or more, in increments of 1 ns (recommended rate: 200 ns). It must also be defined in conformity with the limitations described in Section 6.3.5, “Strobe.” Furthermore, LSI testers are subject to limitations on the number of events, which must also be satisfied.

Number of events per test pattern	:	Up to 256K
Number of test patterns	:	Up to 30
Total number of events in test patterns	:	Up to 1M

6.3.2 Input Delay

(a) Range of input delay
0 ns ≤ input-delay value < strobe point
Define the input delay within the above range in increments of 1 ns. For the limitations on strobe points, see Section 6.3.5, “Strobe.”

(b) Phase difference in input delay
3 ns or more

(c) Types of input delays
Within eight types in one test pattern. A 0-ns delay is treated as one type. A delay value in an RZ waveform and the same delay value in an NRZ waveform are treated as different types. A delay value and the same delay value within an RZ waveform or NRZ waveform are treated as the same type.

6.3.3 Pulse Width

The pulse width of an RZ waveform must be 15 ns or more.

6.3.4 Input-Waveform Format

The input waveform can take on the value 0, 1, P, or N. P and N represent pulse inputs in the RZ waveform. In addition, P and N can only take on a combination of values, such as (0, P) or (1, N), and no other combinations for the same pin in one test pattern.
For bidirectional pins, an RZ waveform can only be entered in cases in which the output state is nonexistent. These pins are handled in the same way as for input pins.

6.3.5 Strobe

The strobe-related limitations are as follows:

(a) Only one type of strobe can be defined in each test pattern.

(b) The minimum value of a strobe must be such that, under all conditions, the strobe remains active for 30 ns or more after all output signals have had their state changed by an applied input signal.

(c) Make sure the maximum value of a strobe is smaller than (test rate – 15 ns).

(d) Set a strobe in increments of 1 ns.

6.4 Precautions Regarding DC Test

Not only are test patterns used for function tests, they also are used for DC tests in which the output voltage is measured. In the creation of a test pattern, make sure the DC test specified below can be performed.

A DC test is performed in order to verify the DC parameters of an LSI. Therefore, the measured pins cannot change state in a measurement event following strobe input.

The following are the items of DC parameters to be measured:

(a) Output-characteristic test (V_{OH}, V_{OL})

Measure the current drive capability of an output buffer. After setting the measured pins to the intended output level, measure the value of a voltage drop that occurs when a current load stipulated in the specification is applied.

In order for an output-characteristic test to be performed, the test pattern must have all states in which the measured pins can operate. In addition, said states cannot change in a measurement event, even when the test rate is extended to infinity.

(b) Quiescent-current test (I_{DDS})

“Quiescent current” refers to a leakage current that flows in the LSI in which inputs are in a steady state. Because the amount of this current is generally very small, measurements must be made under conditions in which no currents other than the leakage current are flowing. To this end, all of the conditions specified below must be met. In addition, events in which the quiescent current can be measured must be set at two or more locations.

(1) All input pins are in a steady state.

(2) Bidirectional pins are driven high or low, or set for output.

(3) No operating parts such as an oscillator exist in the circuit.

(4) The internal tri-state buffer (internal bus) is not left floating or is not contending for bus control.

(5) RAM, ROM, and megacells are not conducting current.

(6) Input pins with pull-up resistors are pulled high.

(7) Bidirectional pins with pull-up resistors are pulled high or are outputting a high signal.

(8) Bidirectional pins with pull-down resistors are set for input or are outputting a low signal.

(c) Input-current test

Measure the input-related parameters of an input buffer. This measurement item includes measurement of the input leakage current and pull-up/pull-down currents. A test is performed for this measurement item through application of the V_{DD} or V_{SS} voltage to the measured pin and measurement of the current flowing through that pin. This means that a high or low voltage is applied to the measured pin during measurement. If this test is performed by applying the V_{DD} (high) voltage to the measured pin while it is held low, the measured pin changes state from low to high, which may cause the LSI to operate unexpectedly.

For measurement during the input-current test, in an event of the test pattern in which the measured pin input is driven high, apply the V_{DD} voltage to the pin. In an event in which the measured pin is held low, apply the V_{SS} voltage to the pin. Unless the test pattern has these states for the measured pin, this test cannot be performed.

The input-current test is further classified into the following categories:

(1) Input-leakage-current test (I_{IH}, I_{IL})
Measure the input current-related parameters of an input buffer that does not have a pull-up or pull-down resistor attached.
The current that flows through the input buffer when a high voltage is applied is referred to as "I_{IH}," and is guaranteed by the maximum current value. For this test to be performed, the test pattern must have an event in which the measured pin has a high signal entered. If the measured pin is a bidirectional pin, it must be set for input, with a high signal entered.
The current that flows through the input buffer when a low voltage is applied is referred to as "I_{IL}," and is guaranteed by the maximum current value. For this test to be performed, the test pattern must have an event in which the measured pin has a low signal entered. If the measured pin is a bidirectional pin, it must be set for input, with a low signal entered.

(2) Pull-up-current test (I_{PU})
Measure the current that flows through the input buffer with a pull-up resistor attached when a low voltage is applied to it. For this test to be performed, the test pattern must have an event in which the measured pin has a low signal entered. If the measured pin is a bidirectional pin, it must be set for input, with a low signal entered.

(3) Pull-down-current test (I_{PD})
Measure the current that flows through the input buffer with a pull-down resistor attached when a high voltage is applied to it. For this test to be performed, the test pattern must have an event in which the measured pin has a high signal entered. If the measured pin is a bidirectional pin, it must be set for input, with a high signal entered.

(4) Off-state leakage current (I_{OZ})
Measure the leakage current that flows in an open-drain tri-state output buffer while its outputs are in the Hi-Z state. This test is actually performed by measuring the current flowing through the measured pin while in the Hi-Z state, when the V_{DD} voltage and V_{SS} voltage is applied to it, respectively. Therefore, the test pattern must have an event in which the measured pin is placed in the high-impedance state.

6.5 Precautions on Use of an Oscillator Circuit

The following shows examples of oscillator circuits (continuous and intermittent oscillation).

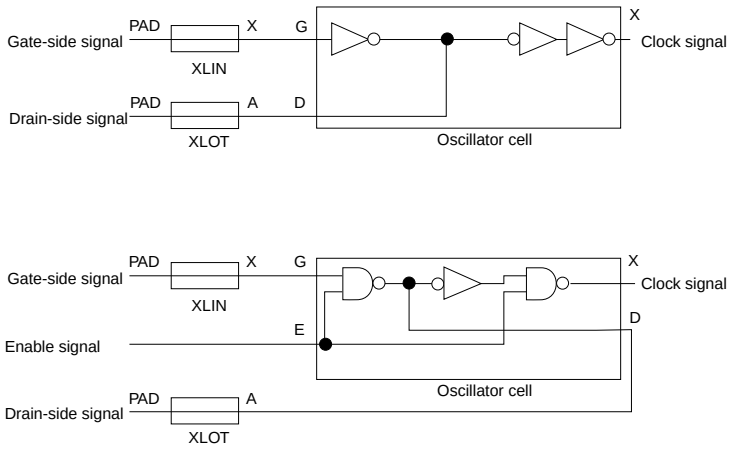


Figure 6-2 Examples of Oscillator Circuits

In general, when an oscillator circuit is used, because the oscillation inverter's drive capability is small, and because the oscillator circuit's output waveform is affected by the load of the measurement environment, the waveform conveyed to the next stage that follows the oscillator circuit is not exact.

To reproduce a simulated state using a tester, therefore, a measure is taken to apply reverse drive (by entering into the drain pin a waveform that is in phase with the signal output to the drain).

When the oscillation inverter is structured as inverter, a reverse drive signal can be produced simply by entering a signal for the drain that is opposite in phase to the signal applied to the gate. However, if comprised of a NAND gate (known as an "intermittent oscillator" or "Gated-OSC"), the signal to be entered for the drain cannot be determined based on the gate signal alone. For this reason, the reverse-drive waveform is determined based on an expected value for the drain pin.

With this method, if the input waveform is an NRZ waveform and the strobe exists at the end of the test rate period, the reverse-drive waveform can be produced using the drain pin's expected value for the input waveform directly as is. However, in the case of an RZ waveform, because the drain pin's expected value is fixed high or low whether oscillating or idle, the reverse-drive waveform cannot be determined based on the drain pin's expected value.

For an intermittently oscillating circuit, therefore, observe the following:

1. Do not use an RZ waveform for the input signal.
2. Do not change the clock signal by changing the state of the enable signal.

6.6 Regarding the AC Test

In an AC test, the length of time from when an input pin changes state until that change of state propagates to the output pin is measured. The measurement paths that have been selected by customers are used for the AC test.

6.6.1 Restrictions on Measurement Events

This test is normally performed using the method known as “binary search.” Therefore, the change points for the measured pin (any output pin that changes state) within a measurement event must be limited to one. (Measurement cannot be made of pins that are outputting an RZ waveform, nor can measurement be made when a hazard is output in the measurement event.) In addition, changes in state of the measured signal must occur in order of High → Low or Low → High (Z-related changes cannot be measured).

Other precautions include that events must be selected so as not to cause multiple output pins to change state simultaneously in a measurement event, or signal contention to occur between bidirectional pins and the LSI tester. This is due to the fact that a simultaneous change in state or signal contention causes the LSI power supply to swing, affecting the measured pin’s output waveform and making accurate measurements impossible.

6.6.2 Restrictions on AC Test Measurement Points

The measurement points in an AC test must be limited to up to four.

6.6.3 Restrictions on Delays in the Measured Path

With the AC test measurement paths, the greater the delay in the measured path, the higher the accuracy of measurement. Make sure the delay time in the measured path is set to 30 ns or more, and is equal to or less than the strobe point under maximum test simulation conditions.

6.6.4 Other Restrictions

(1) Do not specify a path from the oscillator circuit.

(2) Make sure the specified path does not pass through the internal tri-state circuit (internal bus).

(3) Do not specify a path that passes through any other bidirectional cell between the measured path’s input buffer and the output buffer.

(4) If there are two or more working voltage ranges, make sure the measured voltages in the AC test are both within one of such voltage ranges.

6.7 Restrictions on Test Patterns for Bidirectional Pins

Due to tester limitations, bidirectional pins cannot be switched between input and output modes more than twice within one event. Therefore, in the creation of a test pattern, make sure it will not use RZ waveforms to control switching between the input and output modes of a bidirectional cell.

For bidirectional pins, however, RZ waveforms can be used, provided that the pin does not have an output state and is handled in the same way as an input pin.

6.8 Precautions on Handling of the High-Impedance State

At Seiko Epson, the input pins of CMOS devices cannot be in the high-impedance state during simulation, as device operation cannot be guaranteed.

For high-impedance-related measures, I/O cells with pull-up/down resistors are available from Seiko Epson. However, for the reasons specified below, propagation delays during simulation are not taken into consideration for changes in signal state due to the pull-up/down resistors. Because exact operation cannot be simulated, for I/O cells with pull-up/down resistors (including bidirectional pins), a non-input state cannot exist in the input mode during simulation.

<Reasons that propagation delays in pull-up/down resistors are not taken into consideration>

- Because the delay fluctuates significantly due to the external load capacitance
- Because the pull-up/down resistors are used only to avoid floating gates caused by the high-impedance state

At Seiko Epson, before simulation is performed, test patterns are checked for the above using a tool. When the letter “Z,” which represents the high-impedance state, is detected in bidirectional pins (including those with N-channel open-drain output), customers are requested to correct the test pattern.

In such a case, if the letter “Z” is detected in bidirectional pins with pull-up/down resistors, customers will also be requested to correct the test pattern for the reasons described above. The same applies to bidirectional pins with open-drain output.

<Corrective measures>

When test patterns are checked, all occurrences of “Z” in bidirectional pins are indicated by the generation of an error (this does not include the “Z” that is used in the expression of tri-state and N-channel open-drain output pins).

As a means of correcting input patterns, Seiko Epson uses a utility program that automatically replaces the “Z” in said bidirectional pins with logic “1” if they have a pull-up resistor, or with logic “0” if they have a pull-down resistor.

For bidirectional pins, if a pin containing the letter “X” is set for the input mode, the “X” is propagated in simulation. In the simulation result, it is expressed as “?,” regardless of whether the pin comes with a pull-up/down resistor. Customers are requested to correct the input pattern for occurrences of “?” before Seiko Epson reexecutes simulation.

Table 6-1 Handling of Bidirectional-Pin Signals in Simulation

Input Pattern	Input/Output Mode	Simulation	Simulation Result (Output Pattern)
“X”	Input Mode	“X”	“?”
“1”, “H”	Input Mode	“1”	“1”
“0”, “L”	Input Mode	“0”	“0”

Chapter 7 Estimating Power Consumption

In CMOS LSIs, virtually no current flows through the chip while it is idle. During operation, however, they consume a certain amount of power in proportion to the operating frequency. As the power consumption increases, so does the temperature of the LSI chip. An excessively high chip temperature adversely affects the LSI quality, making it necessary to calculate the chip's power consumption in order to determine whether the power consumption falls within its rated power dissipation.

7.1 Calculating Power Consumption

Power consumption in CMOS circuits generally depends on the circuit's operating frequency, load capacitance, and power-supply voltage (this does not include special circuits such as RAM and ROM through which a steady current is flowing). Consequently, the power consumption in CMOS gate arrays can be calculated easily only if the operating frequency and load capacitance of each cell used in the circuit are known. Because the load capacitance of internal cells is difficult to calculate for each cell, the approximate calculation described below may be used.

When making this calculation, determine the power consumption in each of the input and output buffers and internal cells. The sum total of the foregoing is the chip's total power consumption.

Therefore, the total power consumption to be calculated, P_{Total}, is expressed by the equation shown below.

$$P_{Total} = P_i + P_o + P_{int}$$

P_i : power consumption in the input buffer
P_o : power consumption in the output buffer
P_{int} : power consumption in the internal cell

To calculate the power consumption in a dual-power-supply system, see Chapter 9, "Precautions on the Use of Dual Power Supplies."

(1) Power consumption in input buffers (P_i)

The power consumption in input buffers is the sum total of the signal frequencies entered in each buffer (MHz) multiplied by Kp i (µW/MHz).

$$P_i = \sum_{i=1}^{K} (Kp\,i \times f\,i)\ (W)$$

where Kp i : power factor of the input buffer (µW/MHz). See Table 7-1 below. Varies with the operating voltage.
f i : operating frequency of the i'th input buffer (MHz)

Table 7-1 Input Cell Kpi in the S1K50000 Series

V_{DD} (Typ.)	Kp i
3.3 V	6.2 µW/MHz
2.0 V	2.0 µW/MHz

(2) Power consumption of output buffers (P_o)

The power consumption of output buffers differs between DC loads (resistive loads, such as when the counterpart to be connected to is a TTL device) and AC loads (capacitive loads, such as when the counterpart to be connected to is a CMOS device).

In the case of an AC load, the power consumption can be obtained based on the load capacitance CL in the following manner:

- **AC power consumption**

$$P_{AC} = f \times C_L \times (V_{DD})^2\ (W)$$

where f : operating frequency of the output buffer (Hz)
C_L : load capacitance (F)
V_{DD} : power-supply voltage (V)

In the case of a DC load, the power consumption consists of the amount of power consumed by a DC load plus the AC power consumption.

- **DC power consumption**

$P_{DC} = P_{DCH} + P_{DCL}$

where $P_{DCH} = | I_{OH} | \times (V_{DD} - V_{OH})$ (W)
$P_{DCL} = I_{OL} \times V_{OL}$ (W)

The P_{DCH}-to-P_{DCL} ratio is determined by the duty cycle of the output signal.

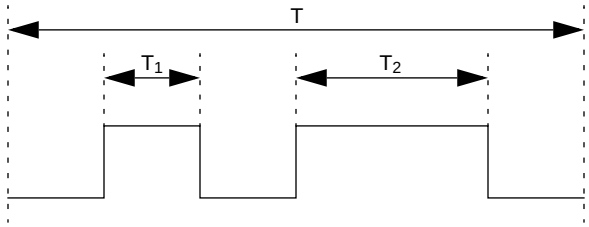


Figure 7-1 Typical Duty Cycle

Duty H = $(T_1 + T_2) / T$
Duty L = $(T - T_1 - T_2) / T$

Therefore,

$$P_{DC} = P_{DCH} + P_{DCL}$$

$$= \sum_{i=1}^{K} \{(V_{DD} - V_{OH}\,i) \times I_{OH}\,i \times \text{Duty H}\} + \sum_{i=1}^{K} \{V_{OL}\,i \times I_{OL}\,i \times \text{Duty L}\}$$

Thus, the power consumption (Po) of the output buffer is

$$P_O = \sum (P_{AC} + P_{DC})$$

$$= \sum_{i=1}^{K} \{f\,i \times C_L\,i \times (V_{DD})^2\} + \sum_{i=1}^{K} \{(V_{DD} - V_{OH}\,i) \times I_{OH}\,i \times \text{Duty H}\}$$

$$+ \sum_{i=1}^{K} \{V_{OL}\,i \times I_{OL}\,i \times \text{Duty L}\}$$

(3) Power consumption in the internal cells (P_{int})

The power consumption in the internal cells varies depending on the cell type, usage efficiency of the cell, operating frequency, and the percentage of cells that operate at that operating frequency, and is calculated as follows:

$$P_{int} = \sum_{i=1}^{K} \{N \times f\,i \times S_p\,i \times (K_{pint})\}\ (W)$$

where N : total number of BC
$f\,i$: operating frequency of the i'th cell (MHz)
$S_p\,i$: percentage of cells among all that operate at the operating frequency, $f\,i$ (approximately 20%–30% is recommended)
K_{pint} : See Table 7-2

Table 7-2 K_{pint} per BC in the S1K50000 Series

V_{DD} (Typ.)	K_{pint}
3.3 V	0.22 µW/MHz
2.0 V	0.08 µW/MHz

To provide low-power operation, Seiko Epson offers a low-power-consumption-type cell known as a "Low-Power Cell." Use of this low-power cell helps to reduce the power consumption per gate to almost half that of ordinary cells (Normal Cell), although the propagation delay time increases slightly.

When using low-power cells, halve the S1K50000-series K_{pint} value per BC listed in Table 7-2 in the calculation of the power consumption.

The low-power cells are flip-flop cells with names suffixed by "X0," and cells with names suffixed by "C."

7.2 Limitations on Power Consumption

The chip temperature of LSIs increases in proportion to their power consumption. The chip temperature of a package-mounted LSI can be calculated based on its ambient temperature Ta, the package's thermal resistance q, and power dissipation PD.

Chip temperature (Tj) = Ta + (PD × θ) (°C)

Under normal operating conditions, we recommend using LSIs at a chip temperature (Tj) of approximately 125°C or less.

The thermal resistance of each package is listed in Table 7-3. The thermal resistance of packages, as shown in Table 7-3, fluctuates significantly depending on how the chip is mounted on the board and whether the chip is heat-radiated by a fan.

Table 7-3 Thermal Resistance of Each Package (single unit in a suspended state)

ALLOY42

PKG	PIN	0 m/sec	1 m/sec	2 m/sec	3 m/sec
		θj-a	θj-a	θj-a	θj-a
QFP5	100	110(°C/W)	75	60	55
QFP5	128	110	75	60	55
QFP8	128	65	–	–	–
QFP8	208	45	–	–	–
QFP12	48	230	–	–	–
QFP13	64	170	–	–	–
QFP14	80	110	–	–	–
QFP15	100	115	50	45	35
QFP20	144	85	70	50	40
TQFP14	80	100	–	–	–
TQFP14	100	100	–	–	–
TQFP15	100	110	–	–	–

CFLGA (Board installation under the windless condition)

Package type	Customer's board size	Chip Size		
		3.82 mm × 3.82 mm	5.73 mm × 5.73 mm	9.55 mm × 9.55 mm
CFLGA424	75 mm	44.0(°C/W)	32.9	24.6
	50 mm	46.9	36.4	27.8
	30 mm	61.1	50.1	42.1
CFLGA307	75 mm	44.0	33.1	24.9
	50 mm	47.1	37.4	28.5
	30 mm	61.7	51.5	43.1
CFLGA239	75 mm	44.0	33.1	25.1
	50 mm	47.3	38.3	29.2
	30 mm	62.2	52.9	43.9
CFLGA152	75 mm	44.8	34.4	–
	50 mm	48.8	39.7	–
	30 mm	63.3	53.9	–
CFLGA104	75 mm	45.5	35.6	–
	50 mm	50.3	41.1	–
	30 mm	64.3	54.9	–

Cu-L/F

PKG	PIN	0 m/sec	1 m/sec	2 m/sec	3 m/sec
		θj-a	θj-a	θj-a	θj-a
QFP5	80	85(°C/W)	55	45	40
QFP5	100	80	55	35	30
QFP5	128	80	55	35	30
QFP8	160	45	32	25	23
QFP8	256	50	–	–	–
QFP10	304	35	20	16	–
QFP12	48	175	120	90	80
QFP13	64	130	80	55	50
QFP14	80	110	–	–	–
QFP15	100	90	–	–	–
QFP20	184	65	–	–	–
QFP21	176	55	–	–	–
QFP21	216	55	–	–	–
QFP22	208	45	35	25	23
QFP22	256	45	35	25	23
QFP23	184	40	–	–	–
QFP23	240	40	–	–	–
TQFP12	48	165	–	–	–
TQFP13	64	140	–	–	–
TQFP15	128	105	–	–	–
TQFP24	144	80	–	–	–
HQFP5	128	60	–	–	–
HQFP8	160	32	19	12	10
H2QFP8	208	34	–	–	–
H2QFP23	240	30	–	–	–
H3QFP15	128	85	–	–	–

PBGA

PKG	PIN	0 m/sec	1 m/sec	2 m/sec	3 m/sec
		θj-a	θj-a	θj-a	θj-a
PBGA	225	72(°C/W)	46	37	–
PBGA	256	53	33	25	–
PBGA	388	45	–	–	–

Chapter 8 Pin Arrangement and Simultaneous Operation

8.1 Estimating the Number of Power-Supply Pins

The necessary number of power-supply pins must be estimated based on the LSI's power consumption and the number of output buffers. In particular, the output buffers conduct a large amount of transient current when switched. This transient current tends to increase as the output buffer's drive capability increases.

Regarding the number of power-supply pins required for the LSI, the following applies with respect to current consumption.

Letting the current consumption be I_{DD} [mA], the number of power-supply pins in pairs, N_{IDD}, required for this current consumption, I_{DD}, is expressed by the equation shown below.

$N_{IDD} \geq I_{DD}/50$ (pair); 50 mA per pair of pins can be supplied

Note: The number of power-supply pins in pairs, N_{IDD}, must at least be two pairs or more.
I_{DD} is the power consumption obtained in Chapter 7 divided by the operating voltage.

For details on how to estimate the number of power-supply pins in a dual-power-supply system, see Chapter 9, "Precautions on the Use of Dual Power Supplies."

Note: If the output buffers have a DC load connected and a steadily flowing current, one or more power-supply pins must be added. For more information, contact Seiko Epson or its distributor.

8.2 Simultaneously Operating Buffers and Added Power Supply

The S1K50000-series cells have a large output drive capability of up to 12 mA. As a result, the output buffers generate a large amount of noise during operation, and an extremely large amount during simultaneous operation.

If a large number of output buffers are operated simultaneously in your application, add power supplies to prevent noise-induced malfunction, as shown in Tables 8-1-1 through 8-2-2.

Table 8-1 Number of V_{SS} Power Supplies Added for Simultaneous Operation of Output Buffers
(V_{DD} = 3.3 V)

Output drive capability (I_{OL})	Number of buffers operating simultaneously	Number of power supplies to add		
		$C_L \leq 50$ pF	$C_L \leq 100$ pF	$C_L \leq 200$ pF
6 mA	≤ 8	0	1	2
	≤ 16	1	2	3
	≤ 24	1	2	4
	≤ 32	2	3	5
12 mA	≤ 8	1	2	2
	≤ 16	2	2	3
	≤ 24	2	3	5
	≤ 32	2	4	8
PCI	≤ 8	1	2	3
	≤ 16	2	3	4
	≤ 24	3	4	5
	≤ 32	4	5	10

Table 8-2 Number of V_{SS} Power Supplies Added for Simultaneous Operation of Output Buffers
(V_{DD} = 2.0 V)

Output drive capability (I_{OL})	Number of buffers operating simultaneously	Number of power supplies to add		
		$C_L \leq 50$ pF	$C_L \leq 100$ pF	$C_L \leq 200$ pF
4 mA	≤ 8	0	1	2
	≤ 16	1	2	3
	≤ 24	1	2	4
	≤ 32	2	3	5

Table 8-3 Number of V_{DD} Power Supplies Added for Simultaneous Operation of Output Buffers

(V_{DD} = 3.3 V)

Output drive capability (I_{OH})	Number of buffers operating simultaneously	Number of power supplies to add		
		$C_L \leq 50$ pF	$C_L \leq 100$ pF	$C_L \leq 200$ pF
6 mA	≤ 8	0	1	1
	≤ 16	1	1	2
	≤ 24	1	2	3
	≤ 32	1	2	3
12 mA & PCI	≤ 8	1	2	2
	≤ 16	2	2	3
	≤ 24	2	3	3
	≤ 32	3	3	6

Table 8-4 Number of V_{DD} Power Supplies Added for Simultaneous Operation of Output Buffers

(V_{DD} = 2.0 V)

Output drive capability (I_{OH})	Number of buffers operating simultaneously	Number of power supplies to add		
		$C_L \leq 50$ pF	$C_L \leq 100$ pF	$C_L \leq 200$ pF
4 mA	≤ 8	0	1	1
	≤ 16	1	1	2
	≤ 24	1	2	3
	≤ 32	1	2	3

8.3 Precautions on Pin Arrangement

When it is decided which package to use, determine the pin arrangement on the package. For the power-supply pins and the number of usable input/output pins on each package of the S1K50000 series, refer to the designated “Pin Arrangement Table.”

When the pin arrangement is decided, send a “Pin Arrangement Table” to Seiko Epson after specifying the pin arrangement on the designated sheets. At Seiko Epson, placement & routing is performed based on the presented “Pin Arrangement Table,” so be sure to confirm that there are no errors or omissions in the table before sending it.

To obtain the designated form for the “Pin Arrangement Table,” contact Seiko Epson or its distributor.

The pin arrangement is one important specification that determines the quality of LSI. It is particularly important in terms of preventing noise-induced malfunction. This is even more important when the difficulty of identifying such noise through simulation or the like is taken into consideration.

To prevent malfunctions in customers’ LSIs due to unknown causes, we recommend carefully reading the contents hereof before creating a pin arrangement table.

8.3.1 Fixed Power-Supply Pins

Depending on the combination of cell types and the package in this series, some pins can only be used for the power supply. In addition, some pins must be fixed to V_{DD}, while others must be fixed to V_{SS}. When selecting a package, confirm this method of pin fixation by referring to the “Pin Arrangement Table.”

8.3.2 Precautions on Pin Arrangement

The pin arrangement affects the LSI’s logic functions and electrical characteristics. Furthermore, the pin arrangement is subject to limitations for reasons involving LSI assembly, the cell, or the bulk structure. Therefore, the following explains the factors requiring caution in the examination of pin arrangement. These factors include the power-supply current, separation of input and output pins, critical signals, simultaneous input/output changes in pull-up/down resistors, and large-current drivers.

(1) Power-supply currents (I_{DD} , I_{SS})

Power-supply currents (I_{DD} , I_{SS}) stipulate the rated amount of current that is allowed to flow through the power-supply pins during operation. If a current exceeding this allowable level flows, the current density in the LSI's internal power-supply wiring becomes excessively high, causing the LSI's reliability to degrade or the device itself to break down. In addition, the LSI's internal voltage increases or decreases by the amount of voltage generated by the current and wiring resistance. This results in device malfunction or adversely affects the DC and AC characteristics.

To prevent such problems, the current density and the impedance of the power-supply wiring must be reduced. This can be accomplished by estimating the power consumption of standard cells in the design of a circuit, and then preparing a sufficient number of power-supply pins so that the current flowing through each power-supply pin does not exceed the permissible value. For details, see Section 8.1, "Estimating the Number of Power-Supply Pins." In addition, make sure the power-supply pins are placed so as to be separated from each other.

Note, however, that the number of power-supply pins finally required is not simply the number of supply pins calculated above, but also includes the power-supply pins that are added as a means of preventing noise problems. For details on the number of supply pins added, see Section 8.2, "Simultaneously Operating Buffers and Added Power Supply."

(2) Noise generated by the operation of output cells

The noise generated by the operation of output cells can be broadly classified into the two types specified below. To reduce these types of noise, install as many power supplies as possible.

a) Noise generated in power-supply lines

The noise generated in power-supply lines presents a problem when multiple outputs are activated, causing the LSI's input threshold level to change, which in turn causes malfunction. The noise in power-supply lines is generated by the simultaneous operation of output cells, which causes a large current to flow through the power-supply lines.

The power-supply noise is affected by inductance components. Therefore, an LSI's equivalent circuit can be expressed as shown in Figure 8-1. In this circuit diagram, when the output changes state from high to low, a current flows from the output pin into the LSI's internal logic, with the current flowing through the equivalent inductance L2 due to the LSI's package or the like. At this time, the equivalent inductance L2 causes the voltage in the LSI's internal V_{SS} power-supply line to fluctuate. This voltage fluctuation in the V_{SS} power-supply line is the "noise" generated in power-supply lines. Because this noise is generated primarily by the equivalent inductance L2, the greater the rapidity of the power-supply current, the larger the amount of noise generated.

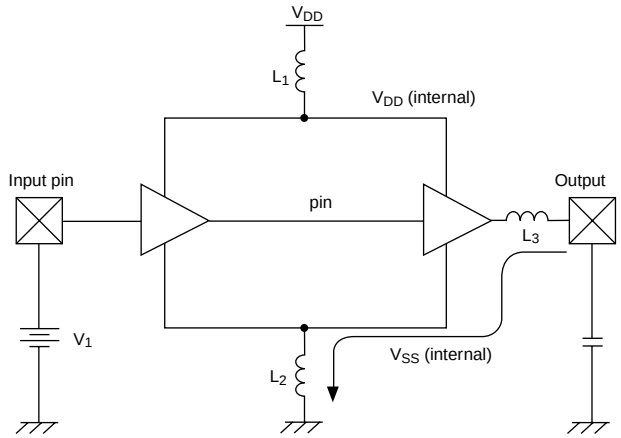


Figure 8-1 Equivalent Circuit of an LSI

b) Overshoot, undershoot, and ringing

Some types of noise, known as overshoot, undershoot, and ringing, are generated by the equivalent inductance inherent in output pins. This equivalent inductance is represented by L3 in Figure 8-1. Because inductance tends to accumulate energy, even when the output changes state to low or high, the accumulated energy generates an overshoot, undershoot, or ringing. Therefore, overshoot and undershoot are proportionate to the magnitude of flowing current, and also to the change rate of the current.

The most efficient means of reducing overshoot and undershoot is the use of output cells with a small drive capability. As the load capacitance increases, overshoot and undershoot tend to decrease. Therefore, caution is required, particularly when output cells with a large drive capability are used.

(3) Separating input and output pins

For pin arrangement, it is an important technique to separate input-pin groups from output-pin groups, as this helps to reduce the influence of noise.

Input pins and bidirectional pins set for input are susceptible to noise. It is therefore important that these pins do not coexist with output pins. To this end, place input pins, output pins, and bidirectional pins so that they are separated from each other, with power-supply pins placed between each group of pins to divide them.

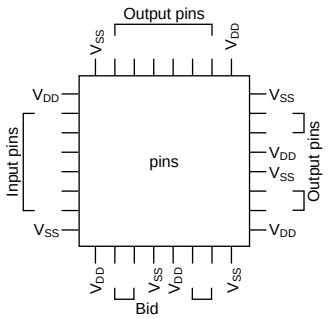


Figure 8-2 Example of the Separation of Input and Output Pins

(4) Critical signals

When placing critical signals issued from such output pins as clock-input and fast-operating output pins, observe the following precautions:

a) Place the clock and reset pins that require minimization of the influence of noise away from output pins and close to the power-supply pins (Figure 8-3).

b) Place the oscillator circuit's input/output pins (OSCIN, OSCOUT) close to each other, separated from other pins by the power-supply pins (V_{DD}, V_{SS}). Do not place output pins that are synchronous to the oscillator circuit near said pins (Figure 8-4).

c) Place fast-operating input and output pins near the middle of one side of the chip (package) (Figure 8-3).

d) If the delay time from any specific input pin to an output pin has a small margin in the customer specifications, place these input/output pins close to each other (Figure 8-3).

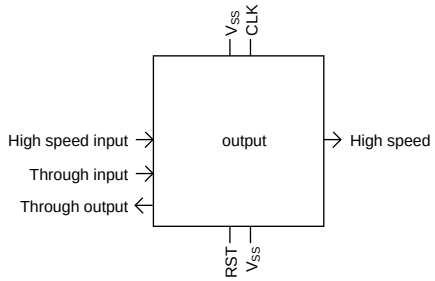


Figure 8-3 Example of the Placement of Critical Signal Pins – 1

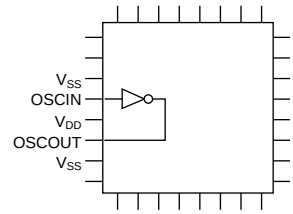


Figure 8-4 Example of the Placement of Critical Signal Pins – 2

(5) Pull-up/pull-down resistor inputs

Pull-up/pull-down resistors have rather large resistance values ranging from several 10 kohms to several 100 kohms and, due to their structure, they are dependent on the power-supply voltage.

If these resistors are used, for example, as test pins while being left open, they tend to be affected easily by power-supply noise and the like to become a cause of malfunction. Therefore, observe the following precautions when placing these resistors:

a) Place the pull-up/pull-down resistors as far from the fast input-signal pins (e.g., clock input pin) as possible (Figure 8-5).

b) Place the pull-up/pull-down resistors so that they are separated from the output-signal pins (particularly large-current output pins) (Figure 8-6).
In addition to the above pin-placement precautions, also take the following into account:

- Apply pull-up/pull-down processing to the board (PCB) as much as possible.
- Choose pull-up/pull-down resistors with resistance values as small as possible.

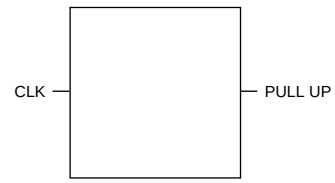


Figure 8-5 Example of the Placement of Pull-Up/Pull-Down Pins – 1

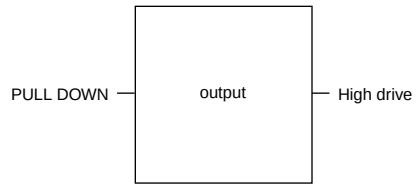


Figure 8-6 Example of the Placement of Pull-Up/Pull-Down Pins – 2

(6) Simultaneous change in outputs

If multiple pins change state simultaneously, they generate noise, causing the LSI to operate erratically. If it is necessary to operate a large number of output pins simultaneously, add power-supply pins to a group of output pins that change state simultaneously in order to prevent such a noise-induced malfunction. For details on the number of power-supply pins to add, as well as the placement method for those additional power-supply pins, see Section 8.2, “Simultaneously Operating Buffers and Added Power Supply.”

One method of reducing said noise is to insert a cell that causes a delay in front of one group of output cells. This helps to reduce the number of output pins that change state simultaneously and therefore the noise generated by a simultaneous change in state (Figure 8-8).

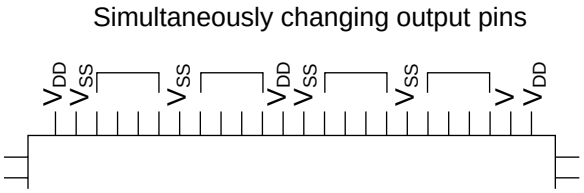


Figure 8-7 Example of the Addition of Power-Supply Pins

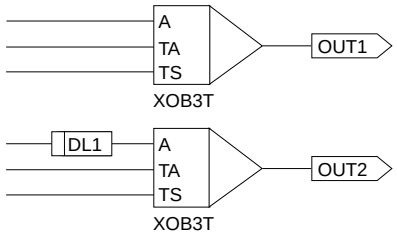


Figure 8-8 Example of the Addition of a Delay Cell

(7) Large-current drivers

When using the output of large-current drivers (I_{OL} = 12 mA, 24 mA, PCI), observe the restrictions described below in the placement of these pins.

a) Restrictions on power-supply enhancement

Because large-current drivers have a large drive capability, the amount of noise generated by the output buffers when they operate is also large. This noise may cause the LSI to operate erratically.
When using large-current drivers, place power-supply pins near their pins to secure the power supply needed for such drivers (Figure 8-9).

b) Low-noise predrivers

To reduce the amount of noise generated by the output buffers of large-current drivers during operation, special low-noise output and bidirectional buffers available from Seiko Epson may be used. For details, see Chapter 3, “Types of Input/Output Buffers and Usage Precautions.”

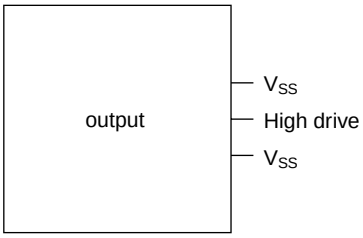


Figure 8-9 Example of Power-Supply Enhancement

(8) Other precautions

The relationship between the package pins and LSI pads is predetermined based on the combination of product types and packages in each series. Therefore, pin usage may be subject to limitations due to the package, or pin placement may be subject to limitations due to the input/output buffer types.
Consider the precautions described below before determining the pin arrangement.

a) NC (non-connected) pins

If the number of LSI pads is smaller than the number of package pins or the LSI pads cannot be assembled into the package pins, some package pins cannot be used. These pins are indicated by “**” in the pin arrangement table.

b) TAB suspended pins

The TAB suspended pins are the package pins that are connected directly to the LSI substrate. These pins are at the V_{SS} (GND) level without being supplied with power from external sources. Normally, leave these pins open when they are mounted on the board. These pins are indicated by “##” in the pin arrangement table.

8.3.3 Example of the Recommended Pin Arrangement

Pin layout is an important factor in determining whether the LSI will operate correctly. The following shows an example of pin arrangement (Figure 8-10) that takes into account all that has been explained in this chapter. Refer to this example in determining the pin arrangement of your application.

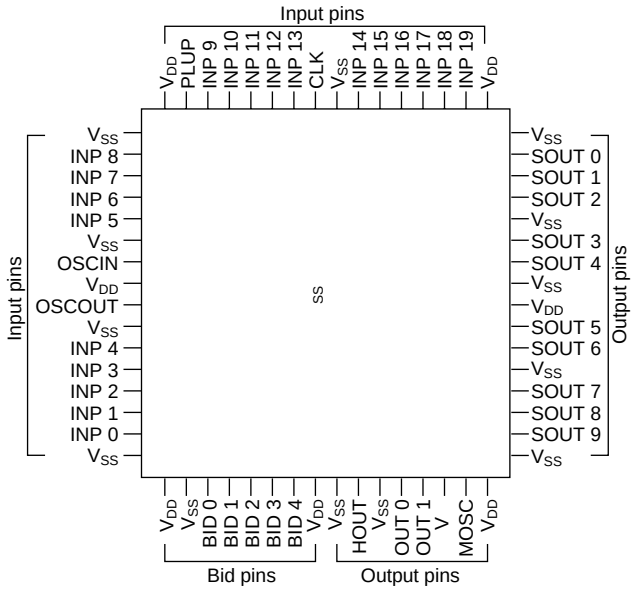


Figure 8-10 Example of Recommended Pin Arrangement

Input pins are placed on the upper and left sides of the package, while output pins that change state simultaneously are placed on the right side. Bidirectional pins and other output pins are placed on the lower side.

Table 8-5 Explanation of Example Pin Arrangement

Location	Pin Name	Explanation of Pin Name	Detailed Explanation of the Position of Each Pin
Upper Edge	PULP CLK	Input pins with pull ups Input pins for the clock	Located where the impact of noise is the least. Located near the center of the package, and near power supply pins.
Left Edge	OSCIN,OSCOUT INP0 to19	Oscillator pins Input pins	Located near the center of the package, and near power supply pins. Located with power supply pins, away from other pins.
Right-hand Edge	SOUT0 to 9	Simultaneously changing output pins	Located near power supply pins and separated from other pins with additional power supply pins.
Bottom Edge	BID0 to 4 MOSC HOUT OUT01	Bi-directional pins Oscillator monitor output pins High-drive output pins Output pins	Located near power supply pins and separated from other pins. Located separated from oscillator pins and near power supply pins. Located near power supply pins. Located near power supply pins and separated from other pins.
All Edges	V_{DD} V_{SS}	V_{DD} power supply pins V_{SS} (GND) power supply pins	

Chapter 9 Precautions on the Use of Dual Power Supplies

The S1K50000 series supports a dual-power-supply system (5.0 V and 3.3 V, or 3.3 V and 2.0 V), allowing input/output buffers to be individually interfaced with a signal of 5.0 V, 3.3 V, or 2.0 V. The internal cell area operates with a single power supply of 3.3 V or 2.0 V.

9.1 Power-Supply Accommodation

The S1K50000 series allows signals operating at voltages that differ from the internal operating voltage to be interfaced. The following two methods can be used to interface with different power-supply systems:

- For a single power supply

  For a single power supply, signals with voltages higher than the power-supply voltage can be fed into the chip through the use of N-channel open-drain buffers or Fail-Safe cells. However, signals with higher voltages than the power-supply voltage cannot be output from the chip. In such a case, the N-channel open-drain buffers and external pull-up resistors can be used in combination.

- For dual power supplies

  Signals with higher voltages than the power-supply voltage can be fed into the chip through the use of dedicated dual-power-supply input buffers. Similarly, signals with higher voltages than the power-supply voltage cannot be output from the chip through the use of dedicated dual-power-supply output buffers.

9.2 Power Supplies in a Dual-Power-Supply System

To apply two different power supplies, use two power-supply cells: HV_{DD} and LV_{DD}. Use HV_{DD} as the power supply for the HV_{DD} system input/output buffers, and LV_{DD} as the power supply for the LV_{DD} system input/output buffers and internal cells. These two power-supply voltages must always meet the following requirement:

$$HV_{DD} \geq LV_{DD}$$

If $HV_{DD} < LV_{DD}$, device operation cannot be guaranteed. The following two operating conditions are recommended:

- HV_{DD} = 5.0 V, LV_{DD} = 3.3 V
- HV_{DD} = 3.3 V, LV_{DD} = 2.0 V

S1K50000-series usage example with two power supplies

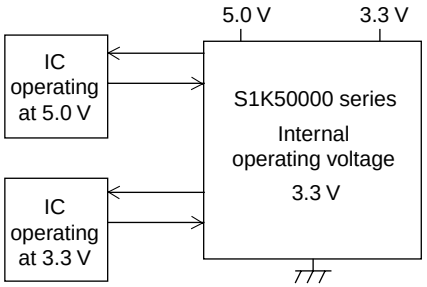


Figure 9-1 S1K50000-Series Usage Example with Two Power Supplies

9.3 Dual-Power-Supply-Type Input/Output Buffers

When operating with a dual-power-supply system, use dedicated dual-power-supply input/output buffers. Be aware that single-power-supply input/output buffers cannot be used in a dual-power-supply system. Therefore, single-power-supply input/output buffers cannot be used in combination with dedicated dual-power-supply input/output buffers. An exception is the test-use buffer (XITST1), which can be used for both dual- and single-power-supply systems.

9.3.1 LV_{DD}-System Input/Output Buffers

The LV_{DD}-system input/output buffers are available in several types, including an input buffer that accepts the input of 3.3 V (or 2.0 V) signals, an output buffer that outputs 3.3-V (or 2.0-V) amplitude signals, and a bidirectional buffer that accepts the input of 3.3-V (or 2.0-V) signals and outputs 3.3-V (or 2.0-V) amplitude signals. The LV_{DD}-system input buffers cannot accept HV_{DD}-system signals, because if such a high-voltage signal is fed in, an excessive current flows into the internal protective diode of the LV_{DD}-system buffer, causing its quality to degrade. Therefore, do not apply voltages higher than LV_{DD}.

9.3.1.1 LV_{DD}-System Input Buffers

This input buffer consists only of input cells. Several types of LV_{DD}-system input buffers are available, as listed in Tables 9-1-1 and 9-1-2.

Table 9-1-1 LV_{DD}-System Input Buffers

(LV_{DD} = 3.3 V)

Cell Name	Input Level	Fuction	With or without a pull-up/down resistor
XLIBC	LVTTL	Buffer	Without
XLIBCP*	LVTTL	Buffer	Pull-up resistor (50 kΩ, 100 kΩ)
XLIBCD*	LVTTL	Buffer	Pull-down resistor (50 kΩ, 100 kΩ)
XLIBH	LVTTL Schmitt	Buffer	Without
XLIBHP*	LVTTL Schmitt	Buffer	Pull-up resistor (50 kΩ, 100 kΩ)
XLIBHD*	LVTTL Schmitt	Buffer	Pull-down resistor (50 kΩ, 100 kΩ)
XLIBPB	PCI-3V	Buffer	Without
XLIBPBP*	PCI-3V	Buffer	Pull-up resistor (50 kΩ, 100 kΩ)
XLIBPBD*	PCI-3V	Buffer	Pull-down resistor (50 kΩ, 100 kΩ)

Note: When * value is 1 or 2, the pull-up/pull-down resistance values correspond to 1:50 kΩ, 2:100 kΩ respectively.

Table 9-1-2 LV_{DD}-System Input Buffers

(LV_{DD} = 2.0 V)

Cell Name	Input Level	Fuction	With or without a pull-up/down resistor
XLIBC	CMOS	Buffer	Without
XLIBCP*	CMOS	Buffer	Pull-up resistor (120 kΩ, 240 kΩ)
XLIBCD*	CMOS	Buffer	Pull-down resistor (120 kΩ, 240 kΩ)
XLIBH	CMOS Schmitt	Buffer	Without
XLIBHP*	CMOS Schmitt	Buffer	Pull-up resistor (120 kΩ, 240 kΩ)
XLIBHD*	CMOS Schmitt	Buffer	Pull-down resistor (120 kΩ, 240 kΩ)

Note: When * value is 1 or 2, the pull-up/pull-down resistance values correspond to 1:120 kΩ, 2:240 kΩ respectively.

9.3.1.2 LV_{DD}-System Output Buffers

The available types of S1K50000-series LV_{DD}-system output buffers are listed in Tables 9-2-1 and 9-2-2.

Table 9-2-1 LV_{DD}-System Output Buffers

(LV_{DD} = 3.3 V)

Function	I_{OL}* / I_{OH}**	Cell Name ***
Normal output	0.1 mA / -0.1 mA 1 mA / -1 mA 2 mA / -2 mA 6 mA / -6 mA 12 mA / -12 mA	XLOBST XLOBMT XLOB1T XLOB2T XLOB3T
Output for PCI	PCI-3V	XLOBPBT
Normal output for high speed	12 mA / -12 mA	XLOB3AT
Normal output for low noise	12 mA / -12 mA	XLOB3BT
3-state output	0.1 mA / -0.1 mA 1 mA / -1 mA 2 mA / -2 mA 6 mA / -6 mA 12 mA / -12 mA	XLTBST XLTBMT XLTB1T XLTB2T XLTB3T
3-state output for PCI	PCI-3V	XLTBPBT
3-state output for high speed	12 mA / -12 mA	XLTB3AT
3-state output for low noise	12 mA / -12 mA	XLTB3BT
3-state output for (Bus hold circuit)	1 mA / -1 mA 2 mA / -2 mA 6 mA / -6 mA 12 mA / -12 mA	XLTBMHT XLTB1HT XLTB2HT XLTB3HT
3-state output for high speed (Bus hold circuit)	12 mA / -12 mA	XLTB3AHT
3-state output for low noise (Bus hold circuit)	12 mA / -12 mA	XLTB3BHT

Notes * V_{OL} = 0.4 V (LV_{DD} = 3.3 V)
** V_{OH} = LV_{DD} - 0.4 V (LV_{DD} = 3.3 V)
*** In addition to the output buffers listed in Table 9-2-1, a configuration without test pins may be considered. If such a configuration is desired, contact Seiko Epson or its distributor.

Table 9-2-2 LV_{DD}-System Output Buffers

(LV_{DD} = 2.0 V)

Function	I_{OL}* / I_{OH}**	Cell Name***
Normal output	0.05 mA / -0.05 mA 0.3 mA / -0.3 mA 0.6 mA / -0.6 mA 2 mA / -2 mA 4 mA / -4 mA	XLOBST XLOBMT XLOB1T XLOB2T XLOB3T
Normal output for high speed	4 mA / -4 mA	XLOB3AT
Normal output for low noise	4 mA / -4 mA	XLOB3BT
3-state output	0.05 mA / -0.05 mA 0.3 mA / -0.3 mA 0.6 mA / -0.6 mA 2 mA / -2 mA 4 mA / -4 mA	XLTBST XLTBMT XLTB1T XLTB2T XLTB3T
3-state output for high speed	4 mA / -4 mA	XLTB3AT
3-state output for low noise	4 mA / -4 mA	XLTB3BT
3-state output for (Bus hold circuit)	0.3 mA / -0.3 mA 0.6 mA / -0.6 mA 2 mA / -2 mA 4 mA / -4 mA	XLTBMHT XLTB1HT XLTB2HT XLTB3HT
3-state output for high speed (Bus hold circuit)	4 mA / -4 mA	XLTB3AHT
3-state output for low noise (Bus hold circuit)	4 mA / -4 mA	XLTB3BHT

Notes * V_{OL} = 0.2 V (LV_{DD} = 2.0 V)
** V_{OH} = LV_{DD} - 0.2 V (LV_{DD} = 2.0 V)
*** In addition to the output buffers listed in Table 9-2-2, a configuration without test pins may be considered. If such a configuration is desired, contact Seiko Epson or its distributor.

9.3.1.3 LV_{DD}-System Bidirectional Buffers

The available types of S1K50000-series LV_{DD}-system bidirectional buffers are listed in Tables 9-3-1 and 9-3-2.

Table 9-3-1 LV_{DD}-System Bidirectional Buffers

(LV_{DD} = 3.3 V)

Input Level	Function	I_{OL}* / I_{OH} **	Cell Name
LVTTL	Bi-directional output	0.1 mA / -0.1 mA 1 mA / -1 mA 2 mA / -2 mA 6 mA / -6 mA 12 mA / -12 mA	XLBCST XLBCMT XLBC1T XLBC2T XLBC3T
	Bi-directional output for high speed	12 mA / -12 mA	XLBC3AT
	Bi-directional output for low noise	12 mA / -12 mA	XLBC3BT
PCI	Bi-directional output for PCI	PCI-3V	XLBPBT
LVTTL Schmitt	Bi-directional for low noise output	0.1 mA / -0.1 mA 1 mA / -1 mA 2 mA / -2 mA 6 mA / -6 mA 12 mA / -12 mA	XLBHST XLBHMT XLBH1T XLBH2T XLBH3T
	Bi-directional output for high speed	12 mA / -12 mA	XLBH3AT
	Bi-directional output for low noise	12 mA / -12 mA	XLBH3BT
LVTTL	Bi-directional output (Bus hold circuit)	1 mA / -1 mA 2 mA / -2 mA 6 mA / -6 mA 12 mA / -12 mA	XLBCMHT XLBC1HT XLBC2HT XLBC3HT
	Bi-directional output for high speed (Bus hold circuit)	12 mA / -12 mA	XLBC3AHT
	Bi-directional output for low noise (Bus hold circuit)	12 mA / -12 mA	XLBC3BHT
LVTTL Schmitt	Bi-directional output (Bus hold circuit)	1 mA / -1 mA 2 mA / -2 mA 6 mA / -6 mA 12 mA / -12 mA	XLBHMHT XLBH1HT XLBH2HT XLBH3HT
	Bi-directional output for high speed (Bus hold circuit)	12 mA / -12 mA	XLBH3AHT
	Bi-directional output for low noise (Bus hold circuit)	12 mA / -12 mA	XLBH3BHT

Notes * V_{OL} = 0.4 V (LV_{DD} = 3.3 V)
** V_{OH} = LV_{DD} - 0.4 V (LV_{DD} = 3.3 V)
*** In addition to the bidirectional buffers listed in Table 9-3-1, a configuration with pull-up/pull-down resistors or without test pins may be considered. If such a configuration is desired, contact Seiko Epson or its distributor.

Table 9-3-2 LV_{DD}-System Bidirectional Buffers

(LV_{DD} = 2.0 V)

Input Level	Function	I_{OL}* / I_{OH} **	Cell Name
CMOS	Bi-directional output	0.05 mA / -0.05 mA 0.3 mA / -0.3 mA 0.6 mA / -0.6 mA 2 mA / -2 mA 4 mA / -4 mA	XLBCST XLBCMT XLBC1T XLBC2T XLBC3T
	Bi-directional output for high speed	4 mA / -4 mA	XLBC3AT
	Bi-directional output for low noise	4 mA / -4 mA	XLBC3BT
CMOS Schmitt	Bi-directional for low noise output	0.05 mA / -0.05 mA 0.3 mA / -0.3 mA 0.6 mA / -0.6 mA 2 mA / -2 mA 4 mA / -4 mA	XLBHST XLBHMT XLBH1T XLBH2T XLBH3T
	Bi-directional output for high speed	4 mA / -4 mA	XLBH3AT
	Bi-directional output for low noise	4 mA / -4 mA	XLBH3BT
CMOS	Bi-directional output (Bus hold circuit)	0.3 mA / -0.3 mA 0.6 mA / -0.6 mA 2 mA / -2 mA 4 mA / -4 mA	XLBCMHT XLBC1HT XLBC2HT XLBC3HT
	Bi-directional output for high speed (Bus hold circuit)	4 mA / -4 mA	XLBC3AHT
	Bi-directional output for low noise (Bus hold circuit)	4 mA / -4 mA	XLBC3BHT
CMOS Schmitt	Bi-directional output (Bus hold circuit)	0.3 mA / -0.3 mA 0.6 mA / -0.6 mA 2 mA / -2 mA 4 mA / -4 mA	XLBHMHT XLBH1HT XLBH2HT XLBH3HT
	Bi-directional output for high speed (Bus hold circuit)	4 mA / -4 mA	XLBH3AHT
	Bi-directional output for low noise (Bus hold circuit)	4 mA / -4 mA	XLBH3BHT

Notes * V_{OL} = 0.2 V (LV_{DD} = 2.0 V)

** V_{OH} = LV_{DD} - 0.2 V (LV_{DD} = 2.0 V)

*** In addition to the bidirectional buffers listed in Table 9-3-2, a configuration with pull-up/pull-down resistors or without test pins may be considered. If such a configuration is desired, contact Seiko Epson or its distributor.

9.3.2 LV_{DD}-System Fail-Safe Cells

- Fail-Safe input buffers

Table 9-4-1 Fail-Safe Input Buffers

(LV_{DD} = 3.3 V)

Input Level	Without Resistor	Pull-down*		Pull-up*	
		50 kΩ	100 kΩ	50 kΩ	100 kΩ
LVTTL	XLIDC	XLIDCD1	XLIDCD2	XLIBBP1	XLIBBP2
LVTTL Schmitt	XLIDH	XLIDHD1	XLIDHD2	—	—

Note * The indicated resistance values are for LV_{DD} = 3.3 V.

- Fail-Safe output buffers

Table 9-4-2 Fail-Safe Output Buffers

(LV_{DD} = 3.3 V)

Function	I_{OL}*	Cell Name	
		N-channel open-drain**	Tri-state
Normal Output	2 mA	XLOD1T	XLTBF1
	6 mA	XLOD2T	XLTBF2
	12 mA	XLOD3T	—
HIGH SPEED Output	2 mA	XLOD1CT	XLTBF1C
	6 mA	XLOD2CT	XLTBF2C
	12 mA	—	XLTBF3A

Notes * V_{OL} = 0.4 V (V_{DD} = 3.3 V)

** In addition to those listed in Table 9-4-2, cells without test pins are available. If the use of such cells is desired, contact Seiko Epson or its distributor.

- Fail-Safe bidirectional buffers

1) N-channel open-drain type

Table 9-4-3 LV_{DD}-System N-Channel Open-Drain Bidirectional Buffers

(LV_{DD} = 3.3 V)

Input Level	Function	I_{OL}*	Cell Name**
LVTTL	Bi-directional output	2 mA 6 mA 12 mA	XLBDC1T XLBDC2T XLBDC3T
	Bi-directional output for high speed	2 mA 6 mA	XLBDC1CT XLBDC2CT
LVTTL Schmitt	Bi-directional output	2 mA 6 mA 12 mA	XLBDH1T XLBDH2T XLBDH3T
	Bi-directional output for high speed	2 mA 6 mA	XLBDH1CT XLBDH2CT

Notes * V_{OL} = 0.4 V (LV_{DD} = 3.3 V)

** For N-channel open-drain bidirectional buffers, in addition to those listed in Table 9-4-3, the use of bidirectional buffers without test pins may be considered. If the use of such bidirectional buffers is desired, contact Seiko Epson or its distributor.

2) Tri-state type

As with tri-state output buffers, this type of cell also cannot be tied high to 5 V by adding pull-up resistors external to the standard cell.

Table 9-4-4 Fail-Safe Cell Bidirectional Buffers

(LV_{DD} = 3.3 V)

Input Level	Drain Type	Test Function	Output Latch Function	Speed	Output Current (mA) *1	Without Resistor	Pull-down		Pull-up	
							50 kΩ	100 kΩ	50 kΩ	100 kΩ
LVTTL	Fail-Safe	N/A	N/A	Normal	–2 / 2	XLBB1	XLBB1D1	XLBB1D2	XLBB1P1	XLBB1P2
					–6 / 6	XLBB2	XLBB2D1	XLBB2D2	XLBB2P1	XLBB2P2
				HIGH-SPEED	–2 / 2	XLBB1C	XLBB1CD1	XLBB1CD2	XLBB1CP1	XLBB1CP2
					–6 / 6	XLBB2C	XLBB2CD1	XLBB2CD2	XLBB2CP1	XLBB2CP2
					–12 / 12	XLBB3A	XLBB3AD1	XLBB3AD2	XLBB3AP1	XLBB3AP2
LVTTL Schmitt	Fail-Safe	N/A	N/A	Normal	–2 / 2	XLBG1	XLBG1D1	XLBG1D2	—	—
					–6 / 6	XLBG2	XLBG2D1	XLBG2D2	—	—
				HIGH-SPEED	–2 / 2	XLBG1C	XLBG1CD1	XLBG1CD2	—	—
					–6 / 6	XLBG2C	XLBG2CD1	XLBG2CD2	—	—
					–12 / 12	XLBG3A	XLBG3AD1	XLBG3AD2	XLBG3AP1	XLBG3AP2

Notes *1: V_{OL} = 0.4 V (LV_{DD} = 3.3 V), V_{OH} = LV_{DD} - 0.4 V (LV_{DD} = 3.3 V)

9.3.3 HV_{DD}-System Input/Output Buffers

The HV_{DD}-system input/output buffers are available in several types, such as an input buffer that accepts the input of 5.0-V (or 3.3-V) signals, an output buffer that outputs 5.0-V (or 3.3-V) amplitude signals, and a bidirectional buffer that accepts the input of 5.0-V (or 3.3-V) signals and outputs 5.0-V (or 3.3-V) amplitude signals.

9.3.3.1 HV_{DD}-System Input Buffers

This input buffer consists only of input cells. The first input stage of the HV_{DD}-system input buffer is configured with an HV_{DD}-system input circuit, and the next stage is configured with an LV_{DD}-system circuit. As a result, HV_{DD}-system signals are converted into LV_{DD}-system signals before being fed into the MSI cell (internal cell area). The available types of HV_{DD}-system input buffers are listed in Tables 9-5-1 through 9-6-2.

Table 9-5-1 HV_{DD}-System Input Buffers

(HV_{DD} = 5.0 V)

Cell Name	Input Level	Fuction	With or without a pull-up/down resistor
XHIBC	CMOS	Buffer	Without
XHIBCP*	CMOS	Buffer	Pull-up resistor (60 kΩ, 120 kΩ)
XHIBCD*	CMOS	Buffer	Pull-down resistor (60 kΩ, 120 kΩ)
XHIBT*1	TTL	Buffer	Without
XHIBTP**1	TTL	Buffer	Pull-up resistor (60 kΩ, 120 kΩ)
XHIBTD**1	TTL	Buffer	Pull-down resistor (60 kΩ, 120 kΩ)
XHIBH	CMOS Schmitt	Buffer	Without
XHIBHP*	CMOS Schmitt	Buffer	Pull-up resistor (60 kΩ, 120 kΩ)
XHIBHD*	CMOS Schmitt	Buffer	Pull-down resistor (60 kΩ, 120 kΩ)
XHIBS*1	TTL Schmitt	Buffer	Without
XHIBSP**1	TTL Schmitt	Buffer	Pull-up resistor (60 kΩ, 120 kΩ)
XHIBSD**1	TTL Schmitt	Buffer	Pull-down resistor (60 kΩ, 120 kΩ)
XHIBPA*1	PCI-5V	Buffer	Without
XHIBPAP**1	PCI-5V	Buffer	Pull-up resistor (60 kΩ, 120 kΩ)
XHIBPAD**1	PCI-5V	Buffer	Pull-down resistor (60 kΩ, 120 kΩ)

Note: When * value is 1 or 2, the pull-up/pull-down resistance values correspond to 1:60 kΩ, 2:120 kΩ respectively.
*1 signifies the cell dedicated to HV_{DD} of 5.0 V.

Table 9-5-2 Input-Level Shifters

(HV_{DD} = 3.3 V)

Cell Name	Input Level	Fuction	With or without a pull-up/down resistor
XHIBC XHIBCP∗ XHIBCD∗	LVTTL LVTTL LVTTL	Buffer Buffer Buffer	Without Pull-up resistor (100 kΩ, 200 kΩ) Pull-down resistor (100 kΩ, 200 kΩ)
XHIBH XHIBHP∗ XHIBHD∗	LVTTL Schmitt LVTTL Schmitt LVTTL Schmitt	Buffer Buffer Buffer	Without Pull-up resistor (100 kΩ, 200 kΩ) Pull-down resistor (100 kΩ, 200 kΩ)
XHIBPB XHIBPBP∗ XHIBPBD∗	PCI-3V PCI-3V PCI-3V	Buffer Buffer Buffer	Without Pull-up resistor (100 kΩ, 200 kΩ) Pull-down resistor (100 kΩ, 200 kΩ)

Note: When ∗ value is 1 or 2, the pull-up/pull-down resistance values correspond to 1:100 kΩ, 2:200 kΩ respectively.

Table 9-6-1 Input-Level Shifters

(HV_{DD} = 5.0 V)

Cell Name	Input Level	Fuction	With or without a pull-up/down resistor
XHIDC XHIDCD∗	CMOS CMOS	Buffer Buffer	Without Pull-down resistor (60 kΩ, 120 kΩ)
XHIDH XHIDHD∗	CMOS Schmitt CMOS Schmitt	Buffer Buffer	Without Pull-down resistor (60 kΩ, 120 kΩ)

Note: When ∗ value is 1 or 2, the pull-up/pull-down resistance values correspond to 1:60 kΩ, 2:120 kΩ respectively.

Table 9-6-2 Input-Level Shifters

(HV_{DD} = 3.3 V)

Cell Name	Input Level	Fuction	With or without pull-up/down resistor
XHIDC XHIDCD∗	LVTTL LVTTL	Buffer Buffer	Without Pull-down resistor (100 kΩ, 200 kΩ)
XHIDH XHIDHD∗	LVTTL Schmitt LVTTL Schmitt	Buffer Buffer	Without Pull-down resistor (100 kΩ, 200 kΩ)

Note: When ∗ value is 1 or 2, the pull-up/pull-down resistance values correspond to 1:100 kΩ, 2:200 kΩ respectively.

9.3.3.2 HV_{DD}-System Output Buffers

The available types of S1K50000-series HV_{DD}-system output buffers are listed in Tables 9-7-1 through 9-8-2.

Table 9-7-1 HV_{DD}-System Output Buffers

(HV_{DD} = 5.0 V)

Function	I_{OL}* / I_{OH}**	Cell Name***
Normal output	0.1 mA / -0.1 mA 1 mA / -1 mA 3 mA / -3 mA 8 mA / -8 mA 12 mA / -12 mA 24 mA / -12 mA	XHOBST XHOBMT XHOB1T XHOB2T XHOB3T XHOB4T
Output for PCI	PCI-5V	XHOBPAT
Normal output for high speed	12 mA / -12 mA 24 mA / -12 mA	XHOB3AT XHOB4AT
Normal output for low noise	12 mA / -12 mA 24 mA / -12 mA	XHOB3BT XHOB4BT
3-state output	0.1 mA / -0.1 mA 1 mA / -1 mA 3 mA / -3 mA 8 mA / -8 mA 12 mA / -12 mA 24 mA / -12 mA	XHTBST XHTBMT XHTB1T XHTB2T XHTB3T XHTB4T
Output for PCI	PCI-5V	XHTBPAT
3-state output for high speed	12 mA / -12 mA 24 mA / -12 mA	XHTB3AT XHTB4AT
3-state output for low noise	12 mA / -12 mA 24 mA / -12 mA	XHTB3BT XHTB4BT
3-state output (Bus hold circuit)	1 mA / -1 mA 3 mA / -3 mA 8 mA / -8 mA 12 mA / -12 mA 24 mA / -12 mA	XHTBMHT XHTB1HT XHTB2HT XHTB3HT XHTB4HT
3-state output for high speed (Bus hold circuit)	12 mA / -12 mA 24 mA / -12 mA	XHTB3AHT XHTB4AHT
3-state output for low noise (Bus hold circuit)	12 mA / -12 mA 24 mA / -12 mA	XHTB3BHT XHTB4BHT

Notes * V_{OL} = 0.4 V (HV_{DD} = 5.0 V)

** V_{OH} = HV_{DD} - 0.4 V (HV_{DD} = 5.0 V)

*** For output buffers, in addition to those listed in Table 9-7-1, use of a configuration without test pins may be considered. If the use of such a configuration is desired, contact Seiko Epson or its distributor.

Table 9-7-2 HV_{DD}-System Output Buffers

(HV_{DD} = 3.3 V)

Function	I_{OL}* / I_{OH}**	Cell Name***
Normal output	0.1 mA / -0.1 mA 1 mA / -1 mA 2 mA / -2 mA 6 mA / -6 mA 12 mA / -12 mA	XHOBST XHOBMT XHOB1T XHOB2T XHOB3T
Output for PCI	PCI-3V	XHOBPBT
Normal output for high speed	12 mA / -12 mA	XHOB3AT
Normal output for low noise	12 mA / -12 mA	XHOB3BT
3-state output	0.1 mA / -0.1 mA 1 mA / -1 mA 2 mA / -2 mA 6 mA / -6 mA 12 mA / -12 mA	XHTBST XHTBMT XHTB1T XHTB2T XHTB3T
Output for PCI	PCI-3V	XHTBPBT
3-state output for high speed	12 mA / -12 mA	XHTB3AT
3-state output for low noise	12 mA / -12 mA	XHTB3BT
3-state output (Bus hold circuit)	1 mA / -1 mA 2 mA / -2 mA 6 mA / -6 mA 12 mA / -12 mA	XHTBMHT XHTB1HT XHTB2HT XHTB3HT
3-state output for high speed (Bus hold circuit)	12 mA / -12 mA	XHTB3AHT
3-state output for low noise (Bus hold circuit)	12 mA / -12 mA	XHTB3BHT

Notes * V_{OL} = 0.4 V (HV_{DD} = 3.3 V)

** V_{OH} = HV_{DD} - 0.4 V (HV_{DD} = 3.3 V)

*** For output buffers, in addition to those listed in Table 9-7-2, use of a configuration without test pins may be considered. If the use of such a configuration is desired, contact Seiko Epson or its distributor.

Table 9-8-1 HV_{DD}-System N-Channel Open-Drain Output Buffers

(HV_{DD} = 5.0 V)

Function	I_{OL}*	Cell Name***
Normal output	3 mA 8 mA 12 mA 24 mA	XHOD1T XHOD2T XHOD3T XHOD4T

Notes * V_{OL} = 0.4 V (HV_{DD} = 5.0 V)

** For N-channel open-drain output buffers, in addition to those listed in Table 9-8-1, use of a configuration without test pins may be considered. If the use of such a configuration is desired, contact Seiko Epson or its distributor.

Table 9-8-2 HV_{DD}-System N-Channel Open-Drain Output Buffers

(HV_{DD} = 3.3 V)

Function	I_{OL}*	Cell Name***
Normal output	2 mA 6 mA 12 mA	XHOD1T XHOD2T XHOD3T

Notes * V_{OL} = 0.4 V (HV_{DD} = 3.3 V)

** For N-channel open-drain output buffers, in addition to those listed in Table 9-8-2, use of a configuration without test pins may be considered. If the use of such a configuration is desired, contact Seiko Epson or its distributor.

9.3.3.3 HV_{DD}-System Bidirectional Buffers

The available types of S1K50000-series HV_{DD}-system bidirectional buffers are listed in Tables 9-9-1 through 9-10-2.

Table 9-9-1 HV_{DD}-System Bidirectional Buffers (1/2)

(HV_{DD} = 5.0 V)

Input Level	Function	I_{OL}* / I_{OH} **	Cell Name***
TTL	Bi-directional output	0.1 mA / -0.1 mA 1 mA / -1 mA 3 mA / -3 mA 8 mA / -8 mA 12 mA / -12 mA 24 mA / -12 mA	XHBTST XHBTMT XHBT1T XHBT2T XHBT3T XHBT4T
	Bi-directional output for high speed	12 mA / -12 mA 24 mA / -12 mA	XHBT3AT XHBT4AT
	Bi-directional output for low noise	12 mA / -12 mA 24 mA / -12 mA	XHBT3BT XHBT4BT
CMOS	Bi-directional output	0.1 mA / -0.1 mA 1 mA / -1 mA 3 mA / -3 mA 8 mA / -8 mA 12 mA / -12 mA 24 mA / -12 mA	XHBCST XHBCMT XHBC1T XHBC2T XHBC3T XHBC4T
	Bi-directional output for high speed	12 mA / -12 mA 24 mA / -12 mA	XHBH3AT XHBH4AT
	Bi-directional output for low noise	12 mA / -12 mA 24 mA / -12 mA	XHBC3BT XHBC4BT
PCI	Bi-directional output for PCI	PCI-5V	XHBPAT
TTL Schmitt	Bi-directional output	0.1 mA / -0.1 mA 1 mA / -1 mA 3 mA / -3 mA 8 mA / -8 mA 12 mA / -12 mA 24 mA / -12 mA	XHBSST XHBSMT XHBS1T XHBS2T XHBS3T XHBS4T
	Bi-directional output for high speed	12 mA / -12 mA 24 mA / -12 mA	XHBS3AT XHBS4AT
	Bi-directional output for low noise (Bus hold circuit)	12 mA / -12 mA 24 mA / -12 mA	XHBS3BT XHBS4BT
CMOS Schmitt	Bi-directional output	0.1 mA / -0.1 mA 1 mA / -1 mA 3 mA / -3 mA 8 mA / -8 mA 12 mA / -12 mA 24 mA / -12 mA	XHBHST XHBHMT XHBH1T XHBH2T XHBH3T XHBH4T
	Bi-directional output for high speed	12 mA / -12 mA 24 mA / -12 mA	XHBH3AT XHBH4AT
	Bi-directional output for low noise	12 mA / -12 mA 24 mA / -12 mA	XHBH3BT XHBH4BT

Notes * V_{OL} = 0.4 V (HV_{DD} = 5.0 V)

** V_{OH} = HV_{DD} - 0.4 V (HV_{DD} = 5.0 V)

*** For bidirectional buffers, in addition to those listed in Table 9-9-1, use of bidirectional buffers configured with pull-up/pull-down resistors or without test pins may be considered. If the use of a configuration without test pins is desired, contact Seiko Epson or its distributor.

Table 9-9-1 HV_{DD}-System Bidirectional Buffers (2/2)

(HV_{DD} = 5.0 V)

Input Level	Function	I_{OL}* / I_{OH} **	Cell Name***
TTL	Bi-directional output (Bus hold circuit)	1 mA / -1 mA 3 mA / -3 mA 8 mA / -8 mA 12 mA / -12 mA 24 mA / -12 mA	XHBTMHT XHBT1HT XHBT2HT XHBT3HT XHBT4HT
	Bi-directional output for high speed (Bus hold circuit)	12 mA / -12 mA 24 mA / -12 mA	XHBT3AHT XHBT4AHT
	Bi-directional output for low noise (Bus hold circuit)	12 mA / -12 mA 24 mA / -12 mA	XHBT3BHT XHBT4BHT
CMOS	Bi-directional output (Bus hold circuit)	1 mA / -1 mA 3 mA / -3 mA 8 mA / -8 mA 12 mA / -12 mA 24 mA / -12 mA	XHBCMHT XHBC1HT XHBC2HT XHBC3HT XHBC4HT
	Bi-directional output for high speed (Bus hold circuit)	12 mA / -12 mA 24 mA / -12 mA	XHBH3AHT XHBH4AHT
	Bi-directional output for low noise (Bus hold circuit)	12 mA / -12 mA 24 mA / -12 mA	XHBC3BHT XHBC4BHT
TTL Schmitt	Bi-directional output (Bus hold circuit)	1 mA / -1 mA 3 mA / -3 mA 8 mA / -8 mA 12 mA / -12 mA 24 mA / -12 mA	XHBSMHT XHBS1HT XHBS2HT XHBS3HT XHBS4HT
	Bi-directional output for high speed (Bus hold circuit)	12 mA / -12 mA 24 mA / -12 mA	XHBS3AHT XHBS4AHT
	Bi-directional output for low noise (Bus hold circuit)	12 mA / -12 mA 24 mA / -12 mA	XHBS3BHT XHBS4BHT
CMOS	Bi-directional output (Bus hold circuit)	1 mA / -1 mA 3 mA / -3 mA 8 mA / -8 mA 12 mA / -12 mA 24 mA / -12 mA	XHBHMHT XHBH1HT XHBH2HT XHBH3HT XHBH4HT
	Bi-directional output for high speed (Bus hold circuit)	12 mA / -12 mA 24 mA / -12 mA	XHBH3AHT XHBH4AHT
	Bi-directional output for low noise (Bus hold circuit)	12 mA / -12 mA 24 mA / -12 mA	XHBH3BHT XHBH4BHT

Notes * V_{OL} = 0.4 V (HV_{DD} = 5.0 V)

** V_{OH} = HV_{DD} - 0.4 V (HV_{DD} = 5.0 V)

*** For bidirectional buffers, in addition to those listed in Table 9-9-1, use of bidirectional buffers configured with pull-up/pull-down resistors or without test pins may be considered. If the use of a configuration without test pins is desired, contact Seiko Epson or its distributor.

Table 9-9-2 HV_{DD}-System Bidirectional Buffers

(HV_{DD} = 3.3 V)

Input Level	Function	I_{OL}* / I_{OH} **	Cell Name***
LVTTL	Bi-directional output	0.1 mA / -0.1 mA 1 mA / -1 mA 2 mA / -2 mA 6 mA / -6 mA 12 mA / -12 mA	XHBCST XHBCMT XHBC1T XHBC2T XHBC3T
	Bi-directional output for high speed	12 mA / -12 mA	XHBC3AT
	Bi-directional output for low noise	12 mA / -12 mA	XHBC3BT
PCI	Bi-directional output for PCI	PCI-3V	XHBPBT
LVTTL Schmitt	Bi-directional output	0.1 mA / -0.1 mA 1 mA / -1 mA 2 mA / -2 mA 6 mA / -6 mA 12 mA / -12 mA	XHBHST XHBHMT XHBH1T XHBH2T XHBH3T
	Bi-directional output for high speed	12 mA / -12 mA	XHBH3AT
	Bi-directional output for low noise	12 mA / -12 mA	XHBH3BT
LVTTL	Bi-directional output (Bus hold circuit)	1 mA / -1 mA 2 mA / -2 mA 6 mA / -6 mA 12 mA / -12 mA	XHBCMHT XHBC1HT XHBC2HT XHBC3HT
	Bi-directional output for high speed (Bus hold circuit)	12 mA / -12 mA	XHBC3AHT
	Bi-directional output for low noise (Bus hold circuit)	12 mA / -12 mA	XHBC3BHT
LVTTL Schmitt	Bi-directional output (Bus hold circuit)	1 mA / -1 mA 2 mA / -2 mA 6 mA / -6 mA 12 mA / -12 mA	XHBHMHT XHBH1HT XHBH2HT XHBH3HT
	Bi-directional output for high speed (Bus hold circuit)	12 mA / -12 mA	XHBH3AHT
	Bi-directional output for low noise (Bus hold circuit)	12 mA / -12 mA	XHBH3BHT

Notes * V_{OL} = 0.4 V (HV_{DD} = 3.3 V)

** V_{OH} = HV_{DD} - 0.4 V (HV_{DD} = 3.3 V)

*** For bidirectional buffers, in addition to those listed in Table 9-9-2, use of bidirectional buffers configured with pull-up/pull-down resistors or without test pins may be considered. If the use of a configuration without test pins is desired, contact Seiko Epson or its distributor.

9.3.4 HV_{DD}-System Fail-Safe Cells

Table 9-10-1 HV_{DD}-System N-Channel Open-Drain Bidirectional Buffers

(HV_{DD} = 5.0 V)

Input Level	Function	I_{OL}*	Cell Name**
TTL	Bi-directional output	3 mA 8 mA 12 mA 24 mA	XHBDT1T XHBDT2T XHBDT3T XHBDT4T
CMOS	Bi-directional output	3 mA 8 mA 12 mA 24 mA	XHBDC1T XHBDC2T XHBDC3T XHBDC4T
TTL Schmitt	Bi-directional output	3 mA 8 mA 12 mA 24 mA	XHBDS1T XHBDS2T XHBDS3T XHBDS4T
CMOS Schmitt	Bi-directional output	3 mA 8 mA 12 mA 24 mA	XHBDH1T XHBDH2T XHBDH3T XHBDH4T

Notes * V_{OL} = 0.4 V (HV_{DD} = 5.0 V)

** For N-channel open-drain bidirectional buffers, in addition to those listed in Table 9-10-1, use of bidirectional buffers configured without test pins may be considered. If the use of a configuration without test pins is desired, contact Seiko Epson or its distributor.

Table 9-10-2 HV_{DD}-System N-Channel Open-Drain Bidirectional Buffers

(HV_{DD} = 3.3 V)

Input Level	Function	I_{OL}*	Cell Name**
LVTTL	Bi-directional output	2 mA 6 mA 12 mA	XHBDC1T XHBDC2T XHBDC3T
LVTTL Schmitt	Bi-directional output	2 mA 6 mA 12 mA	XHBDH1T XHBDH2T XHBDH3T

Notes * V_{OL} = 0.4 V (HV_{DD} = 3.3 V)

** For N-channel open-drain bidirectional buffers, in addition to those listed in Table 9-10-2, use of bidirectional buffers configured without test pins may be considered. If the use of a configuration without test pins is desired, contact Seiko Epson or its distributor.

9.4 Calculating the Delay Time in a Dual-Power-Supply System

In a dual-power-supply system, the dispersion coefficients of delay M, listed in Table 5-1, may not be used for some types of buffers, as specified below.

The following are buffers for which the dispersion coefficients of delay M, listed in Table 5-1, cannot be used:

- HV_{DD}-system input buffers (e.g., XHIBC, XHIBH)
- HV_{DD}-system bidirectional buffers (e.g., XHBC*T, XHBH*T)

For these types of buffers, the Min., Typ., and Max values of T_0 and K are listed for your reference in the “Standard Cell S1K50000-Series MSI Cell Library.” Choose the appropriate T_0 and K values in accordance with the operating conditions, and use the selected values in calculation of the delay time.

1) Calculating delay time (Typ. value)

The delay time (Typ. value) in a dual-power-supply system is calculated in the same way as for a single-power-supply system. Because a highly accurate delay-time calculation environment is provided, please note that the delay calculations are not in agreement with those performed using the values listed in the “Standard Cell S1K50000-Series MSI Cell Library.” When calculating the delay time in input and output buffers, use the T_0 (Typ.) and K (Typ.) values suited for the respective operating voltages of the HV_{DD} and LV_{DD}-system buffers.

To calculate the delay time in the internal cell (Typ. value), use the T_0 (Typ.) and K (Typ.) values suited for the operating voltages of the LV_{DD}-system buffers.

2) Calculating the delay times (Min. and Max. values) and dispersion of delay coefficients

In the case of a single-power-supply system, the Max. and Min. values of the delay time are obtained simply by multiplying the Typ. value by the coefficient M (Table 5-1). For a dual-power-supply system, on the other hand, because the dispersion coefficient of delay differs between HV_{DD}- and LV_{DD}-system cells, first find the Max. and Min. values of the delay time in each cell. Then, total the delay time of each cell thus obtained to find the Max. and Min. values of delay time in the entire circuit.

However, for operation with a dual-power-supply system, the dispersion coefficients of delay M, listed in Table 5-1, cannot be used for some types of buffers such as XHIBC or XHBC*T. To find the Min. value of the delay time in such buffers, for example, use the Min. values of T_0 and K available in the cell library to calculate the Min. value of delay time. Similarly, to find the Max. value of the delay time, use the Max. values of T_0 and K available in the cell library to calculate the Max. value of the delay time.

9.5 Notes on Calculating Power Consumption in a Dual-Power-Supply System

To calculate the chip's power consumption in a dual-power-supply system, the power consumption must be determined separately for the HV_{DD}- and LV_{DD}-system cells.

1) Power consumption of input buffers (Pi (HV_{DD}) and Pi (LV_{DD}))

The calculation formula is the same as for a single-power-supply system. Assuming that the power consumption of the HV_{DD} system is represented by Pi (HV_{DD}), and that of the LV_{DD} system is represented by Pi (LV_{DD}):

$$Pi\ (HV_{DD}) = \sum_{i=1}^{K} (Kp\ i \times f\ i) \quad (W)$$

$$Pi\ (LV_{DD}) = \sum_{i=1}^{K} (Kp\ i \times f\ i) \quad (W)$$

The sum of Pi (HV_{DD}) and Pi (LV_{DD}) calculated from the above equations represents the power consumption of the input buffers. For the HV_{DD}-system input buffers, use the Kp i that applies to 5.0 V (or 3.3 V) and, for the LV_{DD} system, use the Kp i that applies to 3.3 V (or 2.0 V) in order to calculate the power consumption in each system. The Kp i values for the respective power-supply voltages are listed in Table 9-11 below.

Table 9-11

V_{DD} (Typ.)	Kp i
HV_{DD} = 5.0 V	17.7 µW/MHz
HV_{DD} (or LV_{DD}) = 3.3 V	6.2 µW/MHz
LV_{DD} = 2.0 V	2.0 µW/MHz

2) Power consumption of output buffers (Po (HV_{DD}) and Po (LV_{DD}))

The calculation formula is the same as for a single-power-supply system. Assuming that the power consumption of the HV_{DD} system is represented by Po (HV_{DD}), and that of the LV_{DD} system is represented by Po (LV_{DD}):

$$Po\ (HV_{DD}) = \sum\ (P_{AC} + P_{DC})$$
$$= \sum_{i=1}^{K} \{f\,i \times C_L\,i \times (HV_{DD})^2\} + \sum_{i=1}^{K} \{(HV_{DD} - V_{OH}\,i) \times |\ I_{OH}\,i\ | \times Duty\ H\}$$
$$+ \sum_{i=1}^{K} \{V_{OL}\,i \times I_{OL}\,i \times Duty\ L\}$$

$$Po\ (LV_{DD}) = \sum\ (P_{AC} + P_{DC})$$
$$= \sum_{i=1}^{K} \{f\,i \times C_L\,i \times (LV_{DD})^2\} + \sum_{i=1}^{K} \{(LV_{DD} - V_{OH}\,i) \times I_{OH}\,i \times Duty\ H\}$$
$$+ \sum_{i=1}^{K} \{V_{OL}\,i \times I_{OL}\,i \times Duty\ L\}$$

The sum of Po (HV_{DD}) and Po (LV_{DD}) calculated from the above equations represents the power consumption of the output buffers. Be aware that the V_{DD} value for the HV_{DD} system differs from that for the LV_{DD} system.

Note: The $V_{OH}\,i$ value differs between the HV_{DD} and LV_{DD} systems.

3) Power consumption of internal cells (P_{int})

The calculation formula is the same as for a single-power-supply system.

$$P_{int} = \sum_{i=1}^{K} \{(Nb \times U) \times f\,i \times Sp\,i \times K_{pint}\} \quad (W)$$

The power consumption of internal cells is obtained from the above equation. For K_{pint} in the above equation, use the K_{pint} that applies to LV_{DD}. For the K_{pint} values to use, see Table 7-2. Thus, the total amount of power consumption, P_{Total}, is obtained from the following equation:

$$P_{Total} = Pi\ (HV_{DD}) + Pi\ (LV_{DD}) + Po\ (HV_{DD}) + Po\ (LV_{DD}) + P_{int}$$

9.6 Estimating the Number of Power-Supply Pins in a Dual-Power-Supply System

Even during operation of a dual-power-supply system, the amount of current that can flow through each pair of power-supply pins (for both HV_{DD} and LV_{DD} systems) is the same as in the case of a single-power-supply system. Find the necessary number of power-supply-pin pairs separately for the HV_{DD} and LV_{DD} systems.

* Letting the current consumption in the HV_{DD} system be I_{DD} (HV_{DD}) [mA], the number of power-supply-pin pairs NI_{DD} (HV_{DD}) needed for the current consumption I_{DD} (HV_{DD}) is as follows:

  NI_{DD} (HV_{DD}) ≥ I_{DD} (HV_{DD}) / 50 (pair) : 50 mA per pair can be supplied

* Letting the current consumption in the LV_{DD} system be I_{DD} (LV_{DD}) [mA], the number of power-supply-pin pairs NI_{DD} (LV_{DD}) needed for the current consumption I_{DD} (LV_{DD}) is as follows:

  NI_{DD} (LV_{DD}) ≥ I_{DD} (LV_{DD}) / 50 (pair) : 50 mA per pair can be supplied

When calculating the number of power-supply pins here, make sure the HV_{DD} and LV_{DD} systems each have at least two power-supply-pin pairs.

Note: If the output buffers have a DC load connected and have a steadily flowing current, one or more power-supply pins must be added. For more information, contact Seiko Epson or its distributor.

When adding power-supply pins due to simultaneously changing outputs, do so separately for the HV_{DD}- and LV_{DD}-system output buffers by adding power-supply pins for each power-supply system.

For the number of power-supply pins to add, see Tables 8-1-1 through 8-2-2 for the 3.3-V or 2.0-V system, and Tables 9-12 and 9-13 for the 5.0-V system.

Table 9-12 Number of V_{SS} Power-Supply Pins to Add for Output Buffers Operating Simultaneously

(HV_{DD} = 5.0 V)

Output Drive Capability (I_{OL})	Number of Output Buffers Operating Simultaneously	Number of Power-Supply Pins (in Pairs) to Add		
		CL ≤ 50 pF	CL ≤ 100 pF	CL ≤ 200 pF
8 mA	≤ 8	0	1	2
	≤ 16	1	2	4
	≤ 24	1	3	6
	≤ 32	2	4	8
12 mA	≤ 8	1	2	3
	≤ 16	2	3	5
	≤ 24	2	5	7
	≤ 32	3	6	12
24 mA & PCI	≤ 8	2	3	4
	≤ 16	3	4	6
	≤ 24	4	6	8
	≤ 32	6	8	16

Table 9-13 Number of HV_{DD} Power-Supply Pins to Add for Output Buffers Operating Simultaneously

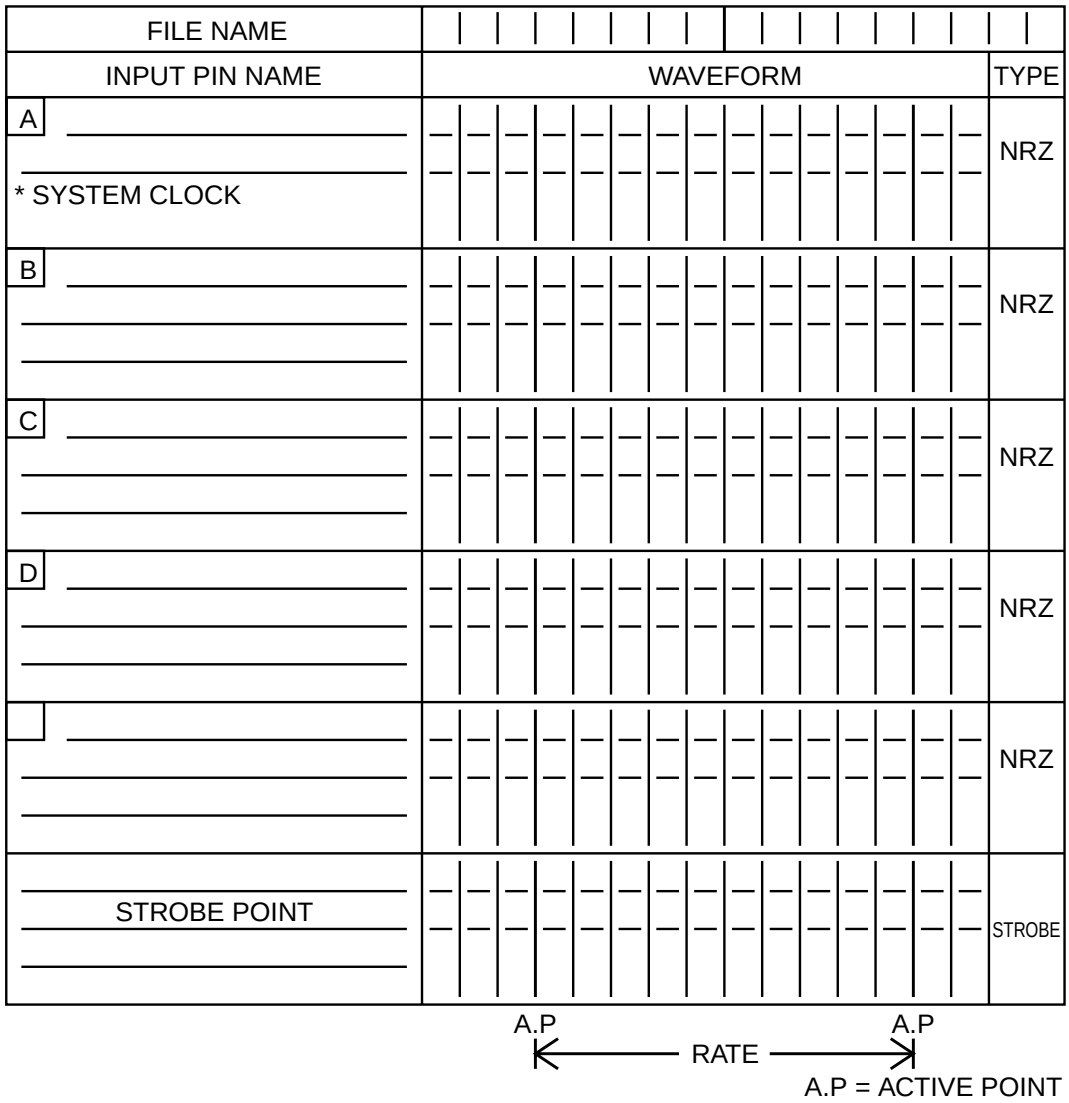
(HV_{DD} = 5.0 V)

Output Drive Capability (I_{OL})	Number of Output Buffers Operating Simultaneously	Number of Power-Supply Pins (in Pairs) to Add		
		CL ≤ 50 pF	CL ≤ 100 pF	CL ≤ 200 pF
8 mA	≤ 8	0	1	1
	≤ 16	1	1	3
	≤ 24	1	2	4
	≤ 32	1	3	5
12 mA & PCI	≤ 8	1	2	3
	≤ 16	2	3	4
	≤ 24	3	4	5
	≤ 32	4	6	10

Appendix Release Note

Simulation Input Timing Waveforms

*The about timing might change with the limitation of the measuring system including a tester.



RATE (ns)	•	(SYSTEM CLOCK)
	DELAY (ns)	COMMENT
A	•	Duty
B	•	
C	•	
D	•	
E	•	

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