

IR255SG..HCB

PHASE CONTROL THYRISTORS

■ Junction Size: Square 250 mils

■ Wafer Size: 4"

■ V_{RRM}Class: 600 to 1200 V

■ Passivation Process: Glassivated MESA

■ Reference IR Packaged Part: n. a.

Major Ratings and Characteristics

Parameters		Units	Test Conditions
V _{TM}	Maximum On-state Voltage	1.25V	$T_J = 25^{\circ}C, I_T = 25 A$
$V_{\mathrm{DRM}}/V_{\mathrm{RRM}}$	Direct and Reverse Breakdown Voltage	600 to 1200 V	$T_J = 25^{\circ}C, I_{DRM}/I_{RRM} = 100 \mu A$ (1)
I _{GT}	Max. Required DC Gate Current to Trigger	80mA	$T_J = 25^{\circ} C$, anode supply = 6 V, resistive load
V _{GT}	Max. Required DC Gate Voltage to Trigger	2 V	$T_J = 25^{\circ} C$, anode supply = 6 V, resistive load
I _H	Holding Current Range	5 to 100 mA	Anode supply = 6 V, resistive load
IL	Maximum Latching Current	300mA	Anode supply = 6 V, resistive load

⁽¹⁾ Nitrogen flow on die edge.

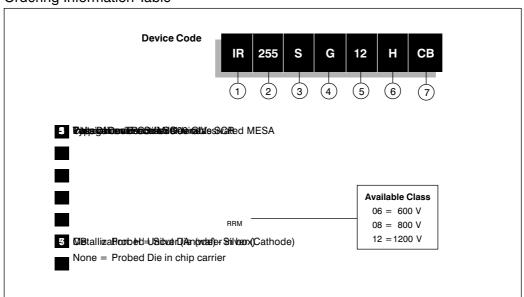
Mechanical Characteristics

Nominal Back Metal Composition, Thickness	Cr-Ni-Ag (1 KA-4 KA -6 KA)
Nominal Front Metal Composition, Thickness	Cr - Ni - Ag (1 KA - 4 KA - 6 KA)
Chip Dimensions	250x250mils (see drawing)
Wafer Diameter	100 mm, with std. <110 > flat
Wafer Thickness	$330 \mu \text{m} \pm 10 \mu \text{m}$
Maximum Width of Sawing Line	130μm
Reject Ink Dot Size	0.25 mm diameter minimum
Ink Dot Location	Seedrawing
Recommended Storage Environment	Storage in original container, in dessicated nitrogen, with no contamination

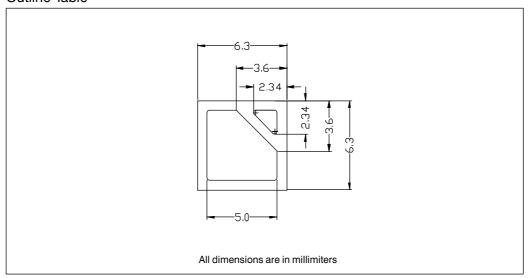
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Ordering Information Table

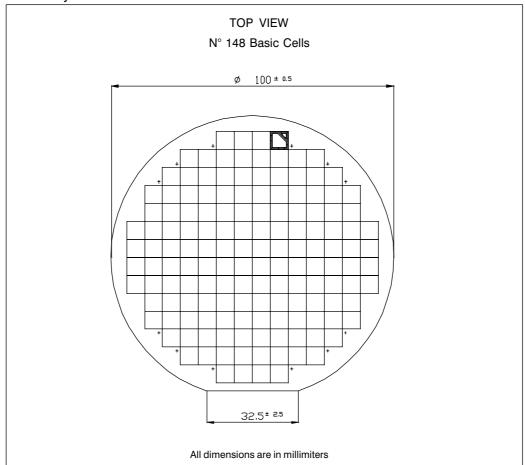


Outline Table



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Wafer Layout





Vishay

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Document Number: 99901 www.vishay.com
Revision: 12-Mar-07 1