ML610Q340/ML610340

8-bit Microcontroller with Voice Output Function

GENERAL DESCRIPTION

Equipped with an LAPIS Semiconductor original 8-bit CPU nX-U8/100, the ML610Q340/ML610340 is a high-performance 8-bit CMOS microcontroller that integrates a wide variety of peripherals such as a timer, synchronous serial port, and voice output function. The nX-U8/100 CPU is capable of executing instructions efficiently on a one-instruction-per-clock-pulse basis through parallel processing by the 3-stage pipelined architecture. The microcontroller is also equipped with a flash memory that has achieved low voltage and low power consumption (at read) equivalent to mask ROMs, so it is best suited to battery-driven applications such as cellular phones. In addition, it has an on-chip debugging function, which allows software debugging/rewriting with the LSI mounted on the board.

FEATURES

- CPU
  - 8-bit RISC CPU (CPU name: nX-U8/100)
  - Instruction repertoire: 16-bit length instructions
  - Instruction set: Transfer, arithmetic operations, comparison, logical operations, multiply/divide operations, bit manipulation, bit logical operations, jump, conditional jump, call return stack manipulation, and arithmetic shift instructions.
  - Built-in on-chip debugging function
  - Minimum instruction execution time:
    0.244 µs (@ 4.096 MHz system clock)

- Internal memory
  - ML610Q340
    Has 96-Kbyte flash memory (48K × 16-bit) built in. (including unusable 1KByte TEST area)
  - ML610340
    Has 96-Kbyte mask memory (48K × 16-bit) built in. (including unusable 1KByte TEST area)
  - Has 512-byte RAM (512 × 8-bit) built in.

- Interrupt controller
  - Non-maskable interrupt: 2 sources (1 internal source and 1 external sources)
  - Maskable interrupt: 12 sources (8 internal sources and 4 external sources)

- Time-base counter
  - Low-speed side time-base counter × 1ch
  - High-speed side time-base counter × 1ch

- Watchdog timer
  - Generates a non-maskable interrupt upon the first overflow and a system reset occurs upon the second
  - Free-running
  - Selectable overflow period: 4 types (125 ms, 500 ms, 2 sec, 8 sec)

- Timer
  - 8-bit × 2ch (16-bit configuration also enabled)

- Voice output function
  - Voice synthesis method: 4-bit ADPCM2 / 8-bit non-linear PCM / 8-bit PCM / 16-bit PCM
  - Sampling frequency: 6.4/8/10.7/12.8/16/21.3/25.6/32 kHz

- Speaker amplifier output power
  - 1W(at 5V)

- Synchronous serial port
  - Master/slave selectable
  - LSB/MSB-first selectable
  - 8-bit/16-bit length selectable

- General-purpose port
  - Input-only port × 4ch
  - Output-only port × 4ch (those as secondary functions are also included)
  - Input-output port × 4ch (those as secondary functions are also included)

- Reset
  - Resetting by the RESET_N pin
  - Resetting upon power-on detection
  - Resetting upon WDT overflow detection

- Clock
  - Low-speed side clock
    Internal frequency division (1/128 of the high-speed side clock)
  - High-speed side clock
    Crystal/ceramic oscillation (4.096 MHz), external clock

- Power management
  - HALT mode: Halts the execution of instructions issued by the CPU (the peripheral circuits continue operating)
  - STOP mode: Stops low-speed and high-speed oscillation (the CPU and the peripheral circuits stop operating)
  - Clock gear: Allows changing the frequency of the high-speed system clock by software (oscillator clock divided by 1, 2, 4, or 8)
  - Block Control Function: Power down (reset registers and stop clock supply) the circuits of unused peripherals.

- Shipment
  - 30-pin SSOP
  - High-speed side clock : Crystal/ceramic oscillation (4.096 MHz)
    Flash Memory : ML610Q340-xxxMB (blank product: ML610Q340-NNNMB)
    Mask Memory : ML610340-xxxMB

  - High-speed side clock : external clock
    Flash Memory : ML610Q340J-xxxMB (blank product: ML610Q340J-NNNMB)
    Mask Memory : ML610340J-xxxMB

    xxx: ROM code number

- Guaranteed operating range
  - Operating temperature: −40°C to +85°C
  - Operating voltage: V_{DD} = 2.2 to 5.5 V, SPV_{DD} = 2.3 to 5.5 V
    (Be sure to apply the same voltage to all the power supplies.)

BLOCK DIAGRAM

ML610Q340

Figure 1 is a block diagram of the ML610Q340.
Symbols with an asterisk "*" indicate that each of them is the secondary or tertiary function of the corresponding port.

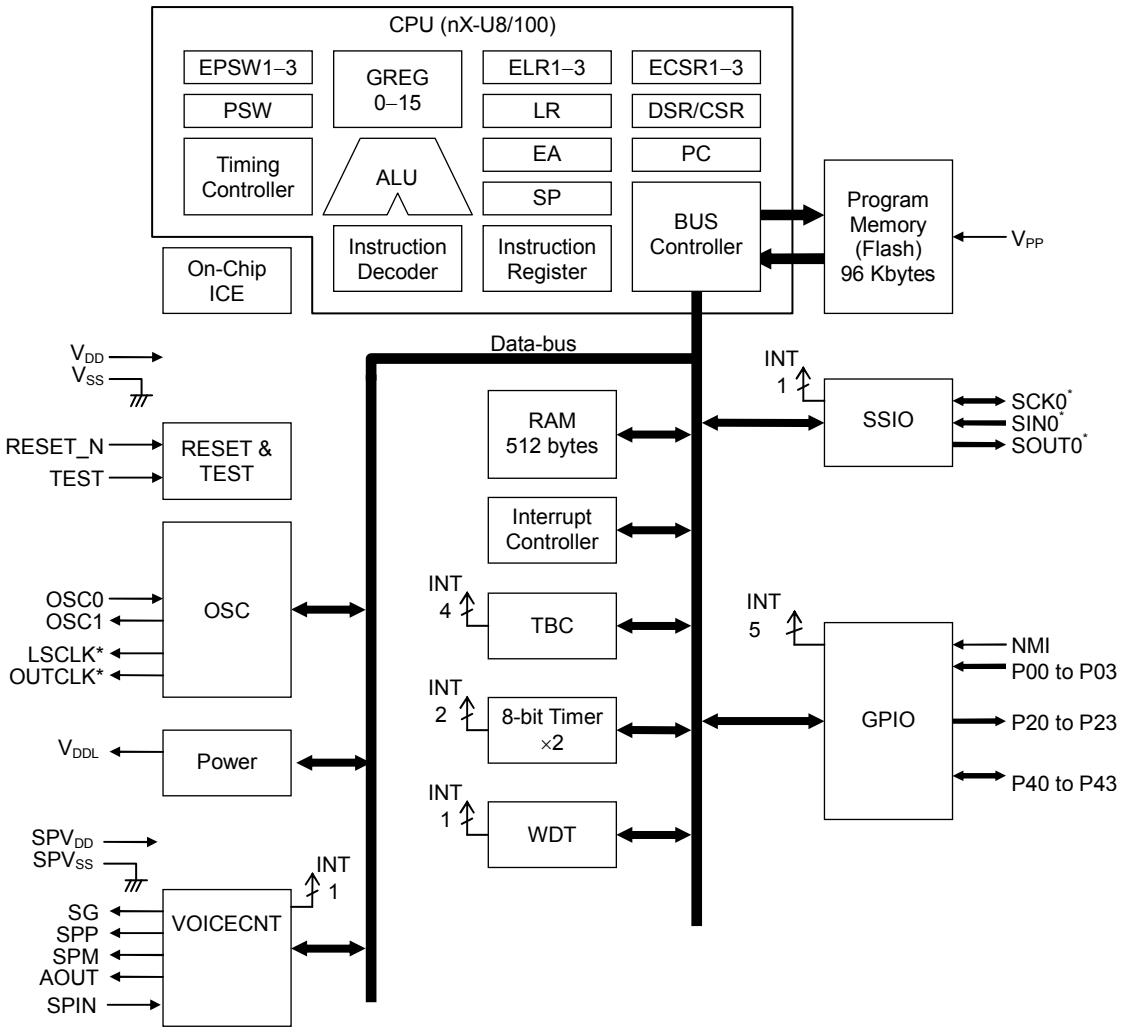


Figure 1 Block Diagram of ML610Q340

ML610340

Figure 2 is a block diagram of the ML610340.
Symbols with an asterisk "*" indicate that each of them is the secondary or tertiary function of the corresponding port.

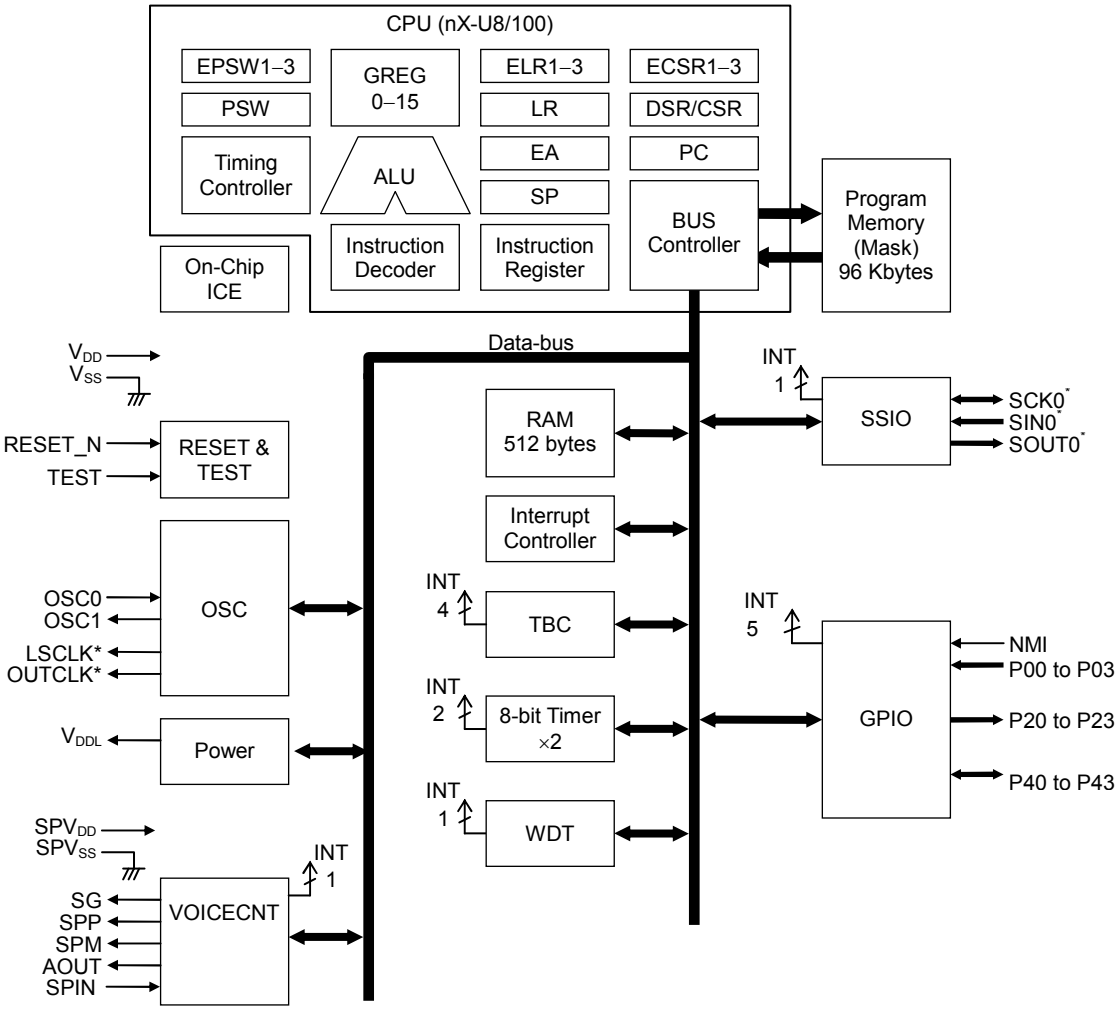
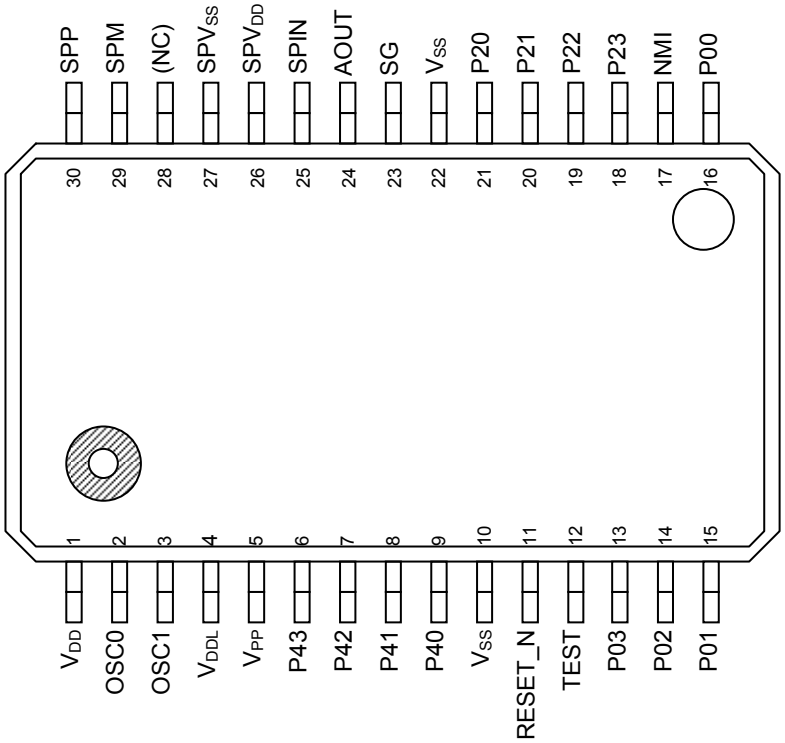


Figure 2 Block Diagram of ML610340

PIN CONFIGURATION

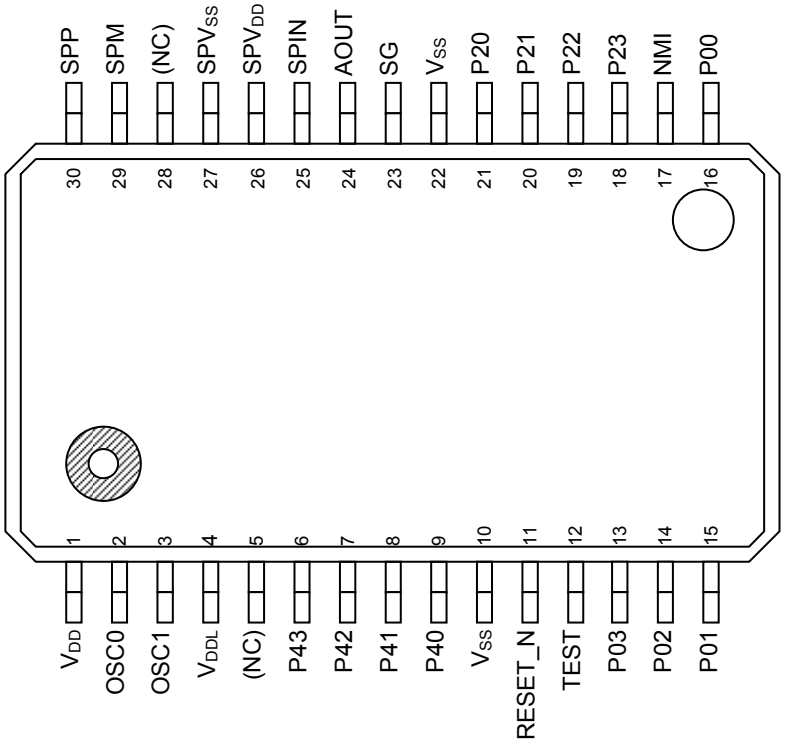
ML610Q340 SSOP package product



NC: No Connection

Figure 3 Pin Configuration of ML610Q340 Package Product

ML610340 SSOP package product



NC: No Connection

Figure 4 Pin Configuration of ML610340 Package Product

LIST OF PINS

PAD No	Primary function			Secondary function			Tertiary function		
	Pin name	I/O	Description	Pin name	I/O	Description	Pin name	I/O	Description
10,22	Vss	—	Negative power supply pin	—	—	—	—	—	—
1	V_{DD}	—	Positive power supply pin	—	—	—	—	—	—
4	V_{DDL}	—	Power supply for internal logic (internally generated)	—	—	—	—	—	—
27	SPV_{SS}	—	Negative power supply pin for built-in speaker amplifier	—	—	—	—	—	—
26	SPV_{DD}	—	Positive power supply pin for built-in speaker amplifier	—	—	—	—	—	—
5	V_{PP}(*)	—	Power supply pin for flash memory	—	—	—	—	—	—
12	TEST	I/O	Input/output pin for testing	—	—	—	—	—	—
11	RESET_N	I	Reset input pin	—	—	—	—	—	—
2	OSC0	I	Connection pin for high-speed clock oscillation	—	—	—	—	—	—
3	OSC1	O	Connection pin for high-speed clock oscillation	P11	I	Input port	—	—	—
24	AOUT	O	LINE output	—	—	—	—	—	—
25	SPIN	I	Analog input to the built-in speaker amplifier	—	—	—	—	—	—
23	SG	O	Reference power supply pin of the built-in speaker amplifier	—	—	—	—	—	—
30	SPP	O	Positive output pin of the built-in speaker amplifier	—	—	—	—	—	—
29	SPM	O	Negative output pin of the built-in speaker amplifier	—	—	—	—	—	—
17	NMI	I	Input port, non-maskable interrupt	—	—	—	—	—	—
16	P00/EXI0	I	Input port / External interrupt	—	—	—	—	—	—
15	P01/EXI1	I	Input port / External interrupt	—	—	—	—	—	—
14	P02/EXI2	I	Input port / External interrupt	—	—	—	—	—	—
13	P03/EXI3	I	Input port / External interrupt	—	—	—	—	—	—
21	P20/LED0	O	Output port / LED drive	LSCLK	O	Low-speed clock output	—	—	—
20	P21/LED1	O	Output port / LED drive	OUTCLK	O	high-speed clock output	—	—	—
19	P22/LED2	O	Output port / LED drive	—	—	—	—	—	—
18	P23/LED3	O	Output port / LED drive	—	—	—	—	—	—

PAD No	Primary function			Secondary function			Tertiary function		
	Pin name	I/O	Description	Pin name	I/O	Description	Pin name	I/O	Description
9	P40	I/O	Input/output port	—	—	—	SIN0	I	SSIO0 data input
8	P41	I/O	Input/output port	—	—	—	SCK0	I/O	SSIO0 synchronous clock input/output
7	P42	I/O	Input/output port	—	—	—	SOUT0	O	SSIO0 data output
6	P43	I/O	Input/output port	—	—	—	—	—	—

*: Applies to the ML610Q340.

PIN DESCRIPTION

Pin name	I/O	Description	Primary/ Secondary/ Tertiary	Logic
Power supply				
V_{SS}	—	Negative power supply pin	—	—
V_{DD}	—	Positive power supply pin	—	—
V_{DDL}	—	Positive power supply pin for internal logic (internally generated) Capacitors C_L(see measuring circuit 1) are connected between this pin and V_{SS}	—	—
SPV_{SS}	—	Negative power supply pin for built-in speaker amplifier	—	—
SPV_{DD}	—	Positive power supply pin for built-in speaker amplifier	—	—
V_{PP}(*)	—	Power supply pin for flash memory	—	—
Test				
TEST	I/O	Input/output pin for testing. Has a pull-down resistor built in.	—	Positive
System				
RESET_N	I	Reset input pin. When this pin is set to a “L” level, the device is placed in system reset mode and the internal circuit is initialized. If after that this pin is set to a “H” level, program execution starts. This pin has a pull-up resistor built in.	—	Negative
OSC0	I	Pins for connecting a crystal unit for high speed clock. Connect a 4.096 MHz crystal unit (see Measuring Circuit 1) to these pins. Also, connect capacitors (C_{DH} and C_{GH}) between these pins and V_{SS} as required.	—	—
OSC1	O		—	—
LSCLK	O	Low-speed clock output. This function is allocated to the secondary function of the P20 pin.	Secondary	—
OUTCLK	O	High-speed clock output. This function is allocated to the secondary function of the P21 pin.	Secondary	—
General-purpose Input port				
P00–P03	I	General-purpose input ports.	Primary	Positive
General-purpose Output port				
P20–P23	O	General-purpose output ports. Provided with a secondary function. Cannot be used as ports if their secondary function is used.	Primary	Positive
General-purpose Input/output port				
P40–P43	I/O	General-purpose input/output ports. Provided with a secondary function. Cannot be used as ports if their secondary function is used.	Primary	Positive

*Applies to the ML610Q340.

Pin name	I/O	Description	Primary/ Secondary/ Tertiary	Logic
Synchronous serial (SSIO)				
SIN0	I	Synchronous serial data input pin. Allocated to the tertiary function of the P40 pin.	Tertiary	Positive
SCK0	I/O	Synchronous serial clock input/output pin. Allocated to the tertiary function of the P41 pin.	Tertiary	—
SOUT0	O	Synchronous serial data output pin. Allocated to the tertiary function of the P42 pin.	Tertiary	Positive
External interrupt				
NMI	I	External non-maskable interrupt input pin. The interrupt occurs on both the rising and falling edges.	Primary	Positive/ Negative
EXI0–3	I	External maskable interrupt input pins. It is possible, for each bit, to specify whether the interrupt is enabled and select the interrupt edge by software. Allocated to the primary function of the P00–P03 pins.	Primary	Positive/ Negative
LED drive				
LED0–3	O	NMOS open drain pins to allow direct driving of LED. Allocated to the secondary function of the P20–P23 pins.	Primary	Positive/ Negative
Voice output function				
AOUT	O	LINE output pin. When you use built-in speaker amplifier, connect with the SPIN pin.	—	—
SPIN	I	Analog input pin of the internal speaker amplifier.	—	—
SG	O	Reference voltage output pin of the internal speaker amplifier.	—	—
SPP	O	Positive output pin of the internal speaker amplifier.	—	—
SPM	O	Negative output pin of the internal speaker amplifier.	—	—

TERMINATION OF UNUSED PINS

How to Terminate Unused Pins

Pin	Recommended pin termination
V_{PP}	Open
RESET_N	Open
TEST	Open
SPV_{DD}	V_{SS}
SPV_{SS}	V_{SS}
AOUT	Open
SPIN	Open
SG	Open
SPP	Open
SPM	Open
P00–P03	V_{DD} or V_{SS}
P20–P23	Open
P40–P43	Open

Note:
It is recommended to configure the unused input ports and input/output ports as inputs with pull-down resistors/pull-up resistors or outputs since the supply current may become excessively large if those pins are left open in the high impedance input setting.

ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings

(V_{SS} = SPV_{SS} = 0V)

Parameter	Symbol	Condition	Rating	Unit
Power supply voltage 1	V_{DD}	Ta = 25°C	–0.3 to +7.0	V
Power supply voltage 2	SPV_{DD}	Ta = 25°C	–0.3 to +7.0	V
Power supply voltage 3	V_{DDL}	Ta = 25°C	–0.3 to +3.6	V
Power supply voltage 4	V_{PP}	Ta = 25°C	–0.3 to +9.5	V
Input voltage	V_{IN}	Ta = 25°C	–0.3 to V_{DD}+0.3	V
Output voltage	V_{OUT}	Ta = 25°C	–0.3 to V_{DD}+0.3	V
Output current 1	I_{OUT1}	P4, Ta = 25°C	–12 to +11	mA
Output current 2	I_{OUT2}	P2, Ta = 25°C	–12 to +20	mA
Power dissipation	PD	Ta = 25°C	861	mW
Storage temperature	T_{STG}	—	–55 to +150	°C

Recommended Operating Conditions

(V_{SS} = SPV_{SS} = 0V)

Parameter	Symbol	Condition	Range	Unit
Operating temperature	T_{OP}	—	–40 to +85	°C
Operating voltage	V_{DD}	—	2.2 to 5.5	V
	SPV_{DD}	—	2.3 to 5.5	
Operating frequency (CPU)	f_{OP}	—	437k to 4.2M	Hz
High-speed crystal/ceramic oscillation frequency	f_{XTH}	—	4.0M, 4.096M	Hz
High-speed crystal oscillation external capacitor	C_{DH}	—	15 to 32	pF
	C_{GH}	—	15 to 32	
Capacitor externally connected to V_{DDL} pin	C_L	—	10±30%	µF
Capacitor externally connected to SG pin	C_{SG}	—	0.1±30%	µF

Flash Memory Operating Conditions

(V_{SS} = SPV_{SS} = 0V)

Parameter	Symbol	Condition	Range	Unit
Operating temperature	T_{OP}	At write/erase	0 to +40	°C
Operating voltage	V_{DD}	At write/erase	2.7 to 3.6	V
	V_{DDL}	At write/erase (*1)	2.5 to 2.75	
	V_{PP}	At write/erase (*1)	7.7 to 8.3	
Maximum rewrite count	C_{EP}	—	80	times
Data retention period	Y_{DR}	—	10	years

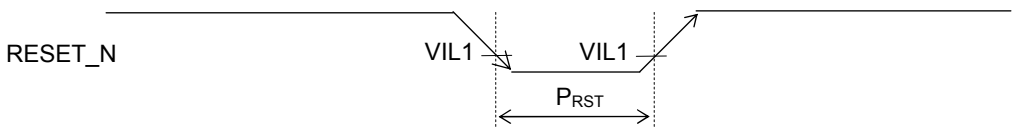
*1: When writing data to, or erasing data from, flash ROM, it is necessary to apply a voltage within the range specified above to the V_{DDL} pin.

DC Characteristics (1 of 5)

(V_{DD} = SPV_{DD} = 2.2 to 5.5V, V_{SS} = SPV_{SS} = 0V, Ta = –40 to +85°C, unless otherwise specified)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit	Measuring circuit
High-speed oscillation start time	T_{XTH}	—	—	2	20	ms	1
Reset pulse width	P_{RST}	—	100	—	—	µs	
Reset noise rejection pulse width	P_{NRST}	—	—	—	0.4		
Time from power-on reset to power-up	T_{POR}	—	—	—	10	ms	

Reset



Reset by RESET_N pin

Power-on reset

DC Characteristics (2 of 5)

(V_{DD} = SPV_{DD} = 2.3 to 5.5V, V_{SS} = SPV_{SS} = 0V,
Ta = –40 to +85°C, unless otherwise specified)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit	Measuring circuit
LINE amplifier output load resistance	R_{LA}	At 1/2V_{DD} output	10	—	—	kΩ	1
LINE amplifier output voltage range	V_{AD}	At output load	V_{DD}×1/6	—	V_{DD}×5/6	V	
SG output voltage	V_{SG}	—	0.95 × V_{DD}/2	DV_{DD}/2	1.05 × V_{DD}/2	V	
SG output resistance	R_{SG}	—	57	96	135	kΩ	
SPM, SPP output load resistance	R_{LSP}	—	8	—	—	Ω	
Speaker amplifier output power	PSPO1	SPV_{DD} = 3.3V, f = 1kHz, RSPO = 8Ω, THD ≥ 10% At SPIN Input	—	0.5	—	W	
	PSPO2	SPV_{DD} = 5.0V, f = 1kHz, RSPO = 8Ω, THD ≥ 10% At SPIN Input	—	1	—	W	
Output offset voltage between SPM and SPP with no signal present	VOF	SPV_{DD}=3.0V, SPIN – SPM gain = +6dB With a load of 8Ω	–50	—	+50	mV	

DC Characteristics (3 of 5) ML610Q340

(V_{DD} = SPV_{DD} = 2.2 to 5.5V, V_{SS} = SPV_{SS} = 0V,
Ta = –40 to +85°C, unless otherwise specified)

Parameter	Symbol	Condition		Min.	Typ.	Max.	Unit	Measuring circuit
Supply current 1	IDD1	CPU: In STOP state. Low-speed/high-speed oscillation: stopped	Ta ≤ +40°C	—	0.5	2.0	μA	1
			Ta ≤ +85°C	—	0.5	8		
Supply current 4	IDD4	CPU: Running at 4.096MHz Crystal/ceramic oscillating mode *1	V_{DD} = SPV_{DD} = 3.0V	—	1.7	4	mA	
			V_{DD} = SPV_{DD} = 5.0V	—	2.2	4		
Supply current 5	IDD5	CPU: Running at 4.096MHz Crystal/ceramic oscillating mode *1 During voice playback (no output load)	V_{DD} = SPV_{DD} = 3.0V	—	3	12		
			V_{DD} = SPV_{DD} = 5.0V	—	8	12		

*1: Use 4.096MHz Crystal Oscillator CHC49SFWB (Kyocera).

DC Characteristics ML610340

(V_{DD} = SPV_{DD} = 2.2 to 5.5V, V_{SS} = SPV_{SS} = 0V,
Ta = –40 to +85°C, unless otherwise specified)

Parameter	Symbol	Condition		Min.	Typ.	Max.	Unit	Measuring circuit
Supply current 1	IDD1	CPU: In STOP state. Low-speed/high-speed oscillation: stopped	Ta ≤ +40°C	—	0.5	2.0	μA	1
			Ta ≤ +85°C	—	0.5	8		
Supply current 4	IDD4	CPU: Running at 4.096MHz Crystal/ceramic oscillating mode *1	V_{DD} = SPV_{DD} = 3.0V	—	0.75	4	mA	
			V_{DD} = SPV_{DD} = 5.0V	—	1.5	4		
Supply current 5	IDD5	CPU: Running at 4.096MHz Crystal/ceramic oscillating mode *1 During voice playback (no output load)	V_{DD} = SPV_{DD} = 3.0V	—	3	12		
			V_{DD} = SPV_{DD} = 5.0V	—	8	12		

*1: Use 4.096MHz Crystal Oscillator CHC49SFWB (Kyocera).

DC Characteristics (4 of 5)

(V_{DD} = SPV_{DD} = 2.2 to 5.5V, V_{SS} = SPV_{SS} = 0V,
Ta = –40 to +85°C, unless otherwise specified)

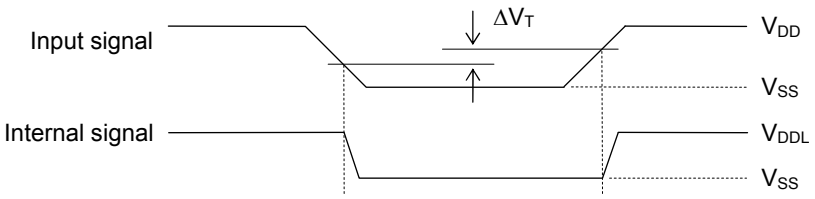
Parameter	Symbol	Condition		Min.	Typ.	Max.	Unit	Measuring circuit
Output voltage 1 (P20–P23) (P40–P43)	VOH1	IOH1 = –0.5mA		V_{DD} –0.5	—	—	V	2
	VOL1	IOL1 = +0.5mA		—	—	0.5		
Output voltage 2 (P20–P23)	VOL2	When LED drive mode is selected	IOL2 = +5mA $V_{DD} \geq$ 2.2V	—	—	0.5		
			IOL2 = +8mA $V_{DD} \geq$ 2.3V	—	—	0.5		
Output leakage current (P20–P23) (P40–P43)	IOOH	VOH = V_{DD} (in high-impedance state)		—	—	1	µA	3
	IOOL	VOL = V_{SS} (in high-impedance state)		–1	—	—		
Input current 1 (RESET_N)	IIH1	VIH1 = V_{DD}		0	—	–1	µA	4
	IIL1	VIL1 = V_{SS}		–1500	–300	–20		
Input current 2 (NMI) (P00–P03) (P40–P43)	IIH2	VIH2 = V_{DD} (when pulled down)		2	30	250		
	IIL2	VIL2 = V_{SS} (when pulled up)		–250	–30	–2		
	IIH2Z	VIH2 = V_{DD} (in high-impedance state)		—	—	1		
	IIL2Z	VIL2 = V_{SS} (in high-impedance state)		–1	—	—		
Input current 3 (TEST)	IIH3	VIH3 = V_{DD}		20	300	1500		
	IIL3	VIL3 = V_{SS}		-1	—	—		

DC Characteristics (5 of 5)

(V_{DD} = SPV_{DD} = 2.2 to 5.5V, V_{SS} = SPV_{SS} = 0V,
Ta = –40 to +85°C, unless otherwise specified)

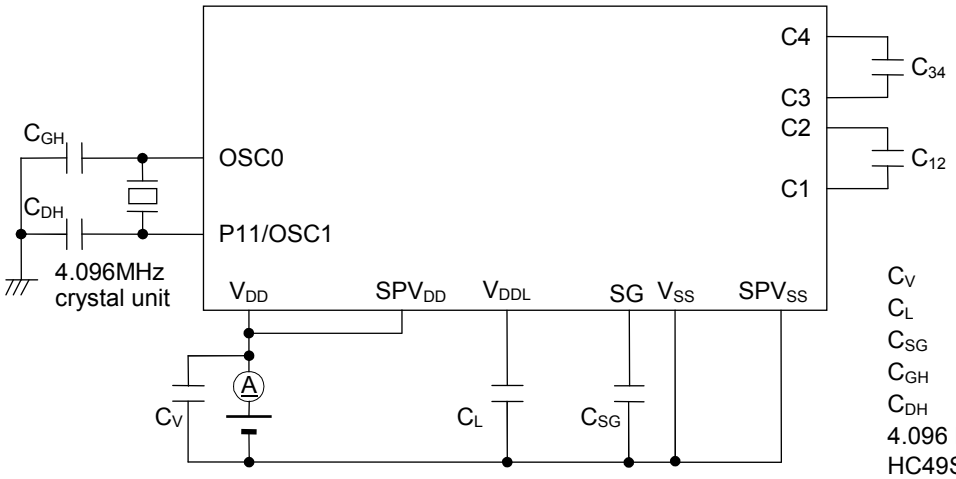
Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit	Measuring circuit
Input voltage 1 (RESET_N) (TEST) (NMI) (P00–P03) (P11) (P40–P43)	VIH1	—	0.7× V_{DD}	—	V_{DD}	V	5
	VIL1	—	0	—	0.3× V_{DD}		
Hysteresis width (RESET_N) (TEST) (NMI) (P00–P03) (P11) (P40–P43)	ΔVT	—	0.05× V_{DD}	—	0.4× V_{DD}		
Input pin capacitance (NMI) (P00–P03) (P11) (P40–P43)	CIN	f = 10kHz V_{rms} = 50mV Ta = 25°C	—	—	10	pF	—

Hysteresis Width



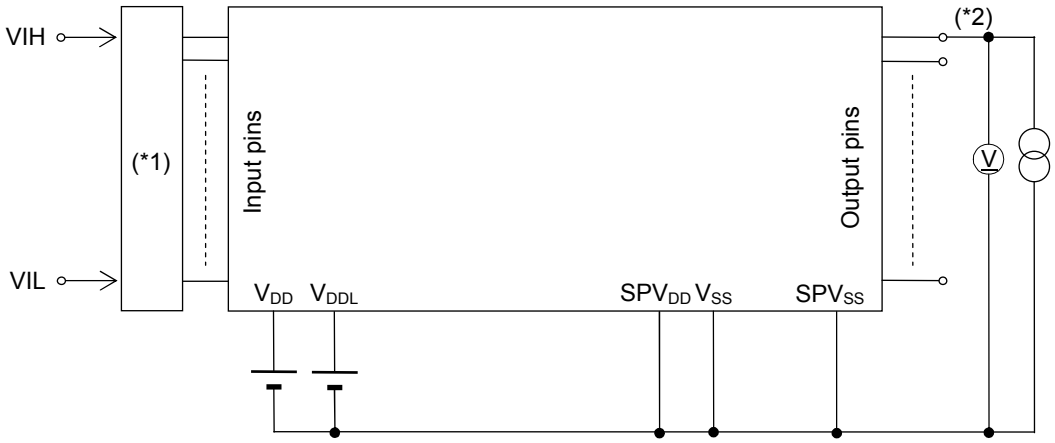
Measuring Circuits

Measuring circuit 1



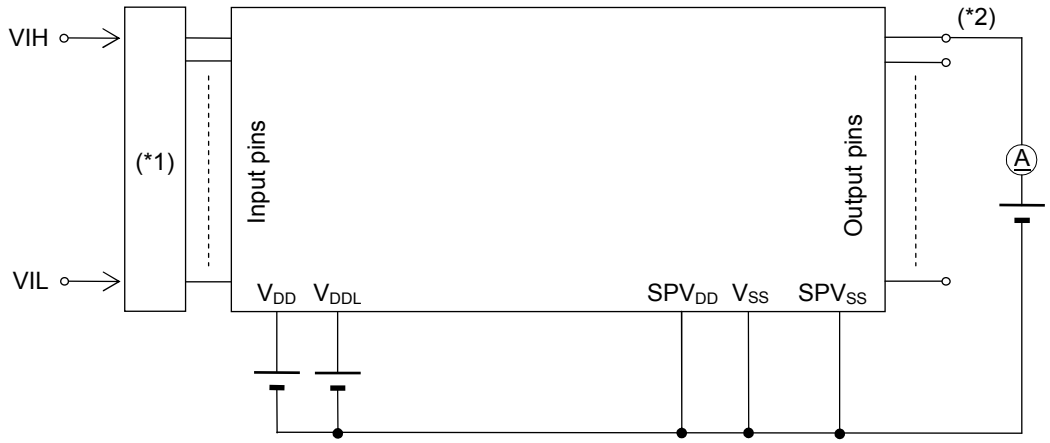
C_V : 1 µF
C_L : 10 µF
C_{SG} : 0.1 µF
C_{GH} : 24 pF
C_{DH} : 24 pF
4.096 MHz crystal unit:
HC49SFWB (Kyocera)

Measuring circuit 2



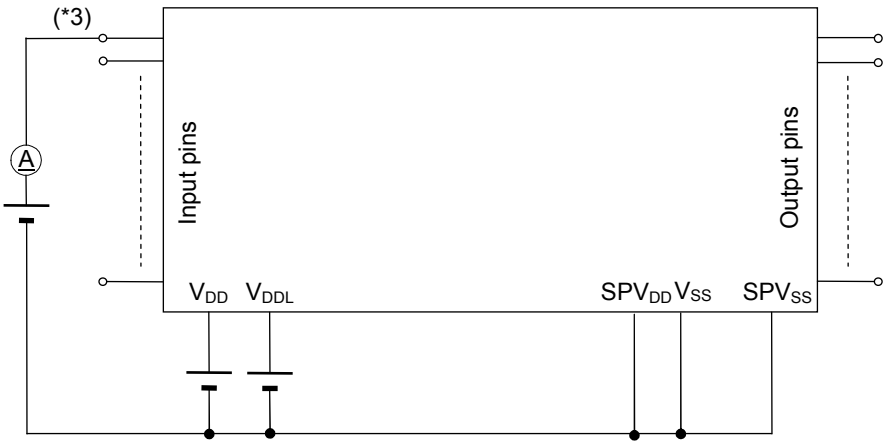
*1: Input logic circuit to determine the specified measuring conditions.
*2: Measured at the specified output pins.

Measuring circuit 3



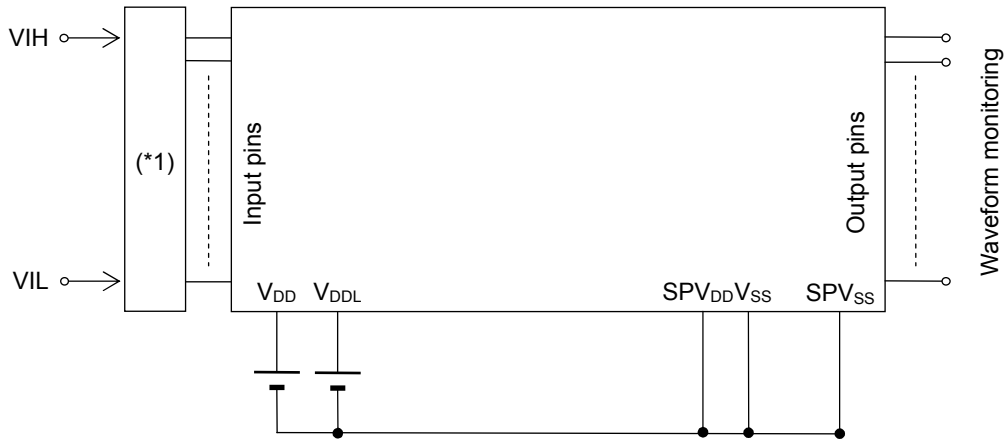
*1: Input logic circuit to determine the specified measuring conditions.
*2: Measured at the specified output pins.

Measuring circuit 4



*3: Measured at the specified input pins.

Measuring circuit 5

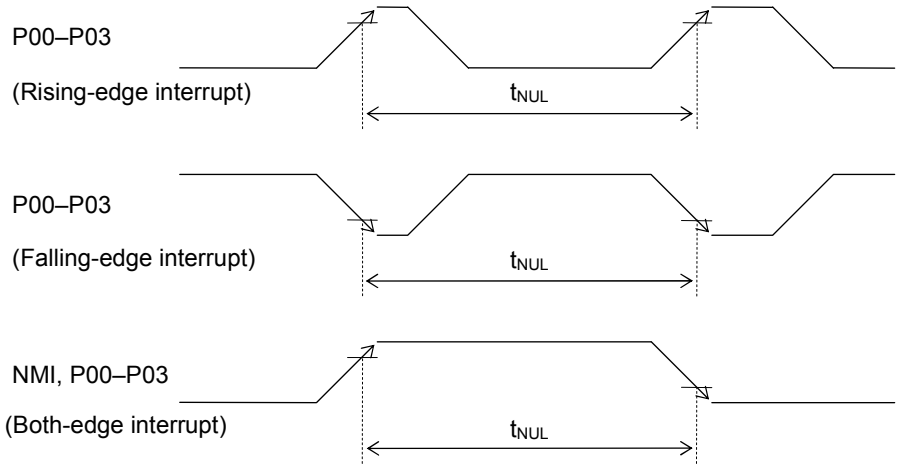


*1: Input logic circuit to determine the specified measuring conditions.

AC Characteristics (External Interrupt)

(V_{DD} = SPV_{DD} = 2.2 to 5.5V, V_{SS} = SPV_{SS} = 0V,
Ta = –40 to +85°C, unless otherwise specified)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
External interrupt disable period	T_{NUL}	Interrupt: Enabled (MIE = 1), CPU: NOP operation	2.5× sysclk	—	3.5× sysclk	µs

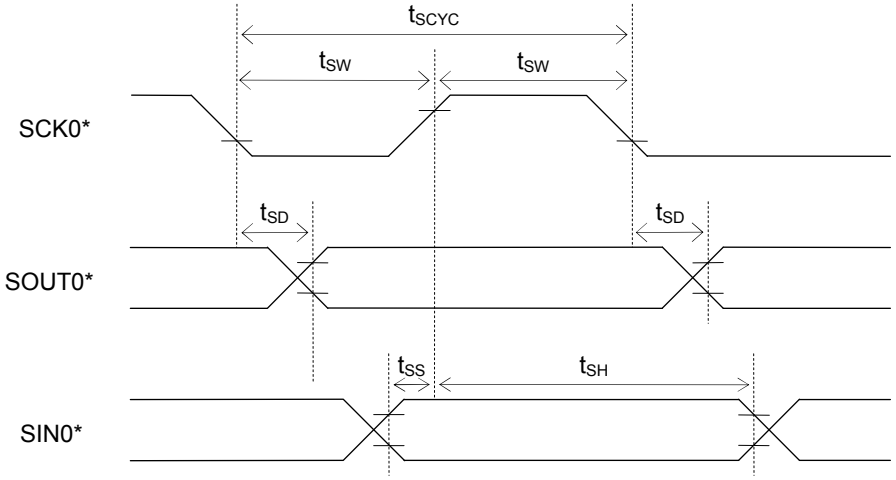


AC Characteristics (Synchronous Serial Port)

(V_{DD} = SPV_{DD} = 2.2 to 5.5V, V_{SS} = SPV_{SS} = 0V,
Ta = –40 to +85°C, unless otherwise specified)

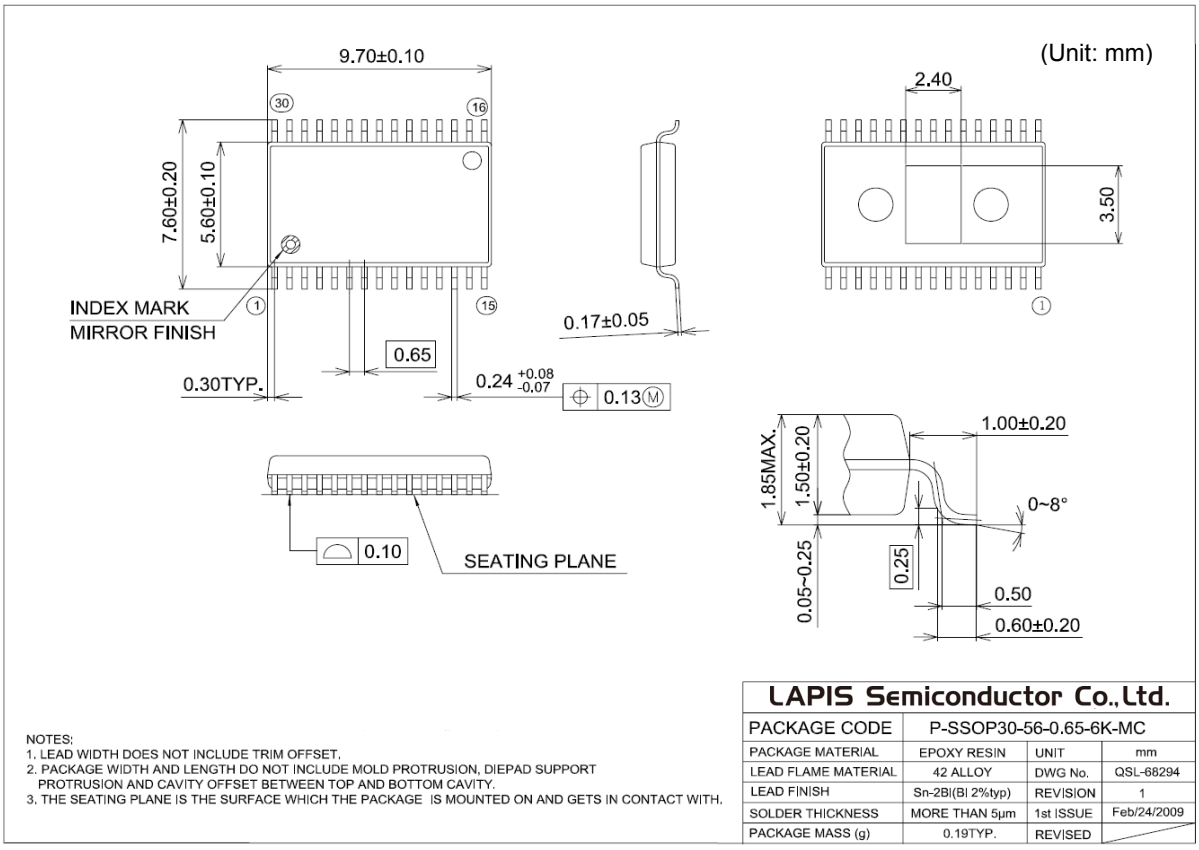
Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
SCK input cycle (slave mode)	t_{SCYC}	High-speed oscillation stopped	10	—	—	µs
		During high-speed oscillation	500	—	—	ns
SCK output cycle (master mode)	t_{SCYC}	—	—	SCK(*1)	—	sec
SCK input pulse width (slave mode)	t_{SW}	High-speed oscillation stopped	4	—	—	µs
		During high-speed oscillation	200	—	—	ns
SCK output pulse width (master mode)	t_{SW}	—	SCK(*1) ×0.4	SCK(*1) ×0.5	SCK(*1) ×0.6	sec
SOUT output delay time (slave mode)	t_{SD}	—	—	—	180	ns
SOUT output delay time (master mode)	t_{SD}	—	—	—	80	ns
SIN input setup time (slave mode)	t_{SS}	—	50	—	—	ns
SIN input hold time	t_{SH}	—	50	—	—	ns

*1: Clock period selected by S0CK3–0 of the serial port 0 mode register (SIO0MOD1)



*: Indicates the secondary function of the corresponding port.

PACKAGE DIMENSIONS



Notes for Mounting the Surface Mount Type Package

The surface mount type packages are very susceptible to heat in reflow mounting and humidity absorbed in storage. Therefore, before you perform reflow mounting, contact ROHM's responsible sales person for the product name, package name, pin number, package code and desired mounting conditions (reflow method, temperature and times).

The heat resistance (example) of this LSI is shown below. Heat resistance (θ Ja) changes with the size and the number of layers of a substrate.

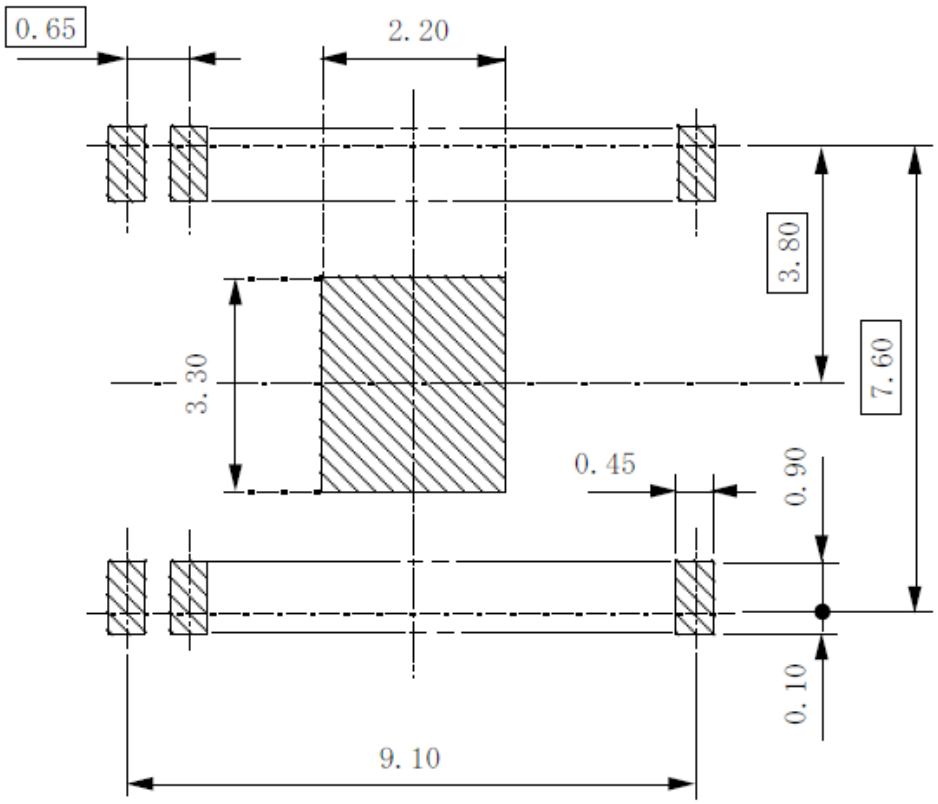
Die pad on the back of a package partial ground contact area	100%
PCB	JEDEC (W/L/t=76.2/114.5/1.6(mm))
PCB Layer	4L
Air cooling conditions	Calm(0m/sec)
Heat resistance(θJa)	45[℃/W]
Power consumption of Chip PMax at OutputPower 1W (5V)	0.818[W]
Power consumption of Chip PMax at OutputPower 0.5W (3.3V)	0.283[W]

TjMax of this LSI is 125℃. TjMax is expressed with the following formulas.

TjMax = TaMax + θJa × PMax

Mounting area for package lead soldering to PCB (reference data) is shown below.
Die pad on the back of a package should connect with the substrate of opening or a V_{SS} for heat dissipation.

Mounting area for package lead soldering to PC boards



[Unit:mm]

When laying out PC boards, it is important to design the foot pattern so as to give consideration to ease of mounting, bonding, positioning of parts,reliability, wiring,and elimination of solder bridges.

The optimum design for the foot pattern varies with the materials of the substrate,the sort and thickness of used soldering paste,and the way of soldering. Therefore when laying out the foot pattern on the PC boards, refer to this figure which mean the mounting area that the package leads are allowable for soldering to PC boards.

REVISION HISTORY

Document No.	Date	Page		Description
		Previous Edition	Current Edition	
FEDL610Q340FULL-01	Jan 7, 2010	–	–	Formally edition 1

NOTICE

No copying or reproduction of this document, in part or in whole, is permitted without the consent of LAPIS Semiconductor Co., Ltd.

The content specified herein is subject to change for improvement without notice.

The content specified herein is for the purpose of introducing LAPIS Semiconductor's products (hereinafter "Products"). If you wish to use any such Product, please be sure to refer to the specifications, which can be obtained from LAPIS Semiconductor upon request.

Examples of application circuits, circuit constants and any other information contained herein illustrate the standard usage and operations of the Products. The peripheral conditions must be taken into account when designing circuits for mass production.

Great care was taken in ensuring the accuracy of the information specified in this document. However, should you incur any damage arising from any inaccuracy or misprint of such information, LAPIS Semiconductor shall bear no responsibility for such damage.

The technical information specified herein is intended only to show the typical functions of and examples of application circuits for the Products. LAPIS Semiconductor does not grant you, explicitly or implicitly, any license to use or exercise intellectual property or other rights held by LAPIS Semiconductor and other parties. LAPIS Semiconductor shall bear no responsibility whatsoever for any dispute arising from the use of such technical information.

The Products specified in this document are intended to be used with general-use electronic equipment or devices (such as audio visual equipment, office-automation equipment, communication devices, electronic appliances and amusement devices).

The Products specified in this document are not designed to be radiation tolerant.

While LAPIS Semiconductor always makes efforts to enhance the quality and reliability of its Products, a Product may fail or malfunction for a variety of reasons.

Please be sure to implement in your equipment using the Products safety measures to guard against the possibility of physical injury, fire or any other damage caused in the event of the failure of any Product, such as derating, redundancy, fire control and fail-safe designs. LAPIS Semiconductor shall bear no responsibility whatsoever for your use of any Product outside of the prescribed scope or not in accordance with the instruction manual.

The Products are not designed or manufactured to be used with any equipment, device or system which requires an extremely high level of reliability the failure or malfunction of which may result in a direct threat to human life or create a risk of human injury (such as a medical instrument, transportation equipment, aerospace machinery, nuclear-reactor controller, fuel-controller or other safety device). LAPIS Semiconductor shall bear no responsibility in any way for use of any of the Products for the above special purposes. If a Product is intended to be used for any such special purpose, please contact a ROHM sales representative before purchasing.

If you intend to export or ship overseas any Product or technology specified herein that may be controlled under the Foreign Exchange and the Foreign Trade Law, you will be required to obtain a license or permit under the Law.