



U74HC2G00

CMOS IC

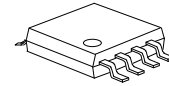
2-INPUT NAND GATE

DESCRIPTION

The UTC **U74HC2G00** is a high-speed CMOS device which provides 2-input NAND gates.

FEATURES

- * Operation Voltage Range: 2.0~6.0V
- * Low Power Dissipation: $I_{CC}=10\mu A(\text{Max})$
- * High Speed: $t_{pd}=9\text{ns}(V_{CC}=4.5\text{V}, C_L=50\text{pF})$
- * Specified from -40 to +85°C and -40 to +125°C



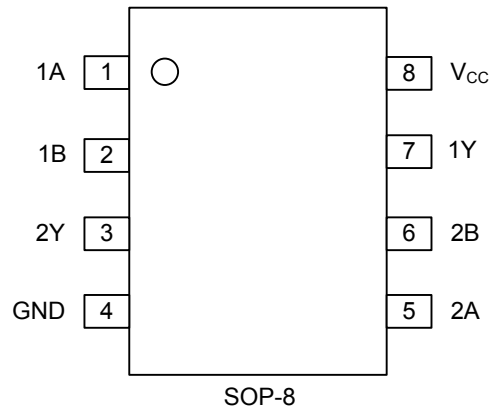
MSOP-8

ORDERING INFORMATION

Ordering Number		Package	Packing
Lead Free	Halogen Free		
U74HC2G00L-SM1-R	U74HC2G00G-SM1-R	MSOP-8	Tape Reel

<p>U74HC2G00L-SM1-R</p>	(1)Packing Type	(1) R: Tape Reel
	(2)Package Type	(2) SM1: MSOP-8
	(3)Lead Plating	(3) G: Halogen Free, L: Lead Free

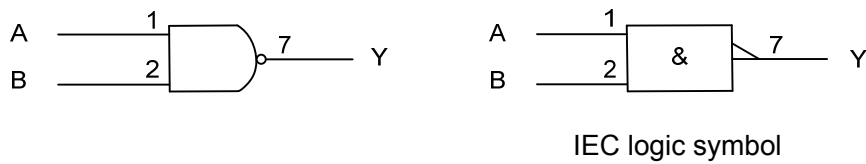
■ PIN CONFIGURATION



■ FUNCTION TABLE (each gate)

INPUT		OUTPUT
A	B	Y
L	L	H
L	H	H
H	L	H
H	H	L

■ LOGIC DIAGRAM (positive logic)



■ ABSOLUTE MAXIMUM RATINGS (unless otherwise specified)

PARAMETER	SYMBOL	RATINGS	UNIT
Supply Voltage	V_{CC}	-0.5~+7.0	V
Input Voltage	V_{IN}	-0.5~+7.0	V
Output Voltage	V_{OUT}	-0.5~ $V_{CC}+0.5$	V
Input Clamp Current	I_{IK}	±20	mA
Output Clamp Current	I_{OK}	±20	mA
Output Current	I_{OUT}	25	mA
V_{CC} or GND Current	I_{CC}	50	mA
Power dissipation	P_D	300	mW
Storage Temperature	T_{STG}	-65 ~ +150	°C

Note: Absolute maximum ratings are those values beyond which the device could be permanently damaged. Absolute maximum ratings are stress ratings only and functional device operation is not implied.

■ RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT
Supply Voltage	V_{CC}	2.0	5.0	6.0	V
Input Voltage	V_{IN}	0		V_{CC}	V
Output Voltage	V_{OUT}	0		V_{CC}	V
Input Transition Rise or Fall Times	$V_{CC}=2.0V$	t_r, t_f	1.67	625	ns
	$V_{CC}=4.5V$			139	ns
	$V_{CC}=6.0V$			83	ns
Operating Temperature	T_A	-40	25	125	°C

■ ELECTRICAL CHARACTERISTICS

(Voltage are referenced to GND=0V, $T_a=25^\circ C$, unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
High-Level Input Voltage	V_{IH}	$V_{CC}=2.0V$	1.5	1.2		V
		$V_{CC}=4.5V$	3.15	2.4		V
		$V_{CC}=6.0V$	4.2	3.2		V
Low-Level Input Voltage	V_{IL}	$V_{CC}=2.0V$		0.8	0.5	V
		$V_{CC}=4.5V$		2.1	1.35	V
		$V_{CC}=6.0V$		2.8	1.8	V
High-Level Output Voltage	V_{OH}	$V_{CC}=2.0V, I_{OH}=-20\mu A$	1.9	2.0		V
		$V_{CC}=4.5V, I_{OH}=-20\mu A$	4.4	4.5		V
		$V_{CC}=6.0V, I_{OH}=-20\mu A$	5.9	6.0		V
		$V_{CC}=4.5V, I_{OH}=-4mA$	4.13	4.32		V
		$V_{CC}=6.0V, I_{OH}=-5.2mA$	5.63	5.81		V
Low-Level Output Voltage	V_{OL}	$V_{CC}=2.0V, I_{OL}=20\mu A$		0	0.1	V
		$V_{CC}=4.5V, I_{OL}=20\mu A$		0	0.1	
		$V_{CC}=6.0V, I_{OL}=20\mu A$		0	0.1	
		$V_{CC}=4.5V, I_{OL}=4mA$		0.15	0.33	
		$V_{CC}=6.0V, I_{OL}=5.2mA$		0.16	0.33	
Input Leakage Current	$I_{I(LEAK)}$	$V_{CC}=6.0V, V_{IN}=V_{CC}$ or GND			±1	μA
Quiescent Supply Current	I_Q	$V_{CC}=6.0V, V_{IN}=V_{CC}$ or GND, $I_{OUT}=0$			10	μA
Input Capacitance	C_{IN}	$V_{CC}=5.0V, V_{IN}=V_{CC}$ or GND		1.5		pF

■ DYNAMIC CHARACTERISTICS (Input: $t_R, t_F \leq 6\text{ns}$; $\text{PRR} \leq 1\text{MHz}$)

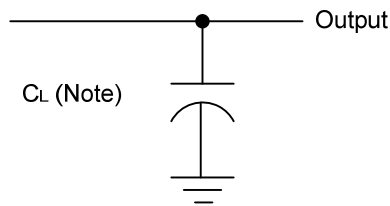
See Fig. 1 and Fig. 2 for test circuit and waveforms.

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Propagation Delay From Input (A and B) to output(Y)	t_{PHL} / t_{PLH}	$V_{CC} = 2.0\text{V}, C_L = 50\text{ pF}$		25	95	ns
		$V_{CC} = 4.5\text{V}, C_L = 50\text{ pF}$		9	19	
		$V_{CC} = 6.0\text{V}, C_L = 50\text{ pF}$		7	16	
Output transition Time	t_{THL} / t_{TLH}	$V_{CC} = 2.0\text{V}, C_L = 50\text{ pF}$		18	95	ns
		$V_{CC} = 4.5\text{V}, C_L = 50\text{ pF}$		6	19	
		$V_{CC} = 6.0\text{V}, C_L = 50\text{ pF}$		5	16	

■ OPERATING CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Power Dissipation Capacitance	Cpd	No load, $f=1\text{MHz}, V_{CC}=5$		10		pF

■ TEST CIRCUIT AND WAVEFORMS



Note: C_L includes probe and jig capacitance.

Fig. 1 Load circuitry for switching times.

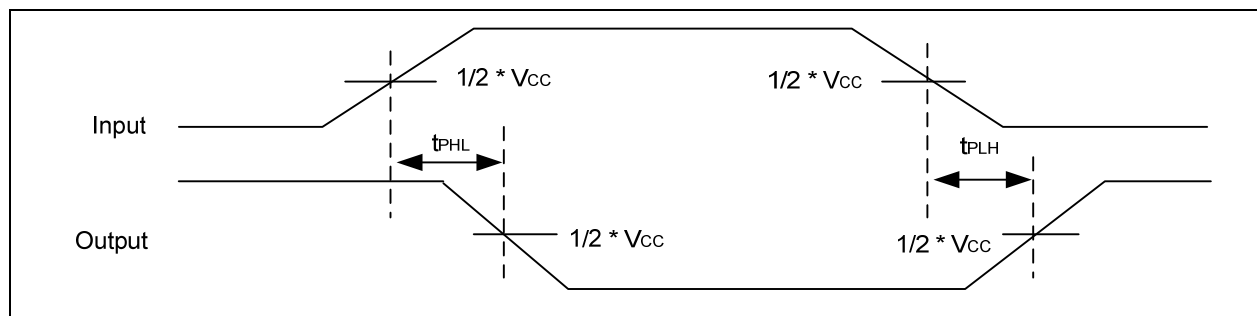


Fig. 2 Propagation delay from input(A and B) to output(Y) and Output transition time.

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