

WPMD2011

Dual P-Channel -20V, -4.4A, 52mΩ Power MOSFET

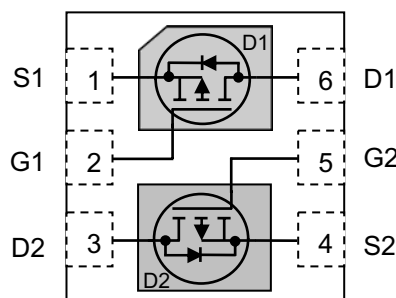
$V_{(BR)DSS}$	$R_{ds(on)}$ (Ω)
-20	0.052 @ -4.5V
	0.064 @ -2.5V
	0.080 @ -1.8V
	0.090 @ -1.5V



DFN2x2-6L

Description

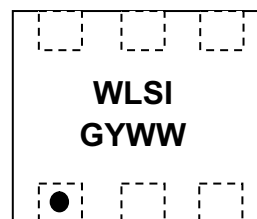
The WPMD2011 is P-Channel enhancement dual MOS Field Effect Transistor. Uses advanced trench technology and design to provide excellent $R_{DS(ON)}$ with low gate charge. This device is suitable for use in DC-DC conversion and power switch applications. Standard Product WPMD2011 is Pb-free.



Pin Configuration (Top View)

Features

- Trench Technology
- Supper high density cell design
- Excellent ON resistance for highest DC current
- Extremely low threshold voltage
- Bidirectional current flow with common source configuration
- DFN2x2 package provides exposed drain pad for excellent thermal conduction



WLSI = Company Code
G = Device Code
Y = Year (last digit)
WW = Week

Applications

- Driver for Relay, Solenoid, Motor, LED etc.
- DC-DC converter circuit
- Power switch
- High side load switch
- Battery management and charging circuit

Order Information

Device	Package	Shipping
WPMD2011-6/TR	DFN2x2-6L	3000/Tape&Reel

ABSOLUTE MAXIMUM RATINGS (Ta = 25 °C, unless otherwise noted)					
Parameter		Symbol	10S	Steady State	Unit
Drain-Source Voltage		V _{DS}	-20		V
Gate-Source Voltage		V _{GS}	±12		
Continuous Drain Current (T _J = 150 °C) ^a	T _A =25°C	I _D	-4.4	-3.7	A
	T _A =70°C		-3.5	-3.0	
Maximum Power Dissipation ^a	T _A =25°C	P _D	2.0	1.4	W
	T _A =70°C		1.3	0.9	
Continuous Drain Current (T _J = 150 °C) ^b	T _A =25°C	I _D	-3.2	-2.6	A
	T _A =70°C		-2.5	-2.1	
Maximum Power Dissipation ^b	T _A =25°C	P _D	1.0	0.7	W
	T _A =70°C		0.6	0.4	
Pulsed Drain Current ^c		I _{DM}	-15		A
Operating Junction Temperature		T _J	150		°C
Storage Temperature		T _{stg}	-55 to 150		°C

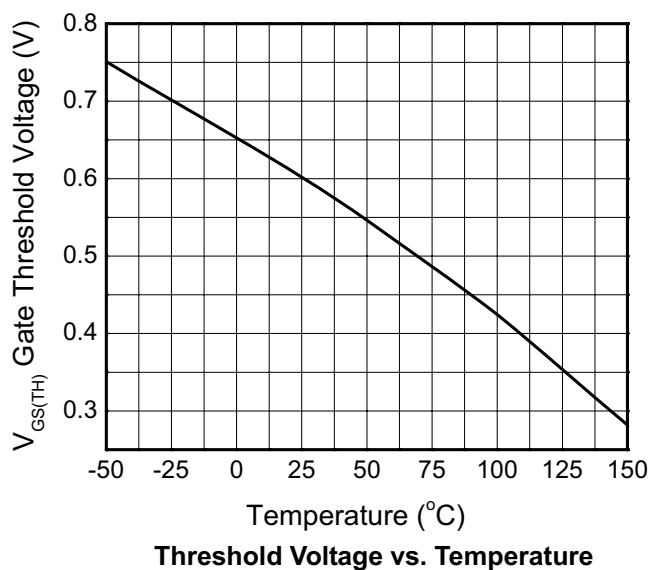
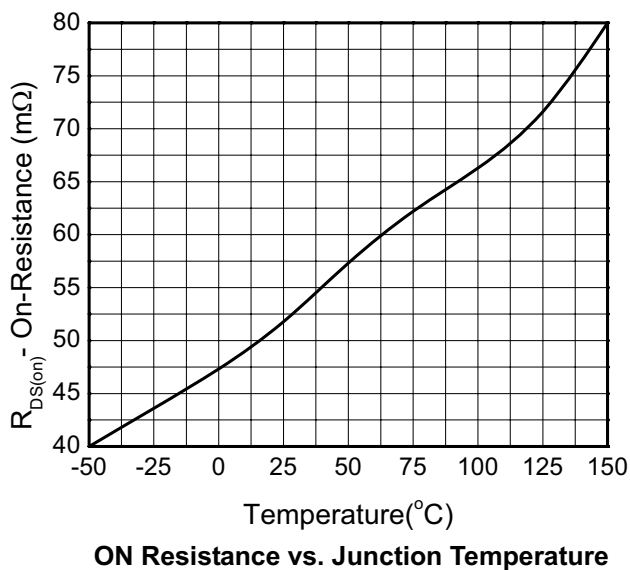
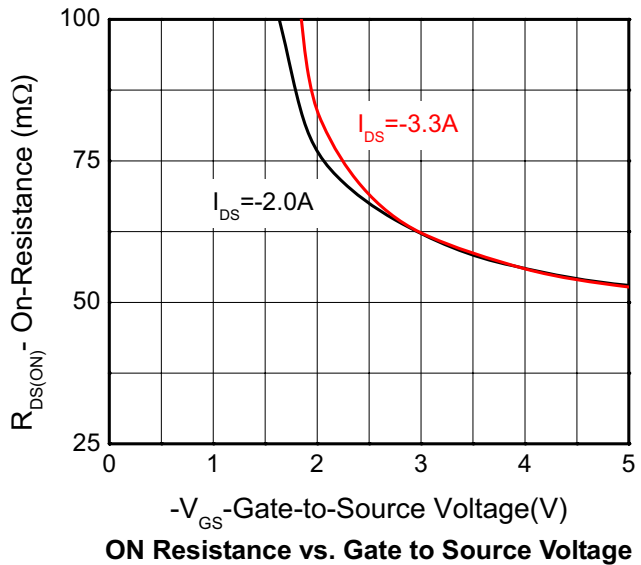
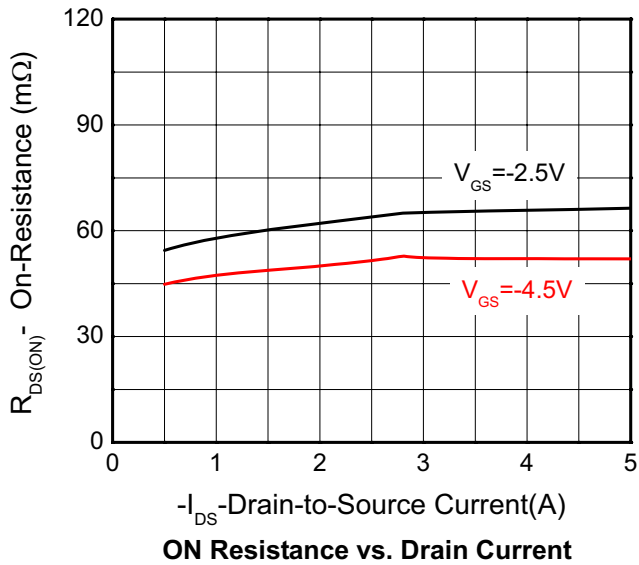
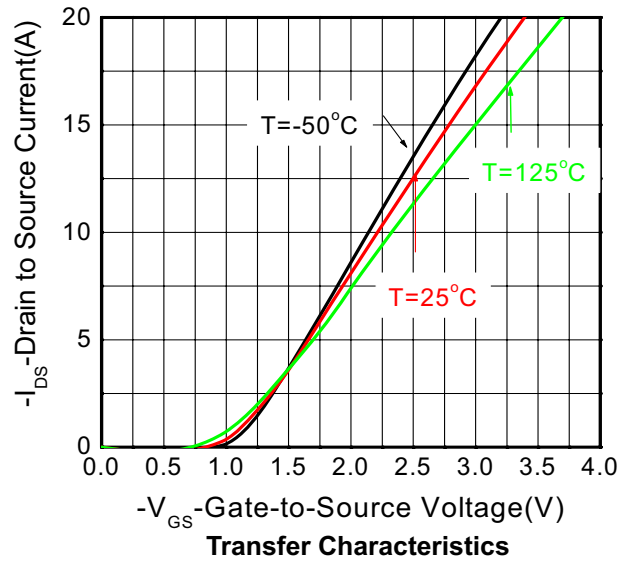
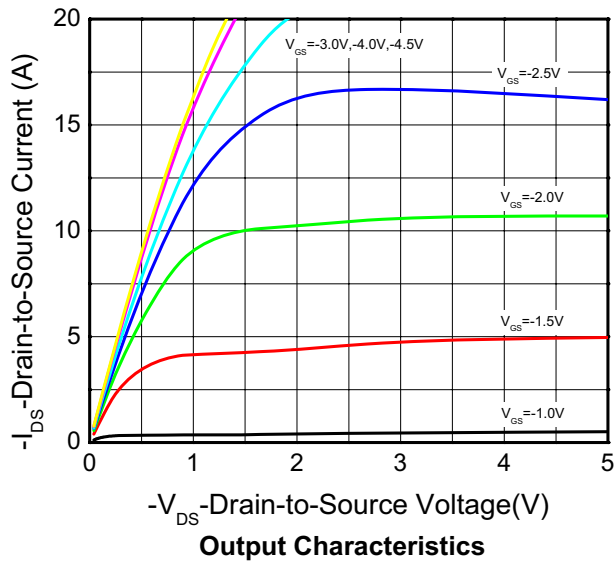
THERMAL RESISTANCE RATINGS					
Single Operation					
Parameter		Symbol	Typical	Maximum	Unit
Junction-to-Ambient Thermal Resistance ^a	t ≤ 10 s	R _{θJA}	45	60	°C/W
	Steady State		62	85	
Junction-to-Ambient Thermal Resistance ^b	t ≤ 10 s	R _{θJA}	80	115	
	Steady State		120	170	
Junction-to-Case Thermal Resistance		R _{θJC}	32	40	
Dual operation					
Junction-to-Ambient Thermal Resistance ^a	t ≤ 10 s	R _{θJA}	40	55	°C/W
	Steady State		58	80	
Junction-to-Ambient Thermal Resistance ^b	t ≤ 10 s	R _{θJA}	75	110	
	Steady State		115	160	
Junction-to-Case Thermal Resistance		R _{θJC}	30	36	

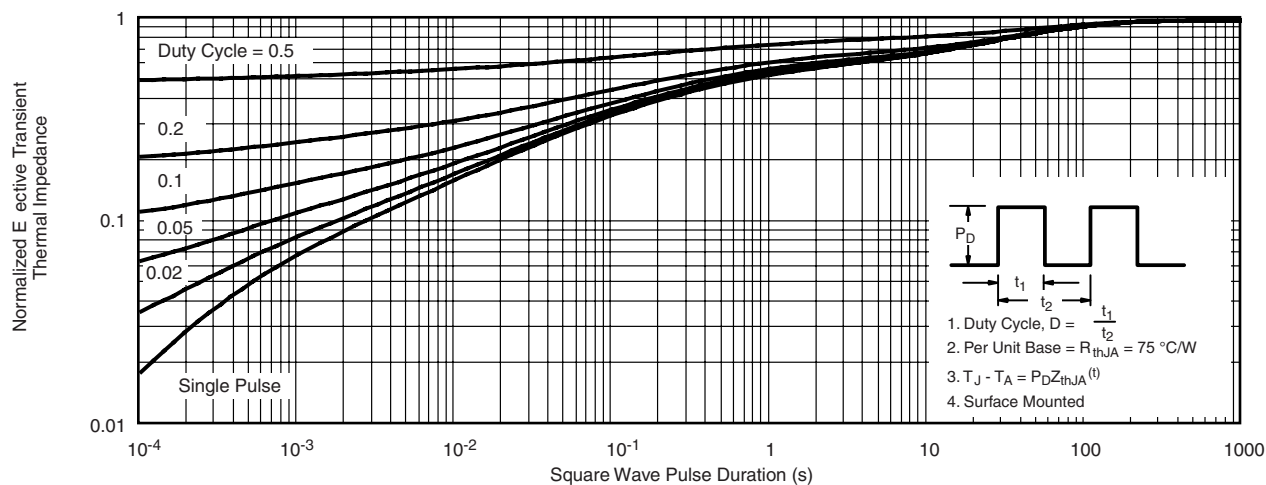
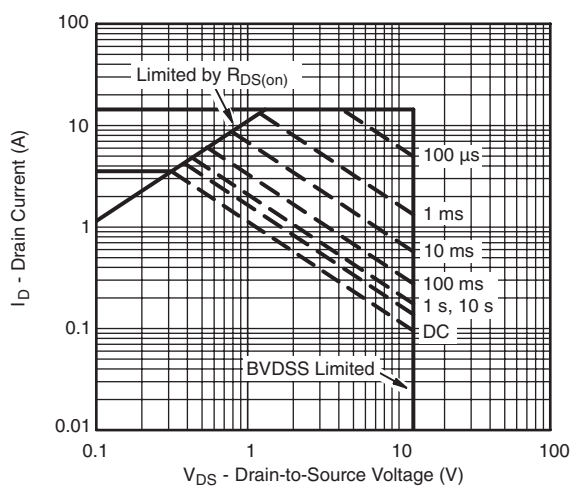
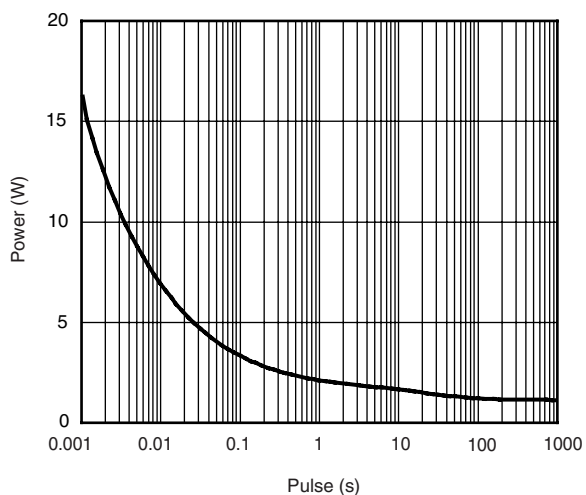
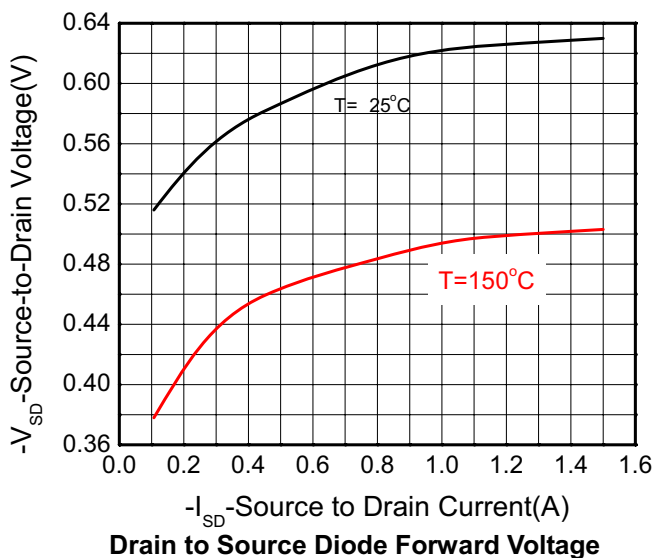
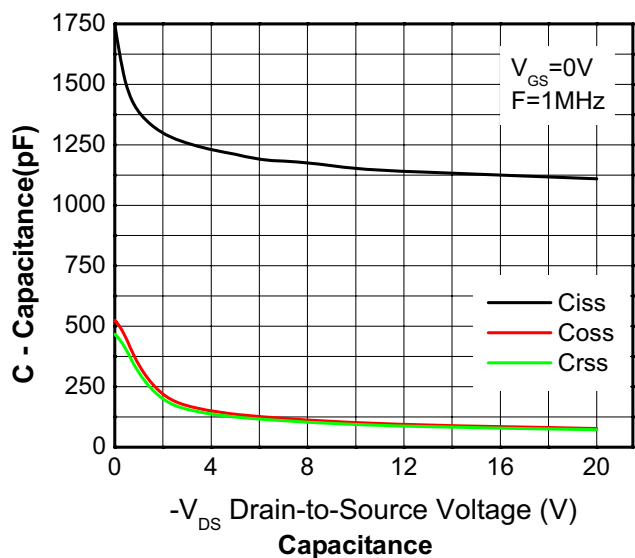
- Surface mounted on FR4 Board using 1 in sq pad size, 1oz Cu.
- Surface mounted on FR4 board using the minimum recommended pad size, 1oz Cu.
- Repetitive rating, pulse width limited by junction temperature, tp=10μs, Duty Cycle=1%
- Repetitive rating, pulse width limited by junction temperature T_J(MAX)=150°C

Electrical Characteristics (Ta= 25°C, unless otherwise noted)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Drain-Source Breakdown Voltage	BV_{DSS}	$V_{GS} = 0\text{ V}, I_D = -250\text{ }\mu\text{A}$	-20			V
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = 16\text{ V}, V_{GS} = 0\text{ V}$			-1	μA
Gate-source Leakage Current	I_{GSS}	$V_{DS} = 0\text{ V}, V_{GS} = \pm 12\text{ V}$			± 100	nA
ON CHARACTERISTICS						
Gate Threshold Voltage	$V_{GS(TH)}$	$V_{GS} = V_{DS}, I_D = -250\text{ }\mu\text{A}$	-0.35	-0.6	-1.0	V
Drain-Source On Resistance	$R_{DS(on)}$	$V_{GS} = -4.5\text{ V}, I_D = -4.0\text{ A}$		52	70	m Ω
		$V_{GS} = -2.5\text{ V}, I_D = -3.0\text{ A}$		64	85	
		$V_{GS} = -1.8\text{ V}, I_D = -2.0\text{ A}$		80	100	
		$V_{GS} = -1.5\text{ V}, I_D = -1.0\text{ A}$		90	150	
Forward Transconductance	g_{FS}	$V_{DS} = -5\text{ V}, I_D = -3.6\text{ A}$		10		S
CHARGES, CAPACITANCES AND GATE RESISTANCE						
Input Capacitance	C_{ISS}	$V_{GS} = 0\text{ V}, f = 1.0\text{ MHz},$ $V_{DS} = -10\text{ V}$		1130		pF
Output Capacitance	C_{OSS}			120		
Reverse Transfer Capacitance	C_{RSS}			115		
Total Gate Charge	$Q_{G(TOT)}$	$V_{GS} = -4.5\text{ V}, V_{DS} = -10\text{ V},$ $I_D = -2.7\text{ A}$		11		nC
Threshold Gate Charge	$Q_{G(TH)}$			0.6		
Gate-Source Charge	Q_{GS}			1.3		
Gate-Drain Charge	Q_{GD}			2.7		
SWITCHING CHARACTERISTICS						
Turn-On Delay Time	$td_{(ON)}$	$V_{GS} = -4.5\text{ V}, V_{DS} = -6\text{ V},$ $R_L = 3\text{ }\Omega, R_G = 6\text{ }\Omega$		9.5		ns
Rise Time	tr			5.8		
Turn-Off Delay Time	$td_{(OFF)}$			54		
Fall Time	tf			13		
BODY DIODE CHARACTERISTICS						
Forward Recovery Voltage	V_{SD}	$V_{GS} = 0\text{ V}, I_S = -1.0\text{ A}$		-0.62	-1.5	V

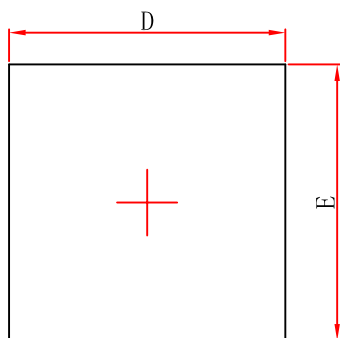
Typical Performance Characteristics



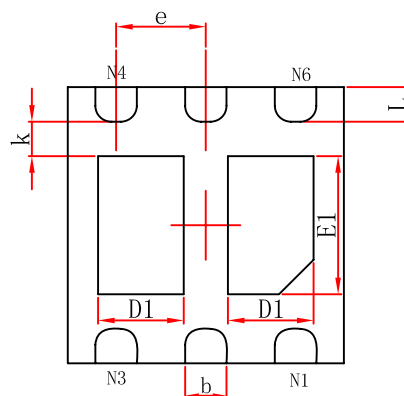


Packaging Information

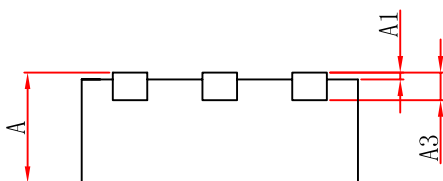
DFN2x2-6L



Top View



Bottom View



Side View

Symbol	Dimension in Millimeters	
	Min.	Max.
A	0.700	0.800
A1	0.000	0.050
A3	0.203REF	
D	1.900	2.100
E	1.900	2.100
E1	0.750	0.850
D1	0.600	0.700
k	0.200MIN	
b	0.250	0.350
e	0.650TYP	
L	0.250	0.350