plerow[™] APM0400-P33



Features

- · S₂₁ = 19.7 dB@380 MHz
 - = 18.3 dB@420 MHz
- · NF fo 10.0 dB over Frequency
- · Unconditionally Stable
- Single 5.4 V Supply
- High OIP3@Low Current

Description

APM0400-P33 is an internally matched amplifier minimodule for such application band in SMD package with the output P1dB of 33 dBm. It is compactly designed for low current consumption and high OIP3. Integrating all the components for biasing and matching within the module enhances production yield and throughput as well. It passes through the stringent DC, RF, and reliability tests. Not sample test but 100% quality control test is made before packing.



RoHS-compliant

Specifications (in Production)

Typ.@T = 25 °C, V_s = 5.4 V, Freq. = 400 MHz, $Z_{o.sys}$ = 50 ohms Specifications Parameter Unit Min Typ Max Frequency Range 380 420 MHz Gain dB 18 19 Gain Flatness dB ±0.7 ±0.8 Noise Figure dB 10 11 Output IP3⁽¹⁾ dBm 44 47 S11/S22 (2) dB -10/-12 Output P1dB dBm 32 33 Switching Time (3) usec -Supply Current mΑ 600 700 Supply Voltage ٧ 5.4 Impedance Ω 50 Max. RF Input Power dBm C.W 23 ~ 25 (before fail) Package Type & Size mm Surface Mount Type, 13Wx13Lx3.8H



2-stage Single Type

More Information

Website: www.asb.co.kr E-mail: sales@asb.co.kr

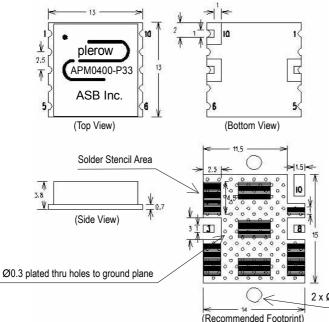
Tel: (82) 42-528-7223 Fax: (82) 42-528-7222

ASB Inc., 4th Fl. Venture Town Bldg., 367-17 Goijeong-Dong, Seo-Gu, Daejon 302-716, Korea

Operating temperature is -40 °C to +85 °C.

OIP3 is measured with two tones at an output power of 18 dBm/tone separated by 1 MHz.
S11, S22 (max) is the worst value within the frequency band.
Switching time means the time that takes for output power to get stabilized to its final level after switching DC voltage from 0 V to V_S.

Outline Drawing (Unit: mm)



Pin Number	Function			
3	RF In			
8	RF Out			
10	Vs			
Others	Ground			

Note: 1. The number and size of ground via holes in a circuit board is critical for thermal RF grounding considerations.

2. We recommend that the ground via holes be placed on the bottom of all ground pins for better RF and thermal performance, as shown in the drawing at the left side.

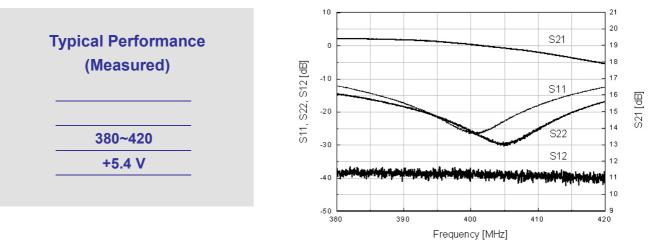
2 x Ø2.0 plated thru holes to screw on heat sinker

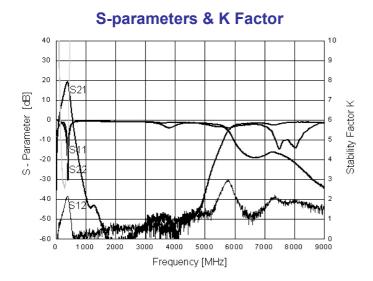


plerow[™] APM0400-P33

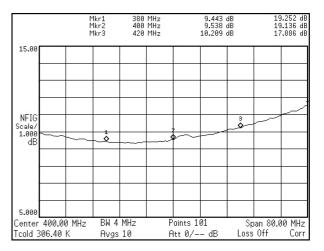
Low Noise & High OIP3 Medium Power Amplifier Module

S-parameters





Noise Figure



OIP3@380MHz

Ch Freq 380 MHz Trig Free Intermod (TOI)							
Center 380.0000000 MHz							
Ref 18 #Samp	3.35 dBm #Att	Mkr1 379.500 MHz 18.155 dBm					
Log 10							
dB/ Offst 0.35		<u> </u>	<u>+</u> Щ	× ·			
dB							
	Center 380.000 MHz +Res BW 30 kHz #VBW 3 kHz			Span 5 MHz Sweep 138 ms			
то	I (Worst Case)	381.5 MHz	45.78 dBm				
	lower upper	378.5 MHz 381.5 MHz					

OIP3@400MHz

	Ch Freg	400 MHz		Trig Free			
Interm	Intermod (TOI)						
Cen	iter 400.00	000000 MHz					
				Mkr1 399.500 MHz			
	3.35 dBm #	Atten 48 dB 🕁	\checkmark	18.018 dBm			
#Samp		i	A				
Log 10							
dB/		<u> </u>					
Offst							
0.35		<u> </u>	_ <u> / </u> \				
dB				~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~			
Contor				Span 5 MHz			
	Center 400.000 MHz #Res BW 30 kHz #VBW 3 kH			Sweep 138 ms			
то	I (Worst Case	e) 401.5 MHz	48.85 dBm				
TOI lower TOI upper		398.5 MHz 401.5 MHz	50.85 dBm 48.85 dBm				



10

plerow[™] APM0400-P33

Low Noise & High OIP3 **Medium Power Amplifier Module**

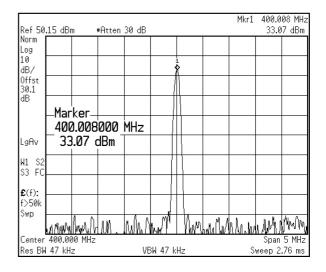
Ch Freq Trig Free 420 MHz Intermod (TOI) Center 420.0000000 MHz Mkr1 420.500 MHz Ref 18.35 dBm #Atten 48 dB 17.942 dBm #Samp Log i₽7

OIP3 @420MHz

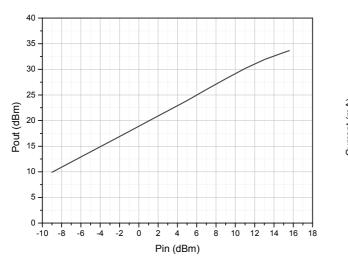
dB7 Offst 0.35 dB		Å		\		<u> </u>			
Center 420.000 MHz #Res BW 30 kHz			#VBW 3 kHz			Span 5 MHz Sweep 138 ms			
TOI (Worst Case)		421.5 MHz		47.14 dBm					
TOI lower TOI upper		418.5 MHz 421.5 MHz		48.25 dBm 47.14 dBm					

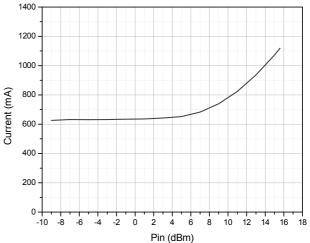
Pout vs Pin@400MHz

P1dB



Current vs Pin@400MHz

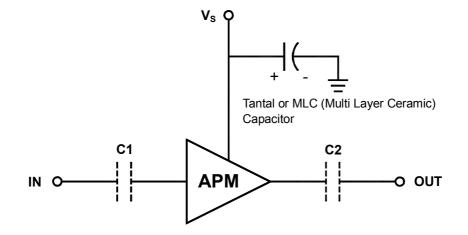




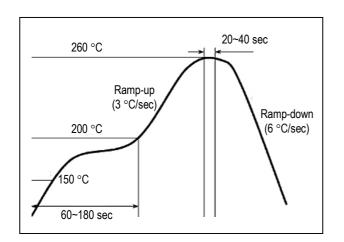


Low Noise & High OIP3 Medium Power Amplifier Module

Application Circuit



- The tantal or MLC (Multi Layer Ceramic) capacitor is optional and for bypassing the AC noise introduced from the DC supply. The capacitance value may be determined by customer's DC supply status. The capacitor should be placed as close as possible to V_s pin and be connected directly to the ground plane for the best electrical performance.
- 2) DC blocking capacitors are always necessarily placed at the input and output port for allowing only the RF signal to pass and blocking the DC component in the signal. The DC blocking capacitors are included inside the APM module. Therefore, C1 & C2 capacitors may not be necessary, but can be added just in case that the customer wants. The value of C1 & C2 is determined by considering the application frequency.



Recommended Soldering Reflow Process

Evaluation Board Layout

