# LCD MODULE SPECIFICATION

## Products Name:APAX T14A2
## 35.7CM(14.1 INCH) XGA(1024x768)
## 262K COLOR TFT LCD MODULE
## 3.3V

● **Preliminary Specification**

**This technical specification is tentative and it will be changed without notice.**


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**Version. 1.0**


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# Contents

## Revision History

| Revision Date | Page | Description |
|---|---|---|
| 4/11/2000 | All | First Release to Customers |
| 8/25/2000 | 5 | Typical power consumption 5.2W → 5.0W<br>Lamp power 3.8W → 3.6W |
| | 7 | CCFL ignition voltage 1600V → 1400V max. |
| | 8 | Add color chromaticity coordinates |
| | 15 | Add CCFL power 3.6W<br>Add CCFL ignition voltage 1400V max. |
| 9/6/2000 | 7<br>15 | CCFL current max. rating 7.0mA → 6.5mA<br>CCFL current typical 6.0mA → 5.5mA |

# 1.0 Handling Precautions

Since front polarizer is easily damaged, pay attention not to scratch it.
Be sure to turn off power supply when inserting or disconnecting from input connector.
Wipe off water drop immediately. Long contact with water may cause discoloration or spots.
When the panel surface is soiled, wipe it with absorbent cotton or other soft cloth.
Since the panel is made of glass, it may break or crack if dropped or bumped on hard surface.
Since CMOS LSI is used in this module, take care of static electricity and insure human earth when handling.
Do not open nor modify the Module Assembly.
Do not press the reflector sheet at the back of the module to any directions.
In case if a Module has to be put back into the packing container slot after once it was taken out from the container, do not press the center of the CCFL Reflector edge. Instead, press at the far ends of the CFL Reflector edge softly. Otherwise the TFT Module may be damaged.
At the insertion or removal of the Signal Interface Connector, be sure not to rotate nor tilt the Interface Connector of the TFT Module.
After installation of the TFT Module into an enclosure (Notebook PC Bezel, for example), do not twist nor bend the TFT Module even momentary. At designing the enclosure, it should be taken into consideration that no bending/twisting forces are applied to the TFT Module from outside. Otherwise the TFT Module may be damaged.
Cold cathode fluorescent lamp in LCD contains a small amount of mercury. Please follow local ordinances or regulations for disposal.
Small amount of materials having no flammability grade is used in the LCD module. The LCD module should be supplied by power complied with requirements of Limited Power Source(2.11, IEC60950 or UL1950), or be applied exemption.
The LCD module is designed so that the CFL in it is supplied by Limited Current Circuit(2.4, IEC60950 or UL1950). Do not connect the CFL in Hazardous Voltage Circuit.

# 2.0 General Description

This specification applies to the 14.1 inch Color TFT/LCD Module .

This module is designed for a display unit of notebook style personal computer.

The screen format is intended to support the XGA (1024(H) x 768(V)) screen and 262k colors

(RGB 6-bits data driver).

All input signals are LVDS interface compatible.

This module does not contain an inverter card for backlight.

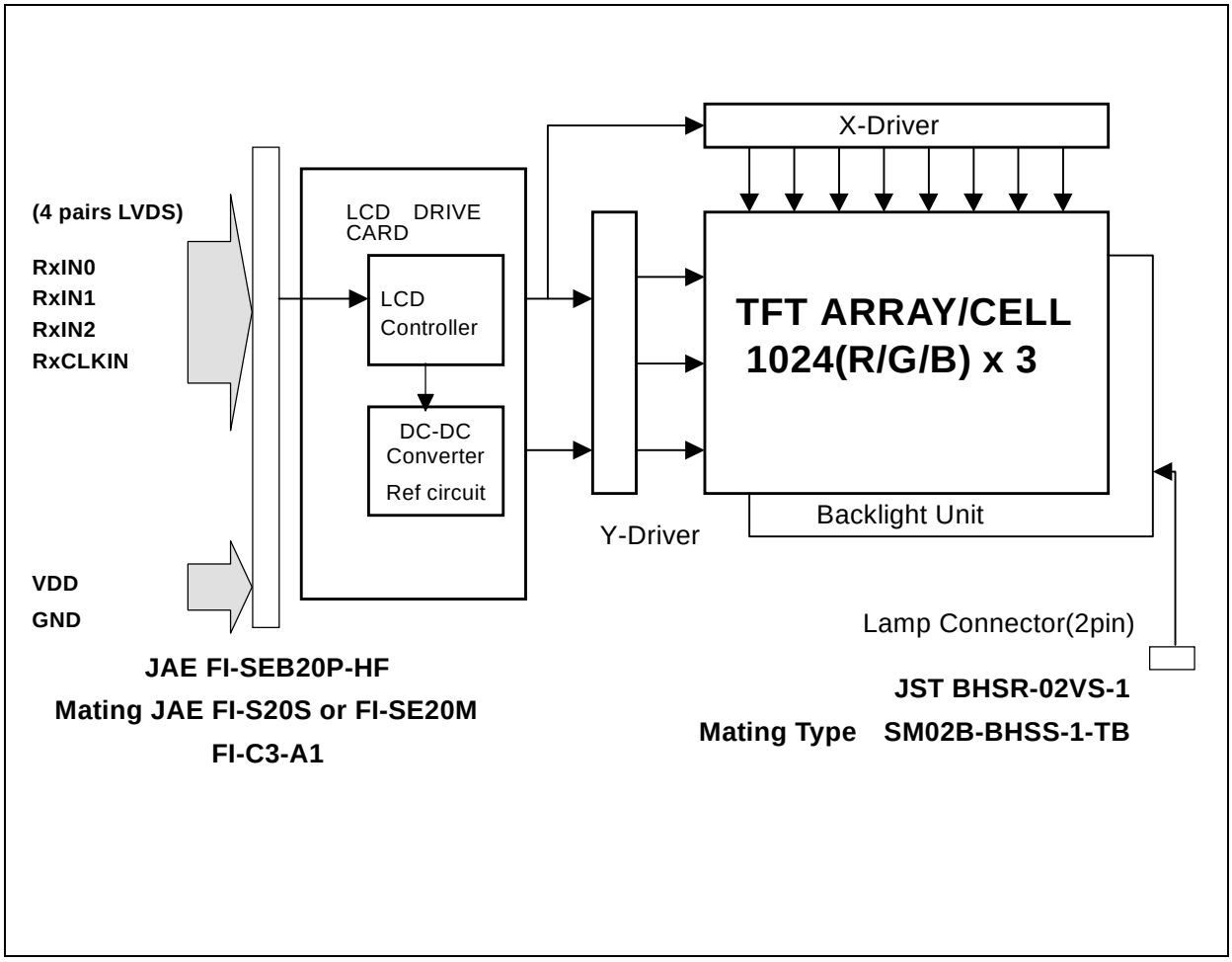
## 2.1 Display Characteristics

The following items are characteristics summary on the table under 25 ℃ condition:

| ITEMS | Unit | SPECIFICATIONS |
|---|---|---|
| Screen Diagonal | [mm] | 357(14.1") |
| Active Area | [mm] | 285.7(H) x 214.3(V) |
| Pixels H x V | | 1024(x3) x 768 |
| Pixel Pitch | [mm] | 0.279(per one triad) x 0.279 |
| Pixel Arrangement | | R.G.B. Vertical Stripe |
| Display Mode | | Normally White |
| Typical White Luminance (ICFL=6.0mA) | [cd/$m^2$] | 150Typ.(5 points average) |
| Contrast Ratio | | 200 : 1 Typ. |
| Optical Rise Time/Fall Time<br>Rise Time<br>Fall Time | [msec] | @25 $^oC$<br>20 Typ., 30 Max.<br>30 Typ., 50 Max. |
| Nominal Input Voltage VDD | [Volt] | +3.3 Typ. |
| Typical Power Consumption<br>(VDD line + VCFL line) | [Watt] | 5.0(w/o Inverter, All black pattern)<br>1.4(VDD) Typ., 3.6(Lamp) Typ. |
| Weight | [Grams] | 550 Max. (w/o Inverter) |
| Physical Size | [mm] | 298.5(W) x 226.5(H) x 6.0(D) Max. |
| Electrical Interface | | R/G/B Data, 3 Sync, Signals, Clock (4 pairs LVDS) |
| Support Color | | Native 262K colors ( RGB 6-bit data driver ) |
| Temperature Range<br>Operating<br>Storage (Shipping) | <br>[$^oC$]<br>[$^oC$] | <br>0 to +50<br>-20 to +60 |

## 2.2 Functional Block Diagram

The following diagram shows the functional block of the 14.1 inches Color TFT/LCD



## 3.0 Absolute Maximum Ratings

Absolute maximum ratings of the module is as following:

| Item | Symbol | Min | Max | Unit | Conditions |
|---|---|---|---|---|---|
| Logic/LCD Drive Voltage | VDD | -0.3 | +4.0 | [Volt] | |
| Input Voltage of Signal | Vin | -0.3 | VDD+0.3 | [Volt] | |
| CCFL Inrush current | ICFLL | - | 20 | [mA] | Note 2 |
| CCFL Current | ICFL | - | 6.5 | [mA] rms | |
| CCFL Ignition Voltage | Vs | - | 1,400 | Vrms | |
| Operating Temperature | TOP | 0 | +50 | [$^{o}$C] | Note 1 |
| Operating Humidity | HOP | 8 | 95 | [%RH] | Note 1 |
| Storage Temperature | TST | -20 | +60 | [$^{o}$C] | Note 1 |
| Storage Humidity | HST | 5 | 95 | [%RH] | Note 1 |
| Vibration | | | 1.5 10-200 | G Hz | |
| Shock | | | 50 18 | G ms | Half sine wave |

Note 1 : Maximum Wet-Bulb should be 39℃ and No condensation.

Note 2 : Duration=50 msec. Max.

## 4.0 Optical Characteristics

The optical characteristics are measured under stable conditions as follows under 25℃ condition:

| Item | | Conditions | Typ. | Note |
|---|---|---|---|---|
| Viewing Angle | [degree] | Horizontal (Right) | — | 40(min) |
| | [degree] | @K≧10 (Left) | | 40(min) |
| K: Contrast Ratio | [degree] | Vertical (Upper) | — | 10(min) |
| | [degree] | @K≧10 (Lower) | — | 30(min) |
| Contrast ratio | | | 200 | — |
| Response Time | [msec] | Rising | 20 | 30(Max.) |
| | [msec] | Falling | 30 | 50(Max.) |
| Color Chromaticity Coordinates (CIE) | | Red x | 0.577 | ±0.04 |
| | | Red y | 0.338 | ±0.03 |
| | | Green x | 0.310 | ±0.03 |
| | | Green y | 0.563 | ±0.03 |
| | | Blue x | 0.158 | ±0.03 |
| | | Blue y | 0.157 | ±0.04 |
| | | White x | 0.310 | ±0.03 |
| | | White y | 0.346 | ±0.03 |
| White Luminance (CCFL 6.0mA) | [cd/$m^2$] | | 150 (5points average) | |

# 5.0 Signal Interface

## 5.1 Connectors

Physical interface is described as for the connector on module.

These connectors are capable of accommodating the following signals and will be following components.

| | |
|---|---|
| **Connector Name / Designation** | For Signal Connector |
| **Manufacturer** | JAE |
| **Type / Part Number** | FI-SEB20P-HF |
| **Mating Housing/Part Number** | FI-S20S or FI-SE20M or FI-S20S with Shell |
| **Mating Contact/Part Number** | FI-C3-A1 |

| | |
|---|---|
| **Connector Name / Designation** | For Lamp Connector |
| **Manufacturer** | JST |
| **Type / Part Number** | BHSR-02VS-1 |
| **Mating Type / Part Number** | SM02B-BHSS-1-TB |

## 5.2 Signal Pin

| Pin# | Signal Name | Pin# | Signal Name |
|---|---|---|---|
| 1 | VDD | 2 | VDD |
| 3 | GND | 4 | GND |
| 5 | RxIN0- | 6 | RxIN0+ |
| 7 | GND | 8 | RxIN1- |
| 9 | RxIN1+ | 10 | GND |
| 11 | RxIN2- | 12 | RxIN2+ |
| 13 | GND | 14 | RxCLKIN- |
| 15 | RxCLKIN+ | 16 | GND |
| 17 | Reserved | 18 | Reserved |
| 19 | GND | 20 | GND |

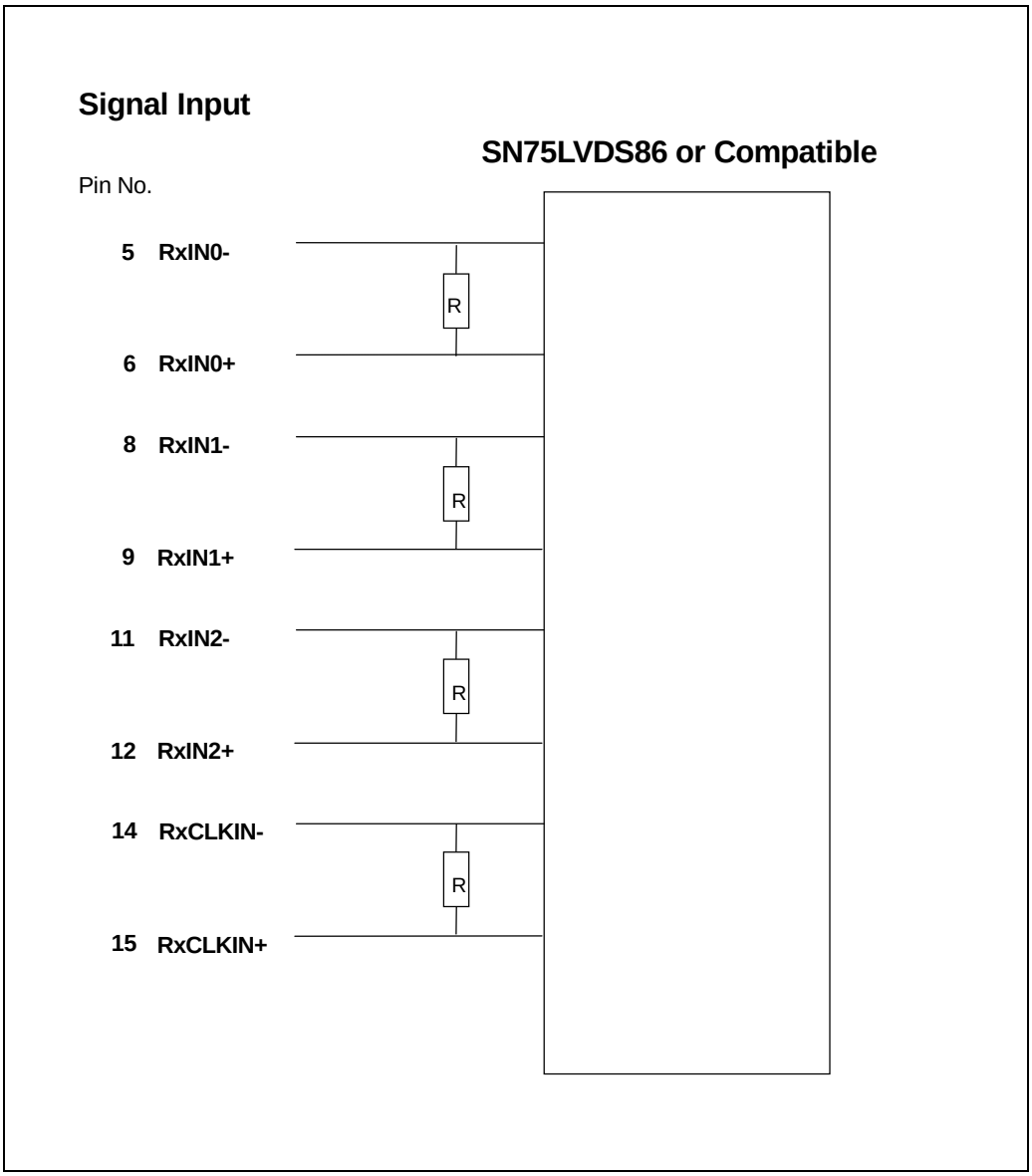
## 5.3 Signal Description

The module using a LVDS receiver. LVDS is a differential signal technology for LCD interface and high speed data transfer device. Transmitter shall be SN75LVDS84 (negative edge sampling) or compatible**.**

| Signal Name | Description |
|---|---|
| RxIN0-, RxIN0+ | LVDS differential data input(Red0-Red5, Green0) |
| RxIN1-, RxIN1+ | LVDS differential data input(Green1-Green5, Blue0-Blue1) |
| RxIN2-, RxIN2+ | LVDS differential data input(Blue2-Blue5, Hsync, Vsync, DSPTMG) |
| RxCLKIN-, RxCLKIN0+ | LVDS differential clock input |
| VDD | +3.3V Power Supply |
| GND | Ground |

**Note**: Input signals shall be low or Hi-Z state when VDD is off.

Internal circuit of LVDS inputs are as following.




The module uses a 100ohm resistor between positive and negative data lines of each receiver input

| Signal Name | Description | |
|---|---|---|
| +RED5<br>+RED4<br>+RED3<br>+RED2<br>+RED1<br>+RED0 | Red Data 5 (MSB)<br>Red Data 4<br>Red Data 3<br>Red Data 2<br>Red Data 1<br>Red Data 0 (LSB)<br><br>**Red-pixel Data** | Red-pixel Data<br>Each red pixel's brightness data consists of these 6 bits pixel data. |
| +GREEN 5<br>+GREEN 4<br>+GREEN 3<br>+GREEN 2<br>+GREEN 1<br>+GREEN 0 | Green Data 5 (MSB)<br>Green Data 4<br>Green Data 3<br>Green Data 2<br>Green Data 1<br>Green Data 0 (LSB)<br><br>**Green-pixel Data** | Green-pixel Data<br>Each green pixel's brightness data consists of these 6 bits pixel data. |
| +BLUE 5<br>+BLUE 4<br>+BLUE 3<br>+BLUE 2<br>+BLUE 1<br>+BLUE 0 | Blue Data 5 (MSB)<br>Blue Data 4<br>Blue Data 3<br>Blue Data 2<br>Blue Data 1<br>Blue Data 0 (LSB)<br><br>**Blue-pixel Data** | Blue-pixel Data<br>Each blue pixel's brightness data consists of these 6 bits pixel data. |
| -DTCLK | **Data Clock** | The typical frequency is 65.0 MHz. The signal is used to strobe the pixel data and DSPTMG signals. All pixel data shall be valid at the falling edge when the DSPTMG signal is high. |
| DSPTMG | **Display Timing** | This signal is strobed at the falling edge of -DTCLK. When the signal is high, the pixel data shall be valid to be displayed. |
| VSYNC | **Vertical Sync** | The signal is synchronized to -DTCLK . |
| HSYNC | **Horizontal Sync** | The signal is synchronized to -DTCLK . |

**Note:** Output signals from any system shall be low or Hi-Z state when VDD is off.

## 5.4 Signal Electrical Characteristics

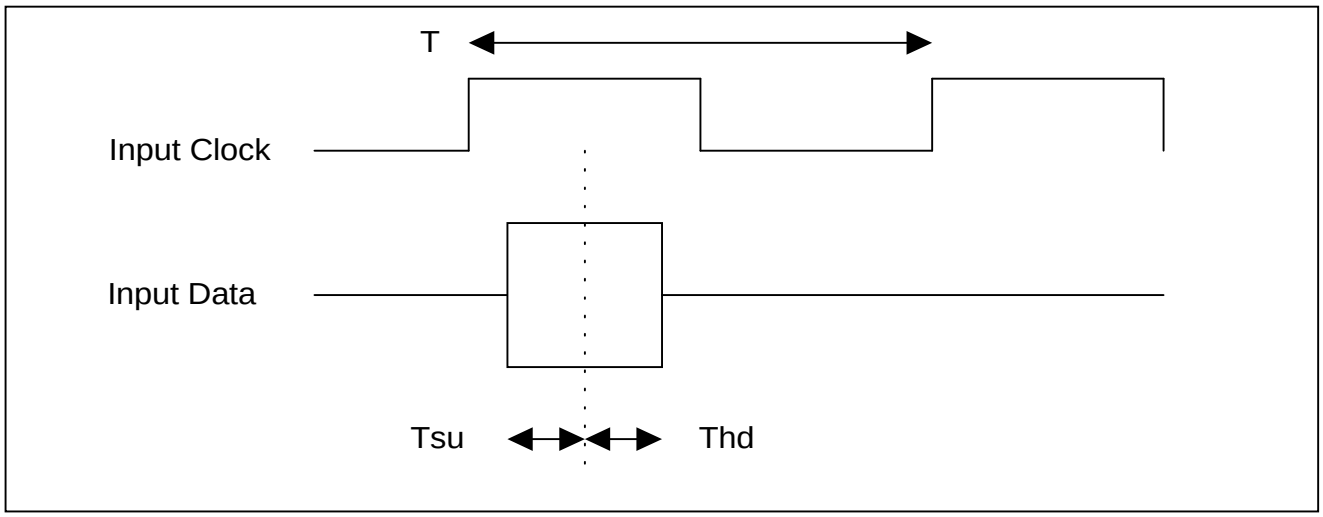
Input signals shall be low or Hi-Z state when VDD is off.
It is recommended to refer the specifications of SN75LVDS86DGG(Texas Instruments) in detail.

Signal electrical characteristics are as follows;

| Parameter | Condition | Min | Max | Unit |
|---|---|---|---|---|
| Vth | Differential Input High Voltage(Vcm=+1.2V) | | 100 | [mV] |
| Vtl | Differential Input Low Voltage(Vcm=+1.2V) | -100 | | [mV] |

LVDS Macro AC characteristics are as follows:

| | Min. | Max. |
|---|---|---|
| Clock Frequency (T) | 50MHz | 67MHz |
| Data Setup Time (Tsu) | 600ps | |
| Data Hold Time (Thd) | 600ps | |

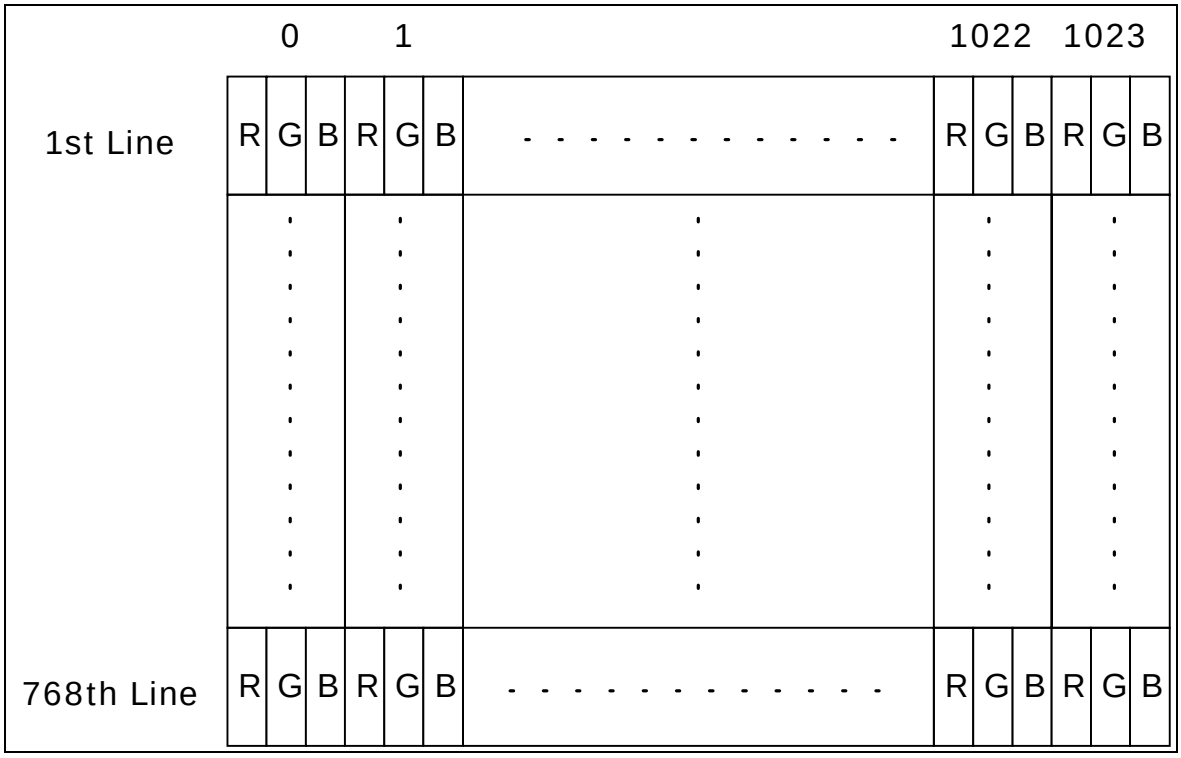



## 5.5 Signal for Lamp connector

| Pin # | Signal Name |
|---|---|
| 1 | Lamp High Voltage |
| 2 | Lamp Low Voltage |

## 6.0 Pixel Format Image

Following figure shows the relationship of the input signals and LCD pixel format.



# 7.0 Parameter guide line for CFL Inverter

| Parameter | Min | Typ | Max | Units | Condition |
|---|---|---|---|---|---|
| White Luminance(5points average) | 130 | 150 | — | [cd/$m^2$] | (Ta=25℃) |
| CCFL current(ICFL) | 2.0 | 5.5 | 6.5 | rms [mA] | (Ta=25℃) Note 2 |
| CCFL Frequency(FCFL) | 40 | 50 | 60 | [KHz] | (Ta=25℃) Note 3 |
| CCFL Ignition Voltage(Vs) | — | — | 1400 | rms[Volt] | (Ta= 0℃) Note 4 |
| CCFL Voltage (Reference) (VCFL) | — | 660 | — | rms [Volt] | (Ta=25℃) Note 5 |
| CCFL Power consumption (PCFL) | — | 3.6 | — | [Watt] | (Ta=25℃) Note 5 |

Note 1:

*1 All of characteristics listed are measured under the condition using the ADT Test inverter.

*2 In case of using an inverter other than listed, it is recommended to check the inverter carefully. Sometimes, interfering noise stripes appear on the screen, and substandard luminance or flicker at low power may happen.

*3 In designing an inverter, it is suggested to check safety circuit ver carefully. Impedance of CFL, for instance, becomes more than 1 [M ohm] when CFL is damaged.

*4 Generally, CFL has some amount of delay time after applying kick-off voltage. It is recommended to keep on applying kick-off voltage for 1 [Sec] until discharge.

*5 CFL discharge frequency must be carefully chosen so as not to produce interfering noise stripes on the screen.

*6 Reducing CFL current increases CFL discharge voltage and generally increases CFL discharge frequency. So all the parameters of an inverter should be carefully designed so as not to produce too much leakage current from high-voltage output of the inverter.

Note 2: It should be emplyed the inverter which has “Duty Dimming”, if ICFL is less than 4mA.

Note 3: CFL discharge frequency shouldbe carefully determined to avoid interference between inverter and TFT LCD.

Note 4: CFL inverter should be able to give out a power that has a generating capacity of over 1,400 voltage. Lamp units need 1,400 voltage minimum for ignition.

Note 5: Calculator value for reference (ICFL×VCFL=PCFL)

# 8.0 Interface Timings

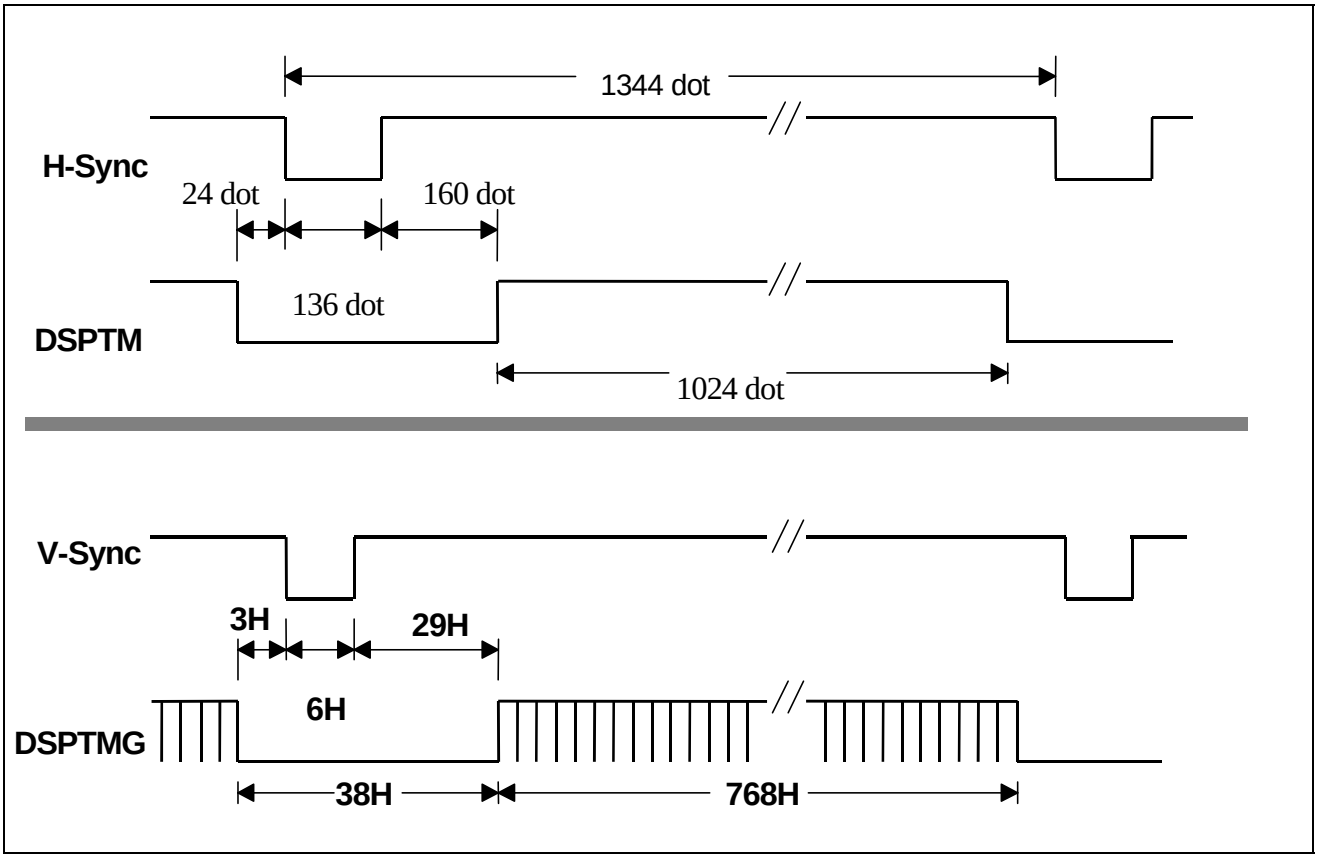
Basically, interface timings should match the VESA 1024x768 /60Hz (VG901101) manufacturing guide line timing.

## 8.1 Timing Characteristics

| Symbol | Description | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| fdck | DTCLK Frequency | | 65.00 | | [MHz] |
| tck | DTCLK cycle time | | 15.38 | | [nsec] |
| tx | X total time | 1206 | 1344 | 2047 | [tck] |
| tacx | X active time | 129 | 1024 | | [tck] |
| tbkx | X blank time | 90 | 320 | | [tck] |
| Hsync | H frequency | | 48.363 | | [KHz] |
| Hsw | H-Sync width | 2 | 136 | | [tck] |
| Hbp | H back porch | 1 | 160 | | [tck] |
| Hfp | H front porch | 0 | 24 | | [tck] |
| ty | Y total time | 771 | 806 | 1023 | [tx] |
| tacy | Y active time | | 768 | | [tx] |
| Vsync | Frame rate | (55) | 60 | 61 | [Hz] |
| Vw | V-sync Width | 1 | 6 | | [tx] |
| Vfp | V-sync front porch | 1 | 3 | | [tx] |
| Vbp | V-sync back porch | 7 | 29 | 63 | [tx] |

**Note:** Hsw(H-sync width) + Hbp(H-sync back porch) should be less than 515 tck.

## 8.2 Timing Definition



# 9.0 Power Consumption

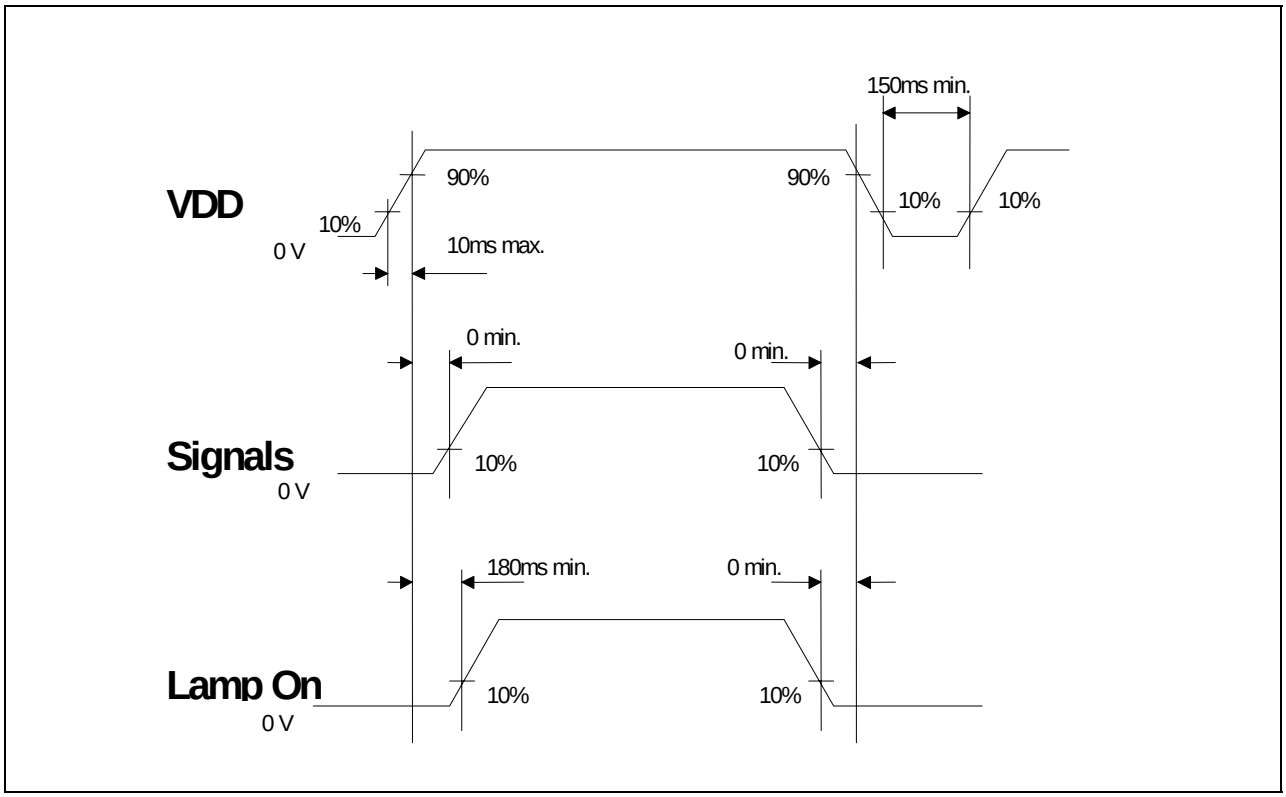
Input power specifications are as follows;

| Symble | Parameter | Min | Typ | Max | Units | Condition |
|---|---|---|---|---|---|---|
| VDD | Logic/LCD Drive Voltage | 3.0 | 3.3 | 3.6 | [Volt] | Load Capacitance 20uF |
| PDD | VDD Power | | 1.4 | | [Watt] | All Black Pattern |
| PDD Max | VDD Power max | | | 1.65 | [Watt] | Max Pattern **Note** |
| IDD | IDD Current | | 420 | | mA | All Black Pattern |
| IDD Max | IDD Current max | | | 500 | mA | Max Pattern **Note** |
| VDDrp | Allowable Logic/LCD Drive Ripple Voltage | | | 100 | [mV] p-p | |
| VDDns | Allowable Logic/LCD Drive Ripple Noise | | | 100 | [mV] p-p | |

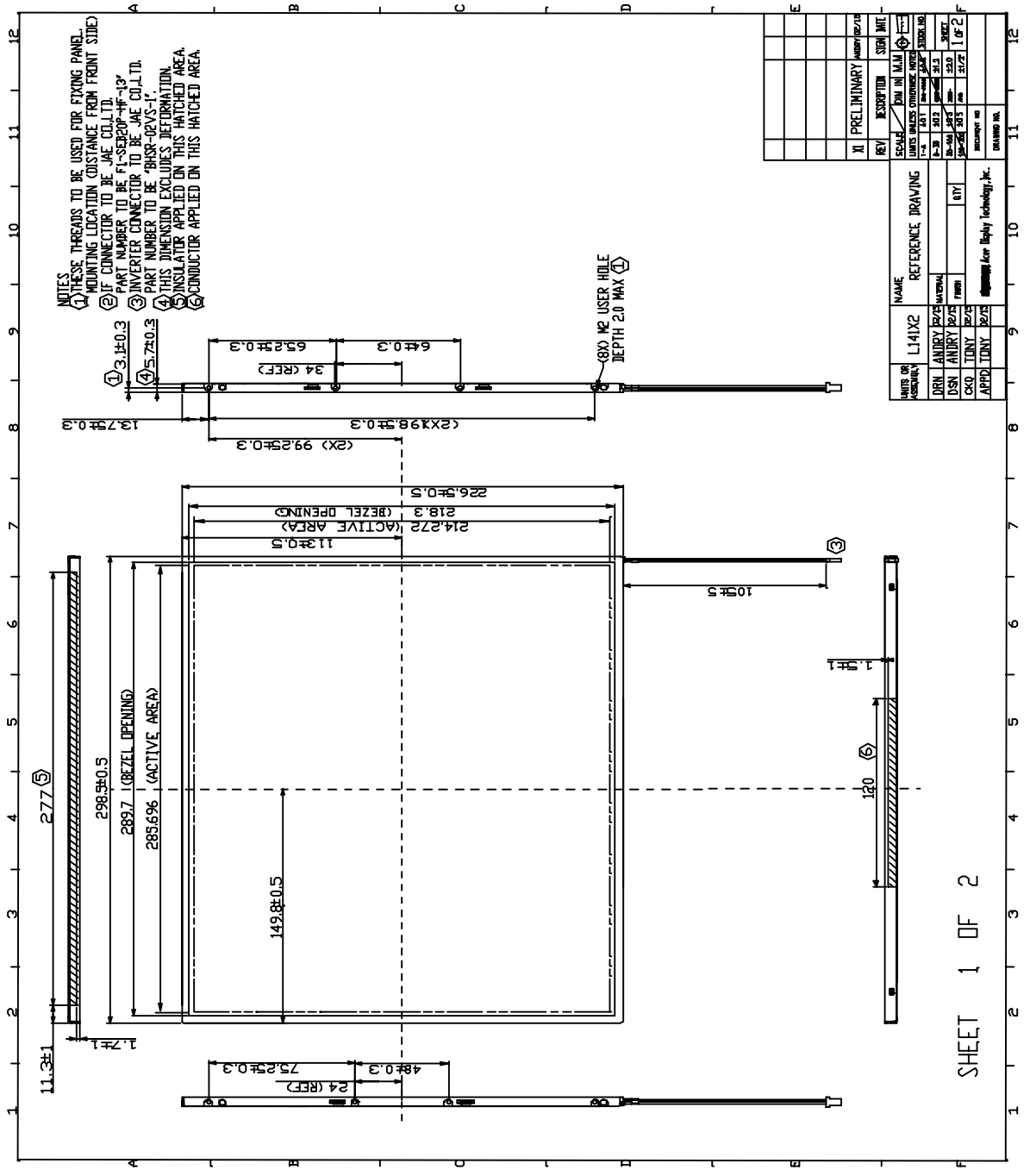
Note: VDD=3.3V

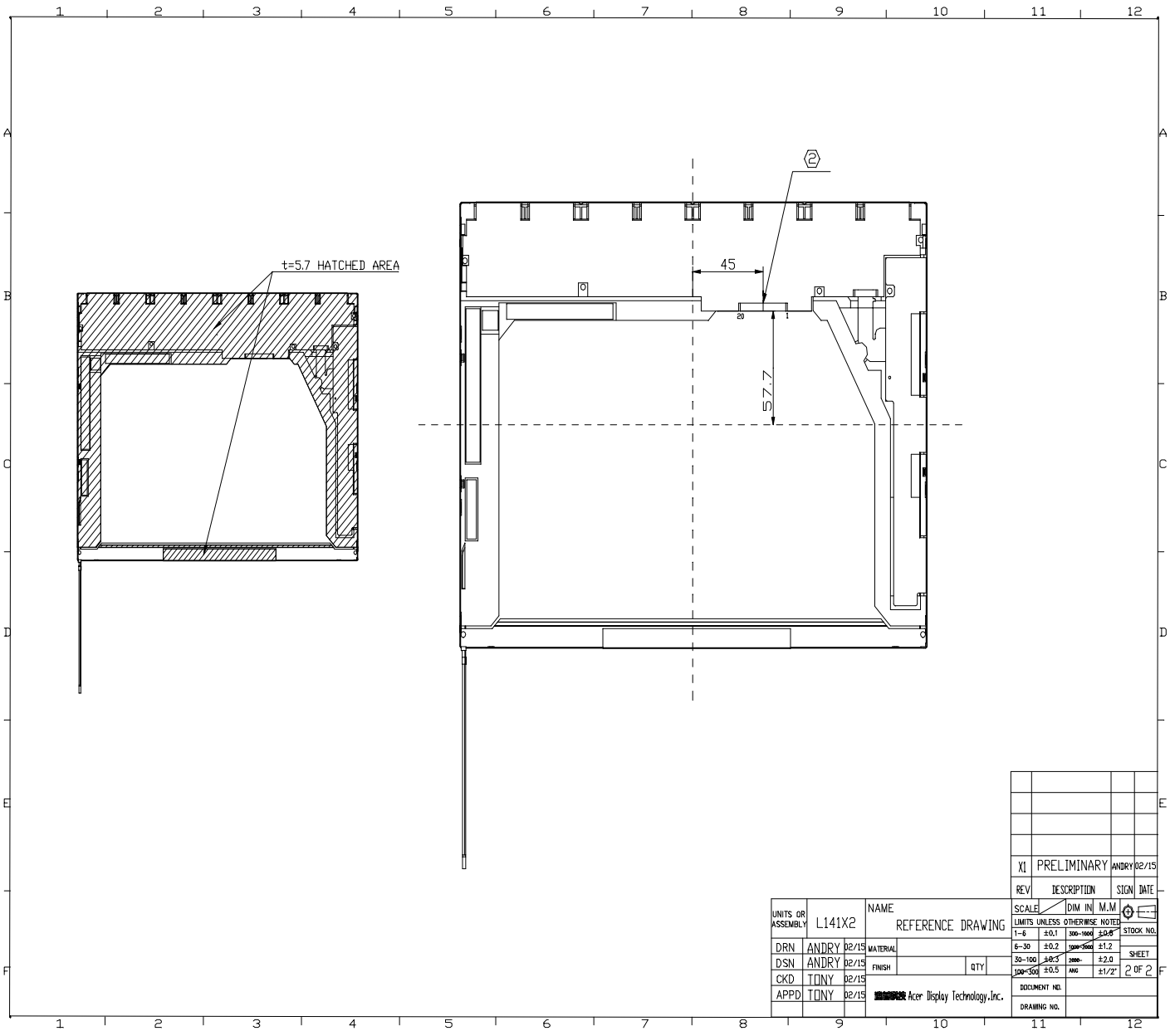
## 10. Power ON/OFF Sequence

VDD power and lamp on/off sequence is as follows. Interface signals are also shown in the chart. Signals from any system shall be Hi-Z state or low level when VDD is off.



# 11.0 Mechanical Characteristics






| | | | | | | | |
|---|---|---|---|---|---|---|---|
| X1 | PRELIMINARY | ANDRY 02/15 | | | | | |
| REV | DESCRIPTION | SIGN DATE | | | | | |
| UNITS OR ASSEMBLY | L141X2 | NAME REFERENCE DRAWING | SCALE | DIM IN | M.M | | |
| DRN ANDRY 02/15 | | | LIMITS UNLESS OTHERWISE NOTED | | | | |
| DSN ANDRY 02/15 | MATERIAL | | 1~6 | ±0.1 | 300~1000 | ±0.8 | STOCK NO. |
| CKD TONY 02/15 | FINISH | QTY | 6~30 | ±0.2 | 1000~3000 | ±1.2 | SHEET |
| APPD TONY 02/15 | [redacted] Acer Display Technology,Inc. | | 30~100 | ±0.3 | 2000~ | ±2.0 | 2 OF 2 |
| | | | 100~300 | ±0.5 | ANG | ±1/2° | |
| | | | DOCUMENT NO. | | | | |
| | | | DRAWING NO. | | | | |