Non-Clip, Low EMI, 2.8W Mono Filterless Class-D Audio Power Amplifier with Auto-Recovery

DESCRIPTION

The EUA2045 is a high efficiency, 2.8W mono class-D audio power amplifier with non-clip. A low noise, filterless PWM architecture eliminates the output filter, reducing external component count, system cost, and simplifying design.

Operating in a single 5V supply, EUA2045 is capable of driving 4Ω speaker load at a continuous average output of 2.8W/10% THD+N or 2.2W/1% THD+N. The EUA2045 has high efficiency with speaker load compared to a typical class AB amplifier. With a 3.6V supply driving an 8Ω speaker , the efficiency for a 400mW power level is 84%.

EUA2045 feature non-clip output control function which detects output signal clip due to the over level input signal and suppress the output signal clip automatically. Also the non-clip output control function can adapt the output clip cause by power supply voltage down with battery.

In cellular handsets, the earpiece, speaker phone, and melody ringer can each be driven by the EUA2045.

The EUA2045 is available in space-saving WCSP and TDFN-8 packages.

FEATURES

- Unique Modulation Scheme Reduces EMI Emissions
- Unique Non-Clip function , Variable NCN1, NCN2,NCNOFF mode Select
- Short Circuit Auto-Recovery
- Efficiency at 3.6V With an 8-Ω Speaker:
  - 84% at 400 mW
- Low Quiescent Current and Shutdown Current
- 2.5V to 5.5V Wide Supply Voltage
- Shutdown Pin Compatible with 1.8V Logic GPIO
- Optimized PWM Output Stage Eliminates LC Output Filter
- Improved PSRR (-68 dB) Eliminates Need for a Voltage Regulator
- Fully Differential Design Reduces RF Rectification and Eliminates Bypass Capacitor
- Improved CMRR Eliminates Two Input Coupling Capacitors
- Internally Generated 325-kHz Switching Frequency
- Integrated Pop and Click Suppression Circuitry
- 1.5mm×1.5mm Wafer Chip Scale Package (WCSP) and 3mm×3mm TDFN-8 Package
- RoHS Compliant and 100% Lead(Pb)-Free Halogen-Free

APPLICATIONS

- Ideal for Wireless or cellular Handsets and PDAs

Typical Application Circuit

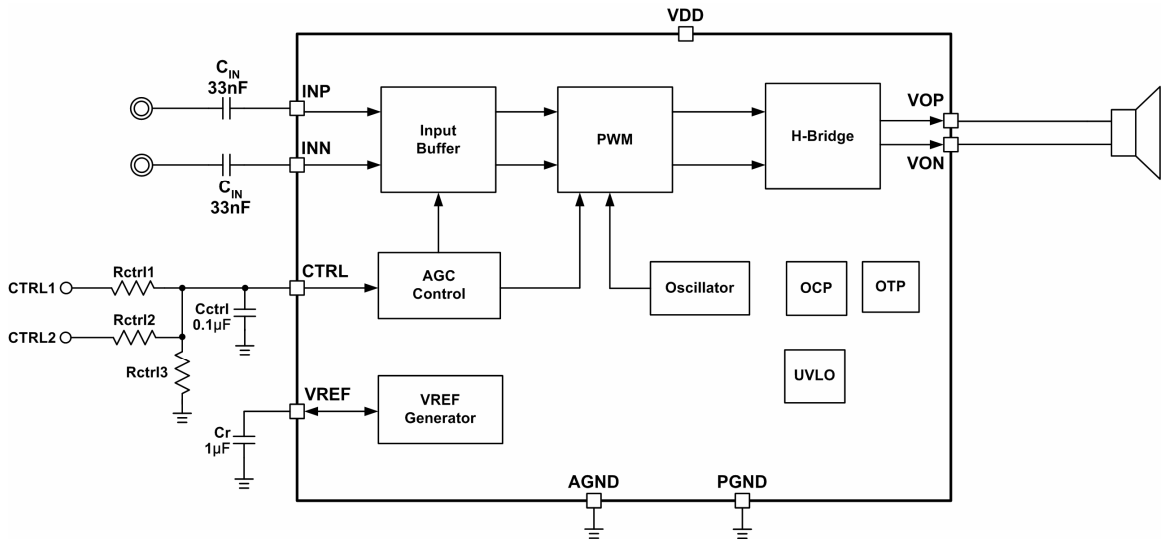
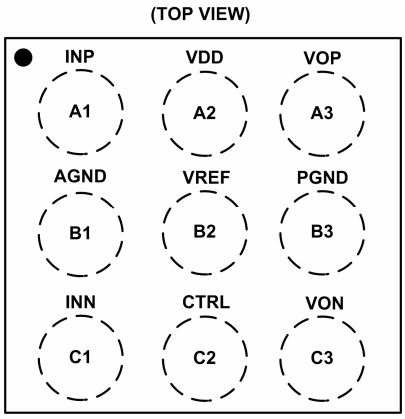
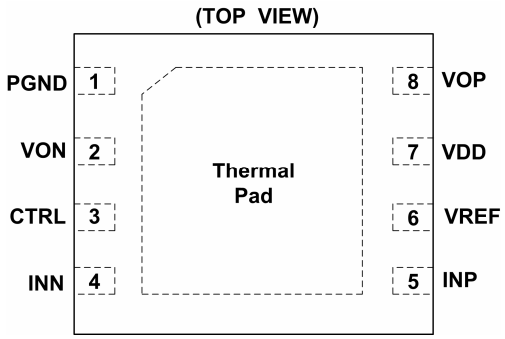


Figure1.

Pin Configurations

Package Type	Pin Configurations	Package Type	Pin Configurations
WCSP-9		TDFN-8	

Pin Description

PIN	WCSP-9	TDFN-8	I/O	DESCRIPTION
INP	A1	5	A	Positive input terminal (differential +)
VDD	A2	7	Power	Power supply
VOP	A3	8	O	Positive output terminal (differential +)
AGND	B1	Thermal Pad	GND	GND for analog circuits
VREF	B2	6	A	Analog reference power supply terminal
PGND	B3	1	GND	GND for output
INN	C1	4	A	Negative input terminal (differential -)
CTRL	C2	3	I	Shut down and Non-clip control terminal
VON	C3	2	O	Negative output terminal (differential -)

(Note) I: Input terminal O: Output terminal A: Analog terminal

Ordering Information

Order Number	Package Type	Marking	Operating Temperature Range
EUA2045HIR1	WCSP-9	xxx J00	-40 °C to +85°C
EUA2045JIR1	TDFN-8	xxxxx A2045	-40 °C to +85°C

EUA2045 □ □ □ □

- Lead Free Code
  1: Lead Free, Halogen-Free
- Packing
  R: Tape & Reel
- Operating temperature range
  I: Industry Standard
- Package Type
  H: WCSP
  J: TDFN

Absolute Maximum Ratings

- Supply Voltage, V_{DD} ---------- -0.3 V to 6V
- Voltage at Any Input Pin ---------- -0.3 V to V_{DD} +0.3V
- Junction Temperature, T_{JMAX} ---------- 150°C
- Storage Temperature Rang, T_{stg} ---------- -65°C to 150°C
- ESD Susceptibility ---------- 2kV
- Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds ---------- 260°C
- Thermal Resistance

  θ_{JA} (WCSP-9) ---------- 110°C/W

  θ_{JA} (TDFN-8) ---------- 72°C/W

Recommended Operating Conditions

		Min.	Max.	Unit
Supply voltage, V_{DD}		2.5	5.5	V
Common mode input voltage range, V_{IC}	V_{DD}=2.5V,5.5V,CMRR ≤ -49dB	0.5	V_{DD}-0.8	V
Operating free-air temperature, T_A		-40	85	°C

Electrical Characteristics T_A = 25°C (Unless otherwise noted)

Symbol	Parameter	Conditions	EUA2045			Unit
			Min.	Typ.	Max.	
$\|V_{OS}\|$	Output offset voltage (measured differentially)	$V_{I=}$ 0V,A_V=2 V/V, V_{DD}=2.5V to 5.5V		1	25	mV
PSRR	Power supply rejection ratio	V_{DD}= 2.5V to 5.5V		-68	-55	dB
$\|I_{IH}\|$	High-level input current	V_{DD}= 5.5V, V_I= 5.8V			1	μA
$\|I_{IL}\|$	Low-level input current	V_{DD}= 5.5V, V_I= -0.3V			1	μA
$I_{(Q)}$	Quiescent current	V_{DD}= 5.5V, no load		4.8		mA
		V_{DD}= 3.6V, no load		4.0		
		V_{DD}= 2.5V, no load		3.5		
$I_{(SD)}$	Shutdown current	V_{CTRL}=0V, V_{DD}= 2.5V to 5.5V		0.5		μA
rDS(on)	Static drain-source on-state resistance	V_{DD}= 2.5V		700		mΩ
		V_{DD}= 3.6V		500		
		V_{DD}= 5.5V		400		
$f_{(sw)}$	Switching frequency	V_{DD}= 2.5V to 5.5V	270	325	380	kHz
V_{UVLH}	Power supply start-up threshold voltage			2		V
V_{UVLL}	Power supply shut-down threshold voltage			1.8		V

Electrical Characteristics T_A = 25°C ,Gain= 2V/V,R_L=8Ω (Unless otherwise noted)

Symbol	Parameter	Conditions		EUA2045 Min.	EUA2045 Typ.	EUA2045 Max.	Unit
P_O	Output power	THD+N=10%, f=1kHz, R_L=4Ω	V_{DD}= 5V		2.8		W
			V_{DD}= 3.6V		1.42		
			V_{DD}= 2.5V		0.68		
		THD+N=1%, f=1kHz, R_L=4Ω	V_{DD}= 5V		2.26		W
			V_{DD}= 3.6V		1.14		
			V_{DD}= 2.5V		0.54		
		THD+N=10%, f=1kHz, R_L=8Ω	V_{DD}= 5V		1.67		W
			V_{DD}= 3.6V		0.86		
			V_{DD}= 2.5V		0.42		
		THD+N=1%, f=1kHz, R_L=8Ω	V_{DD}= 5V		1.36		W
			V_{DD}= 3.6V		0.69		
			V_{DD}= 2.5V		0.33		
THD+N	Total harmonic distortion plus noise	V_{DD}= 5V,P_O=1W, R_L=8Ω, f=1kHz			0.15		%
		V_{DD}= 3.6V,P_O=0.5W, R_L=8Ω, f=1kHz			0.15		
		V_{DD}= 2.5V,P_O=200mW, R_L=8Ω, f=1kHz			0.15		
kSVR	Supply ripple rejection ratio	V_{DD}= 3.6V, Inputs ac-grounded with C_I= 2μF	f=217 Hz, $V_{(RIPPLE)}$=200mVpp		-60		dB
SNR	Signal-to-noise ratio	V_{DD}= 5V,P_O=1W, R_L=8Ω			89		dB
Vn	Output voltage noise	V_{DD}= 3.6V, f=20Hz to 20kHz,Inputs ac-grounded with C_I= 2μF	No weighting		181		μV_{RMS}
			A weighting		140		
t_{STUP}	Start-up time	Cr= 1μF			32		ms
t_{WK}	Wake-up mode settling time				180		ms
t_{SD}	Shutdown settling time				180		ms
t_{MOD}	Each mode settling time			0.1			ms
NCN							
V_{NCN1}	Non-clip1 mode setting threshold voltage			1.20		V_{DD}	V
V_{NCN2}	Non-clip2 mode setting threshold voltage			0.80		1.10	V
V_{NCNO}	Non-clip off mode setting threshold voltage			0.36		0.68	V
V_{SD}	Shut down mode setting threshold voltage			0		0.14	V
t_{AT1}	Attack time 1	V_{DD}= 3.6V			45		ms
t_{RL1}	Release time 1	V_{DD}= 3.6V			2.6		s
t_{AT2}	Attack time 2	V_{DD}= 3.6V			10		ms
t_{RL2}	Release time 2	V_{DD}= 3.6V			1.2		s
A_{MAX}					-10		dB

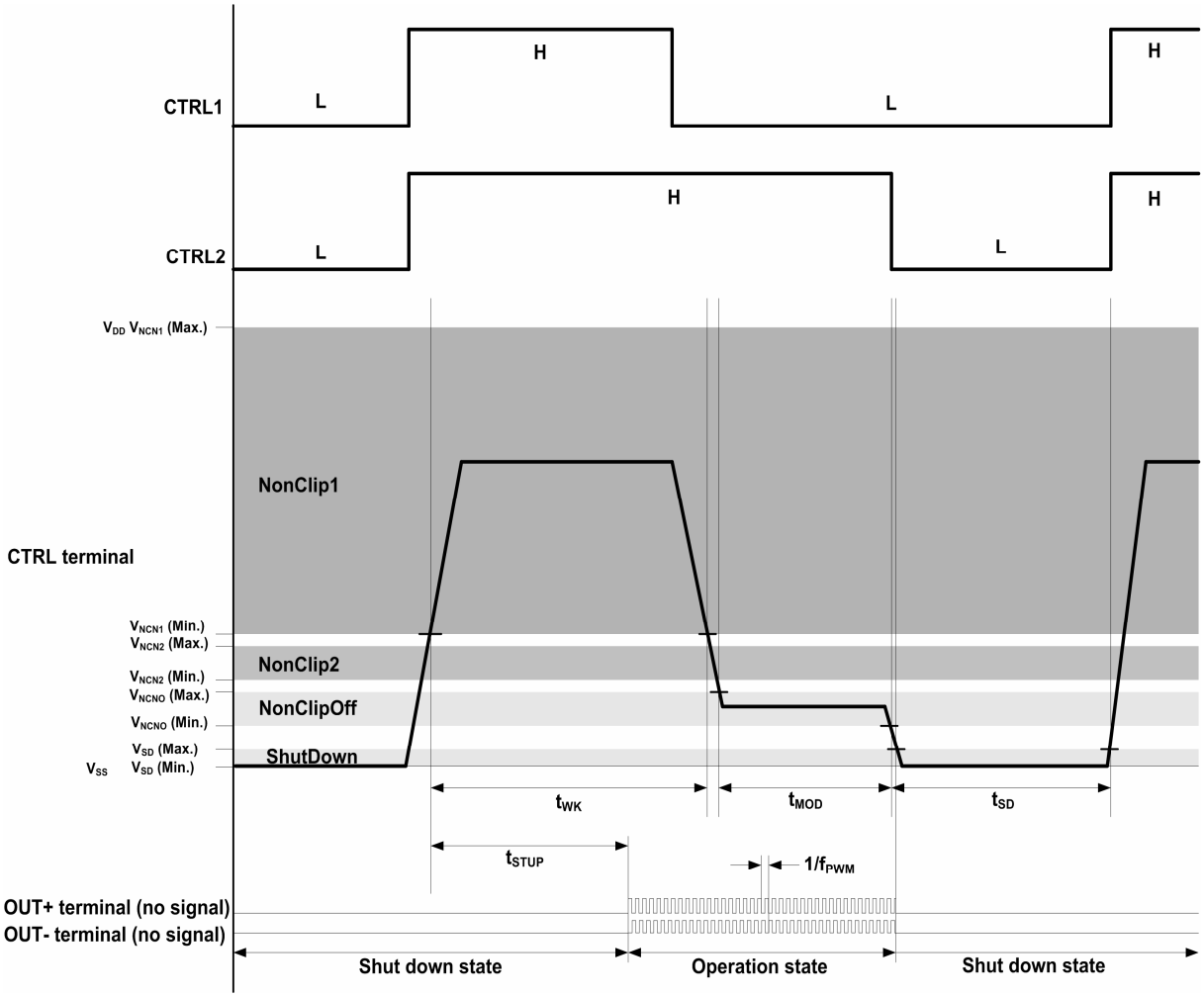

CTRL1
CTRL2
L
H
L
H
L
H
L
H
V_{DD} V_{NCN1} (Max.)
NonClip1
CTRL terminal
V_{NCN1} (Min.)
V_{NCN2} (Max.)
NonClip2
V_{NCN2} (Min.)
V_{NCNO} (Max.)
NonClipOff
V_{NCNO} (Min.)
V_{SD} (Max.)
V_{SS}
V_{SD} (Min.)
ShutDown
t_{WK}
t_{MOD}
t_{SD}
t_{STUP}
$1/f_{PWM}$
OUT+ terminal (no signal)
OUT- terminal (no signal)
Shut down state
Operation state
Shut down state

Figure2.

Typical Operating Characteristics

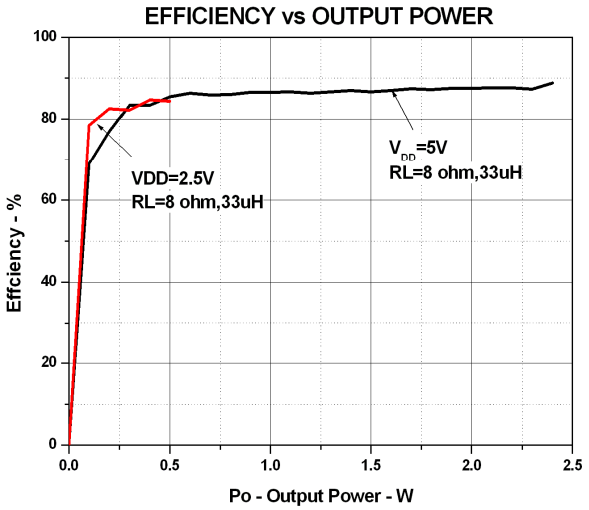


Figure3.

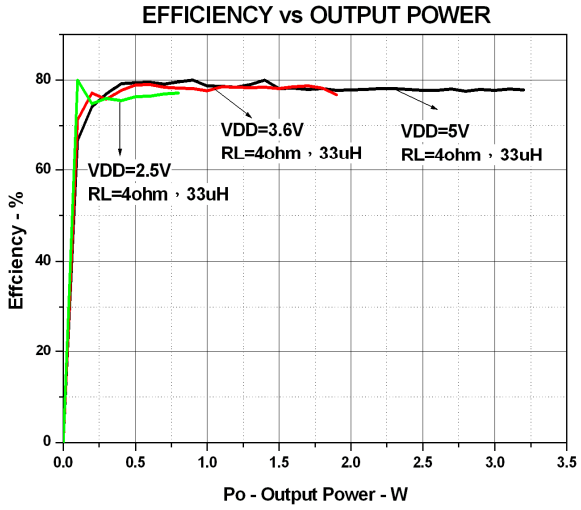


Figure4.

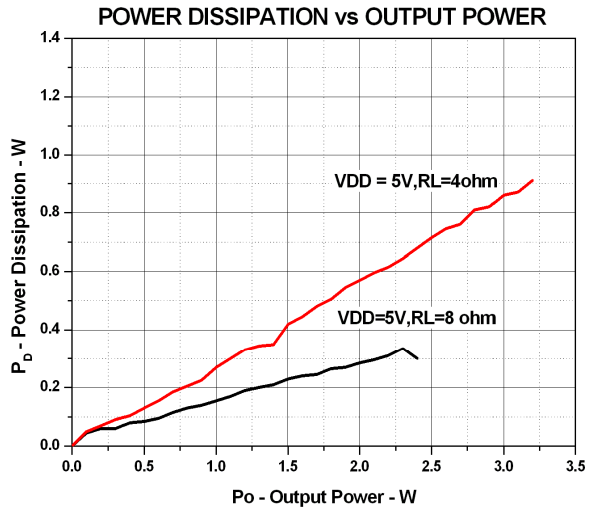


Figure5.

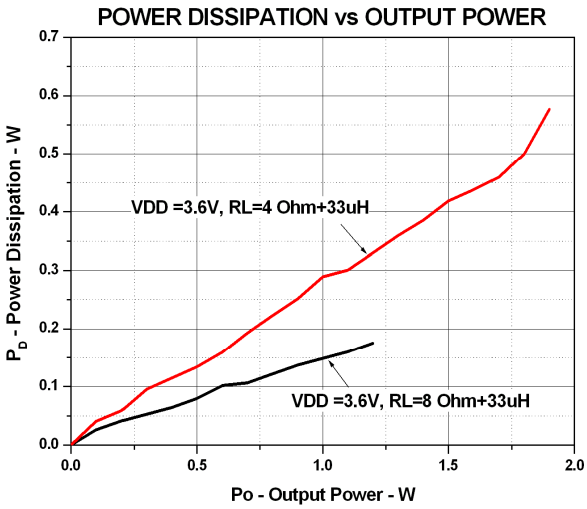


Figure6.

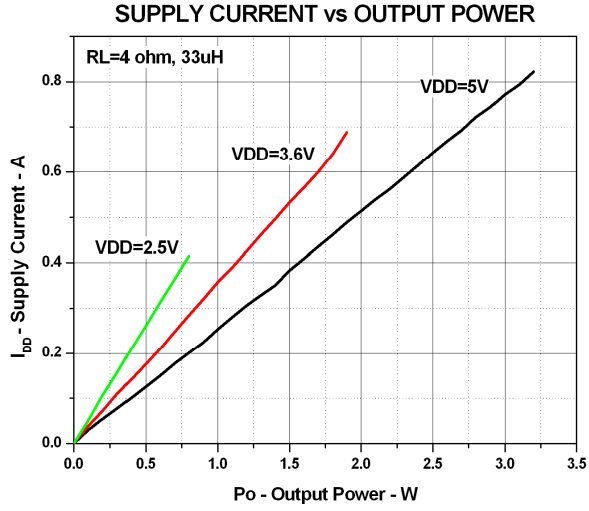


Figure7.

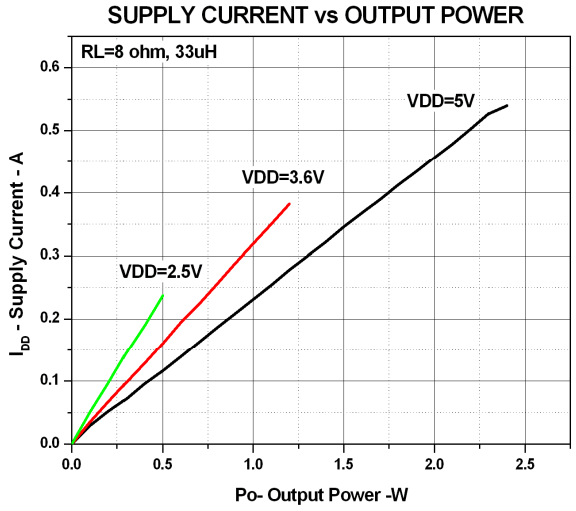


Figure8.

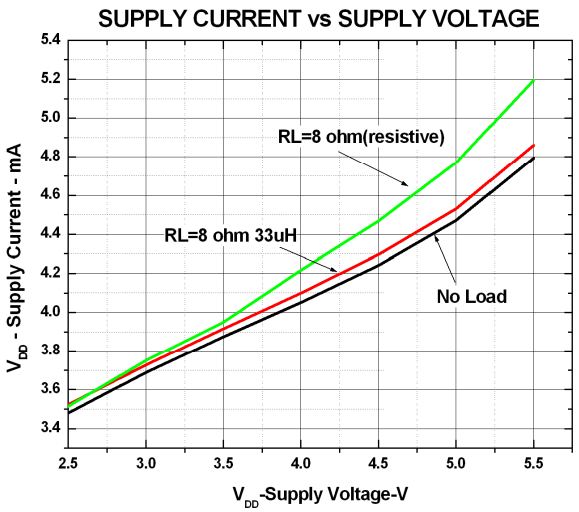


Figure9.

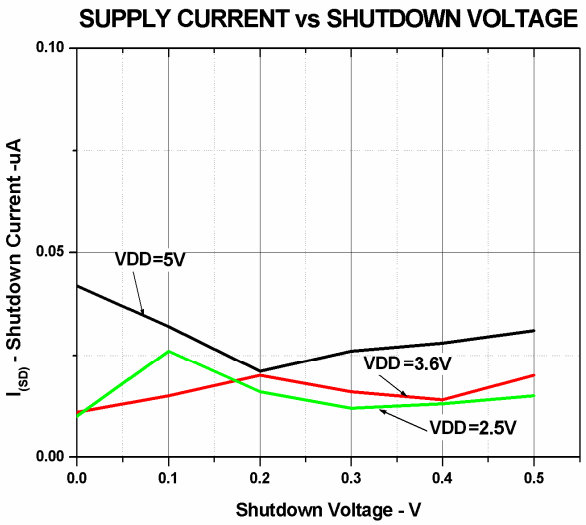


Figure10.

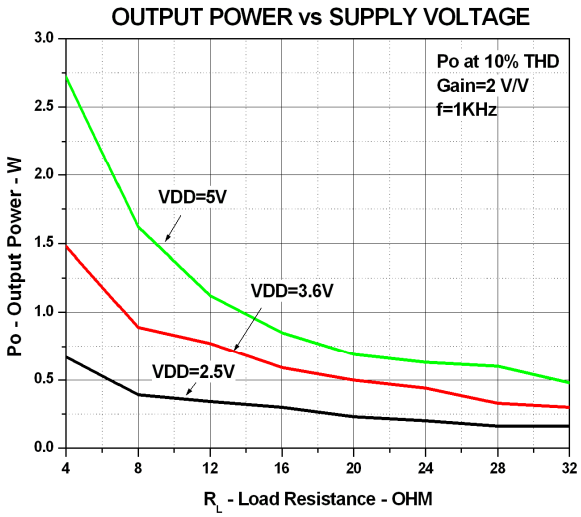


Figure11.

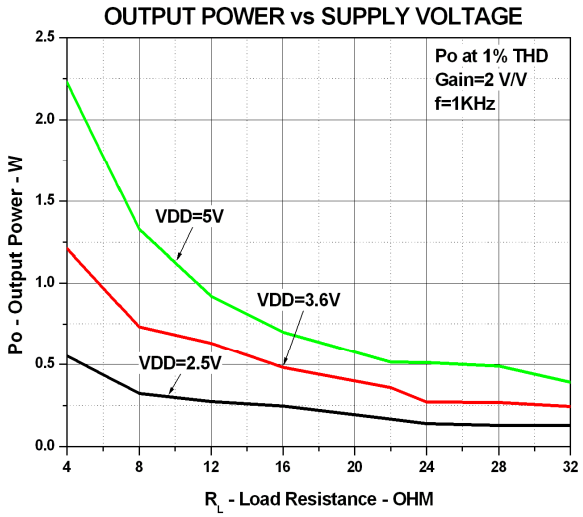


Figure12.

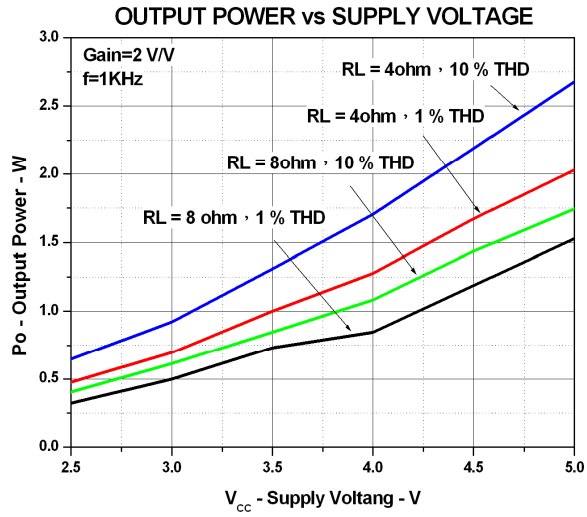


Figure13.

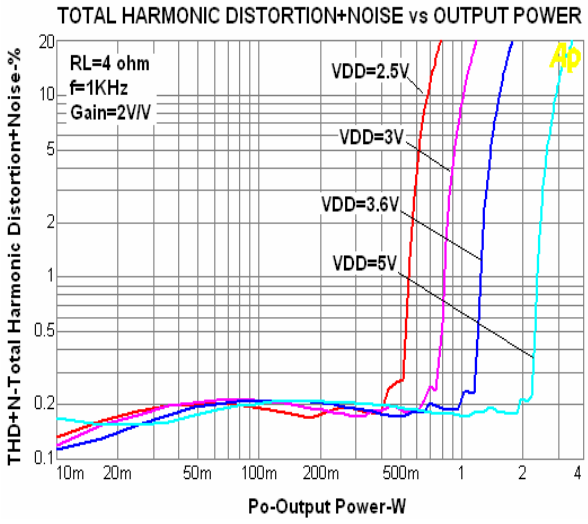


Figure14.

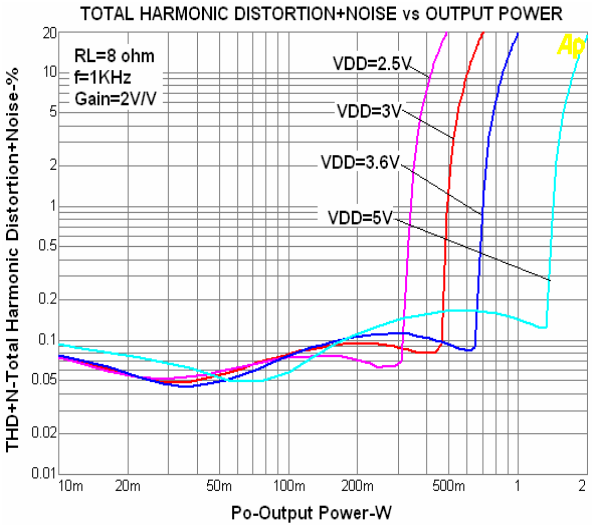


Figure15.

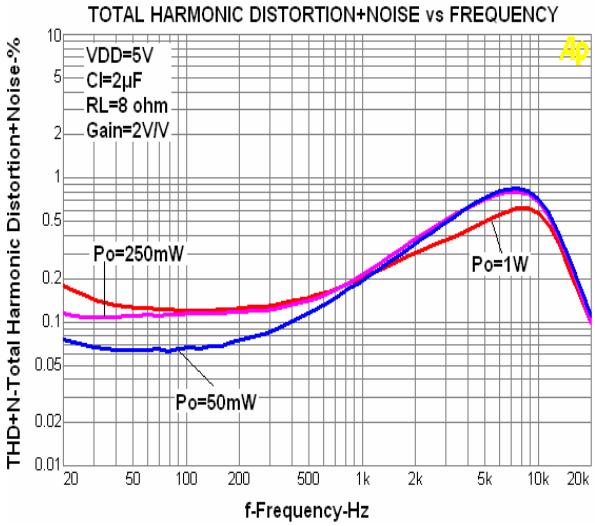


Figure16.

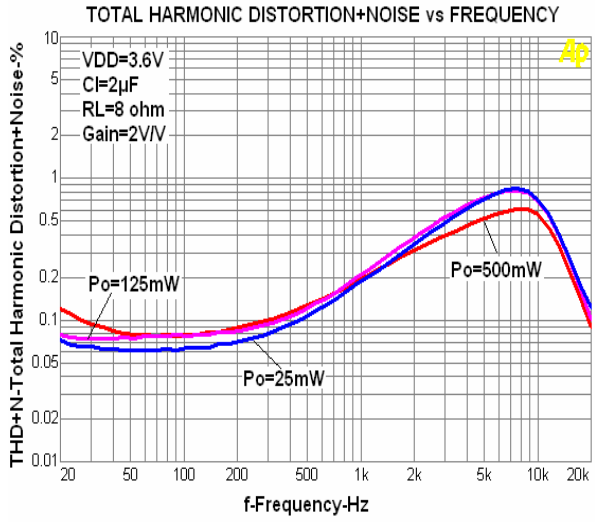


Figure17.

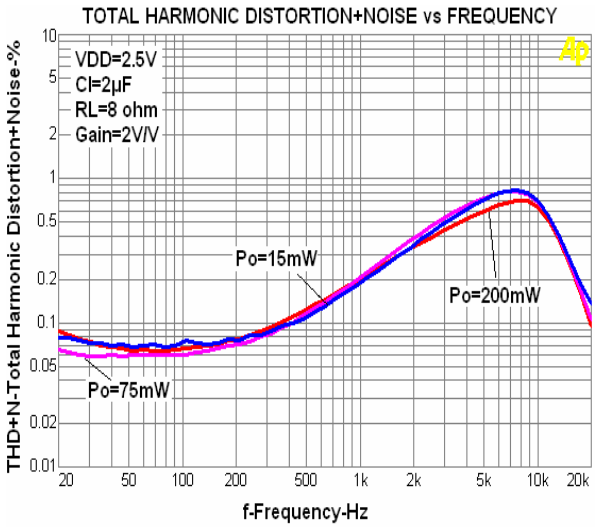


Figure18.

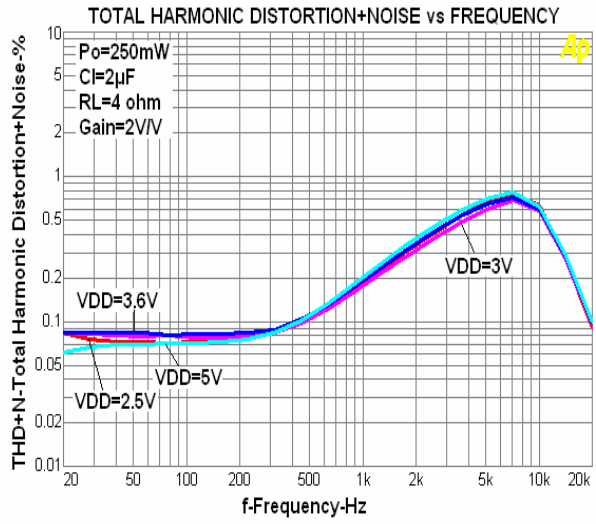


Figure19.

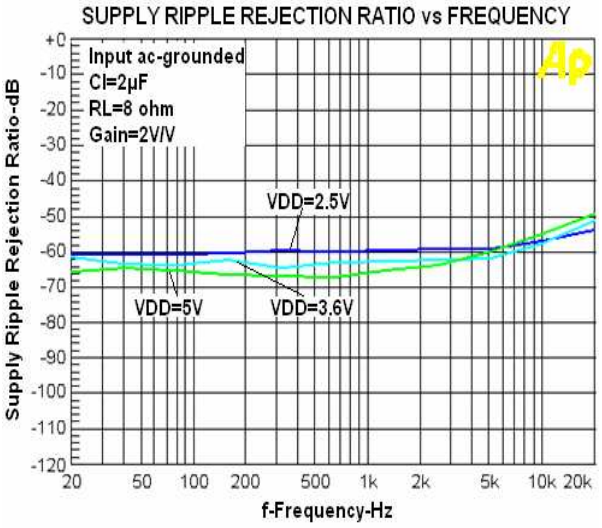


Figure20.

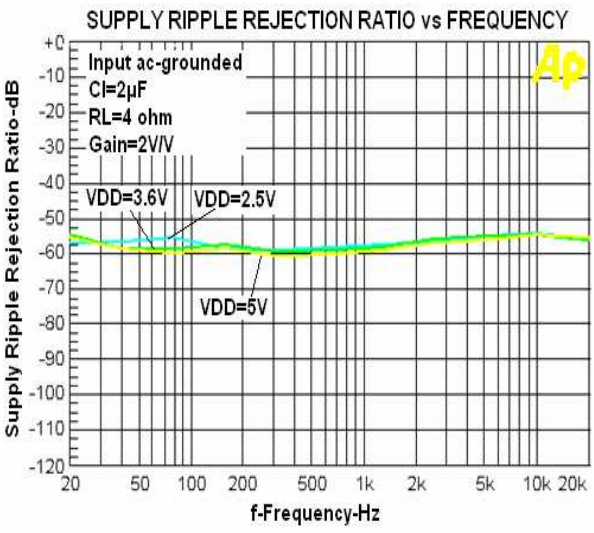


Figure21.

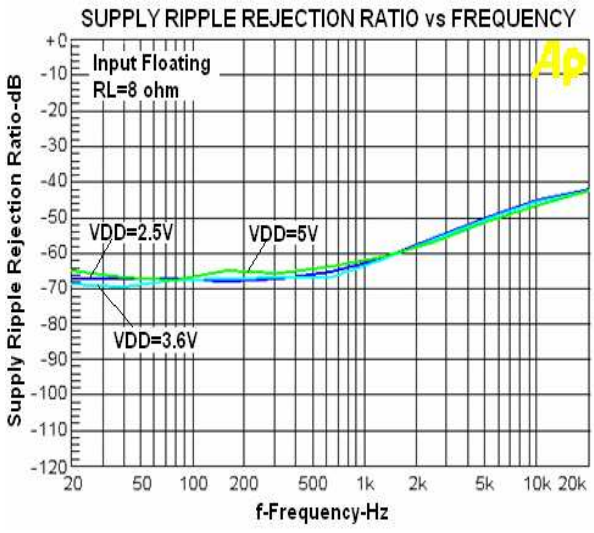


Figure22.

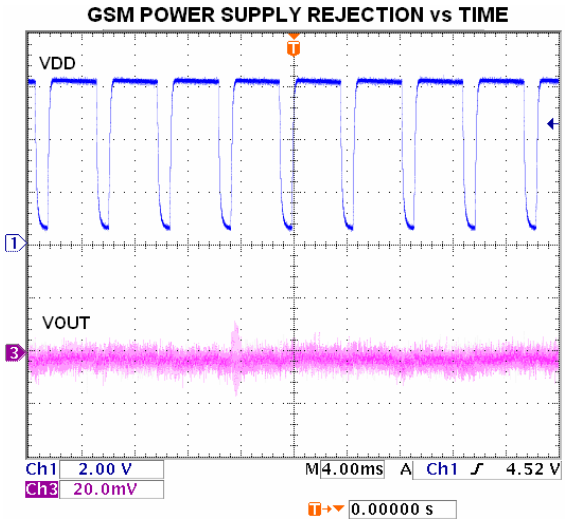


Figure23.

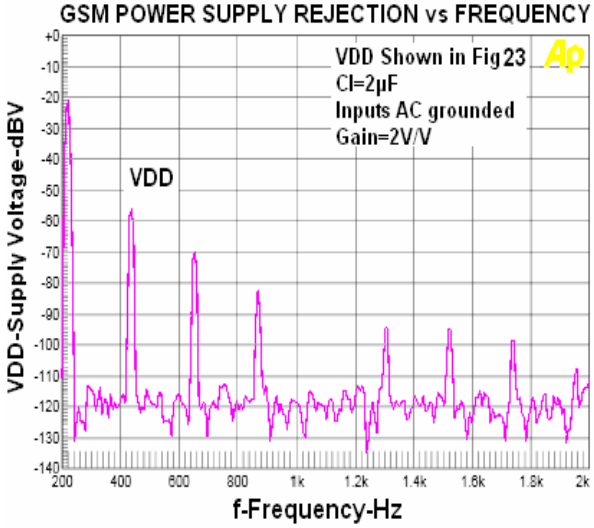


Figure24.

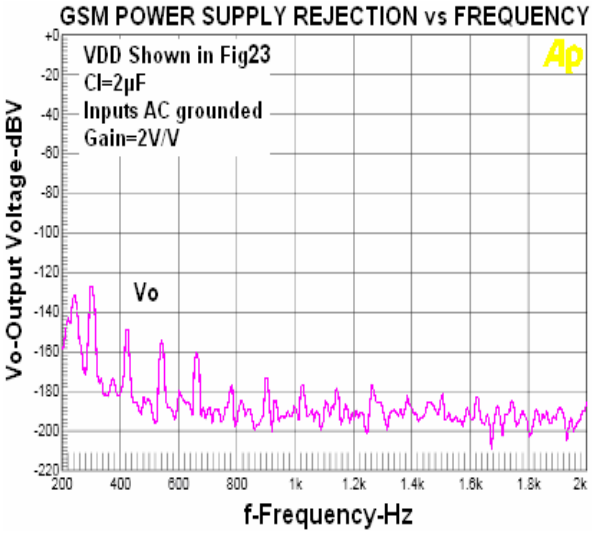


Figure25.

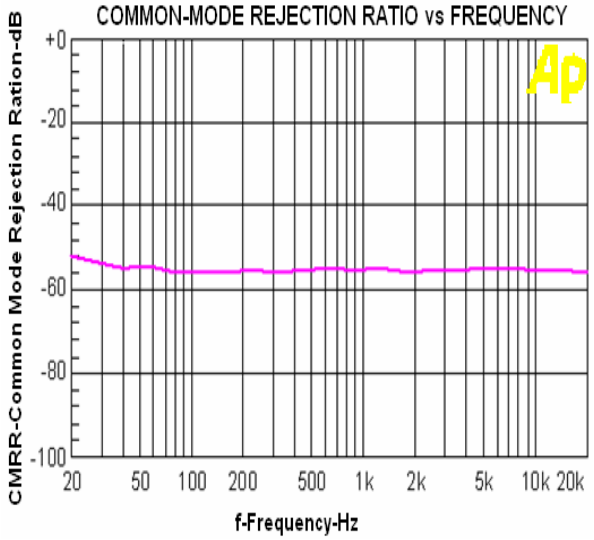


Figure26.

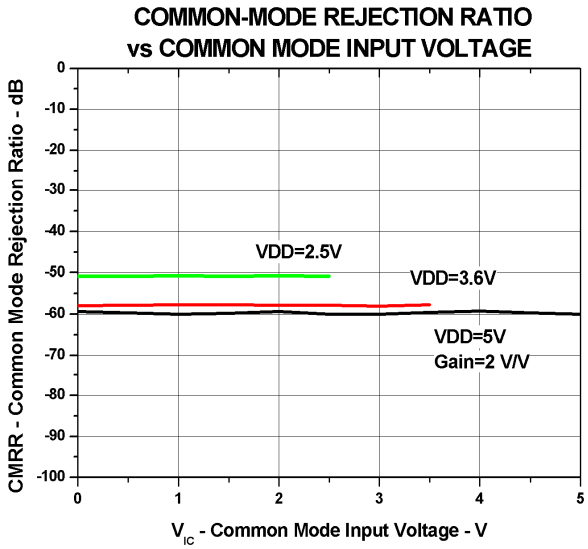


Figure27.

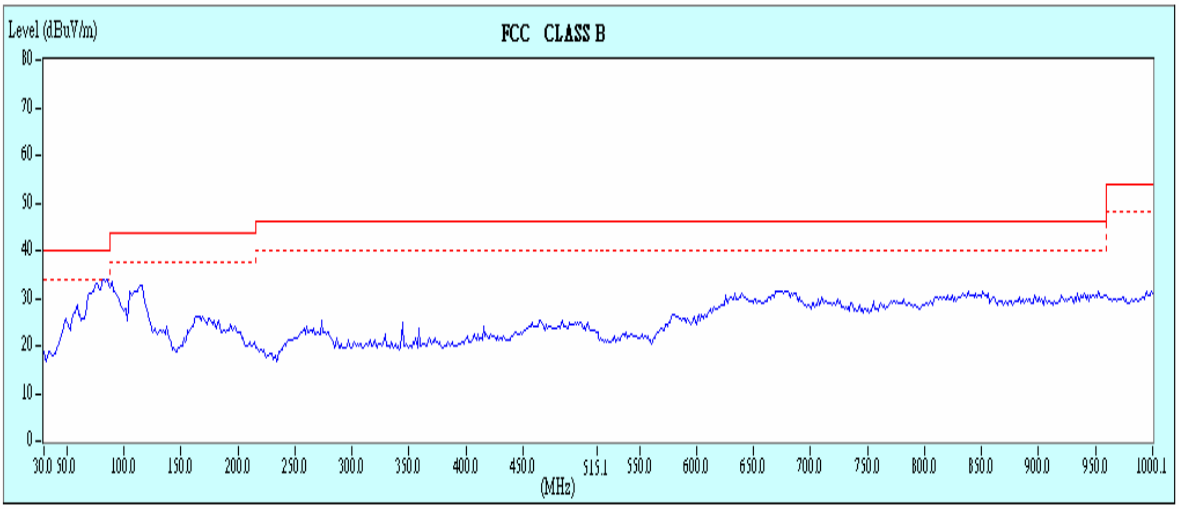


Figure28.

Application Information

Fully Differential Amplifier

The EUA2045 is a fully differential amplifier that features differential inputs and outputs. The EUA2045 also includes a common mode feedback loop that controls the output bias value to average it at $V_{DD}/2$ for any DC common mode input voltage. This allows the device to always have a maximum output voltage swing, and by consequence, maximize the output power. Moreover, as the load is connected differentially, compared to a single-ended topology, the output is four times higher for the same power supply voltage. The fully differential EUA2045 can still be used with a single-ended input; however, the EUA2045 should be used with differential inputs when in a noisy environment, like a wireless handset, to ensure maximum noise rejection.

Advantages of Fully Differential Amplifiers

The advantages of a full-differential amplifier are:

- Very high PSRR (Power Supply Rejection Ratio).
- High common mode noise rejection.
- Virtually zero pop without additional circuitry, giving an faster start-up time compared to conventional single-ended input amplifiers.
- No input coupling capacitors required thanks to common mode feedback loop.
- Midsupply bypass capacitor not required.

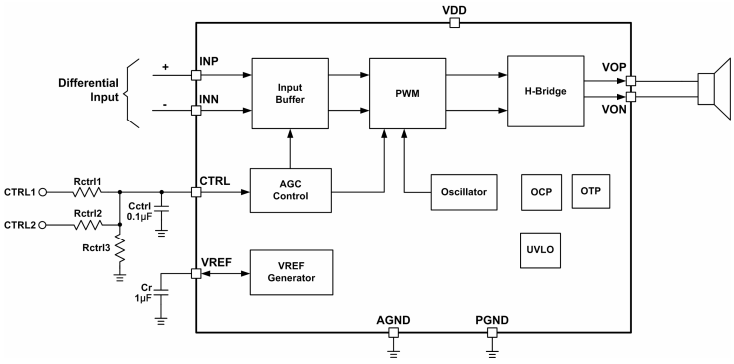


Figure 29. Differential Input Configuration

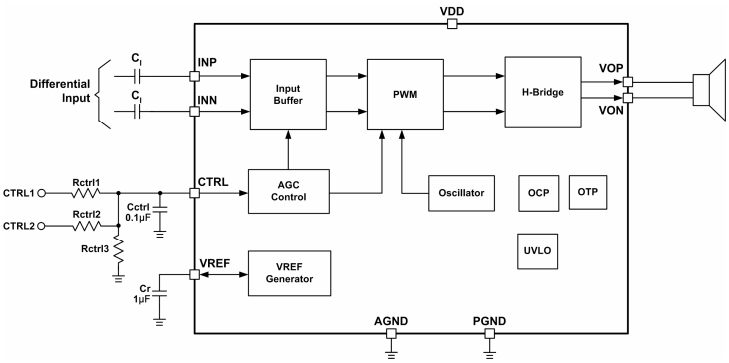


Figure 30. Differential Input Configuration and Input Capacitors

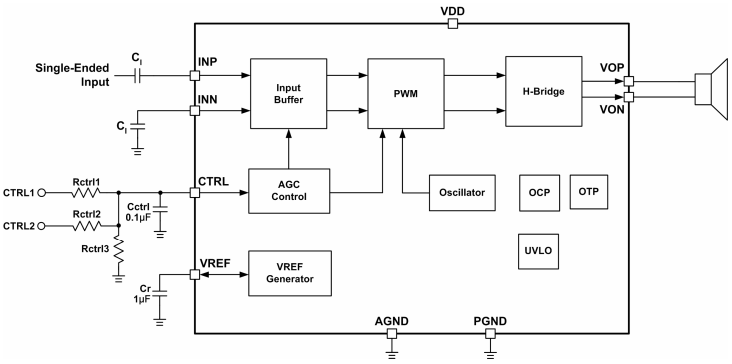


Figure 31. Single-Ended Input Configuration

Short Circuit Auto-Recovery

When a short circuit event happens, the EUA2045 goes to shutdown mode and tries to reactivate itself after few milliseconds. This auto-recovery will continue until the short circuit event is removed.

Power Supply Decoupling Capacitor (C_S)

The EUA2045 is a high-performance CMOS class-D audio amplifier that requires adequate power supply decoupling to ensure the efficiency is high and total harmonic distortion (THD) is low. For higher frequency transients, spikes, or digital hash on the line, a good low equivalent-series-resistance (ESR) ceramic capacitor, typically 1μF, placed as close as possible to the device V_{DD} lead works best. Placing this decoupling capacitor close to the EUA2045 is very important for the efficiency of the class-D amplifier, because any resistance or inductance in the trace between the device and the capacitor can cause a loss in efficiency. For filtering lower-frequency noise signals, a 10μF or greater capacitor placed near the audio power amplifier would also help.

Single-Ended Input Depop Function

In single-ended input application, there is an inherently voltage difference in input pairs when shutdown is released. In order to eliminate pop noise, the pop cancellation circuit need to charge the input capacitor C_I until fully-differential inputs are balanced and output power to load gradually.

Protection Function

EUA2045 has the following protection functions for the digital amplifier; Over-current Protection function, Thermal Protection function, and Low voltage Malfunction Prevention function.

- Over-current Protection Function

This is the function to establish the over-current protection mode when detecting a short circuit between EUA2045 differential output terminal and VSS, VDD, or another differential output. In the over current protection mode, the differential output terminal becomes a high impedance state.

The over current protection mode can be cancelled by shut down or turning on the power again.

● Thermal Protection Function

This is the function to establish the thermal protection mode when detecting excessive high temperature of EUA2045 itself. In the thermal protection mode, the differential output terminal becomes Weak Low state (a state grounded through high resistivity). And, when EUA2045 gets out of such condition, the protection mode is cancelled.

● Low voltage Malfunction Prevention function

This is the function to establish the low voltage protection mode when VDD terminal voltage becomes lower than the detection voltage (V_{UVLL}) for the low voltage malfunction prevention and to cancel the protection mode when VDD terminal voltage becomes higher than the threshold voltage (V_{UVLH}) and by return procedure form shut down for its deactivation.

(In sag state , this function works and EUA2045 becomes a low voltage protection mode.)

In the low voltage protection mode, the differential output pin becomes Weak Low state (a state grounded through high resistivity). EUA2045 will start up within the start-up time (T_{STUP}) when the low voltage protection mode is cancelled.

Control Function

● VREF terminal output

The voltage of VDD/2 is output from the VREF terminal, Capacitor (1μF) is connected between the VREF terminal and GND for stabilization.

● Shut down and Initialization function

When CTRL terminal is connected to GND potential, the IC goes to the shut-down mode. In the mode, all the circuit functions stop and its current consumption becomes the lowest. And, the output terminals become Weak Low (A high resistance grounded state).

When in the shut-down mode, the level of the terminal must not be changed from GND level during t_{SD}.

On the contrary, when CTRL terminal is set to H level, the shut-down mode is canceled and the IC starts up after startup time (t_{STUP}).

Caution :

Please start up the former source circuit first to stabilize the DC bias point (See Figure 32-②) and then cancel the shut-down state of EUA2045. The time (T_{DLY}) required to stabilize the voltage can be found by the formula (See (1) shown below). And, signal variation in the former source circuit should be a value lower than PVDD.

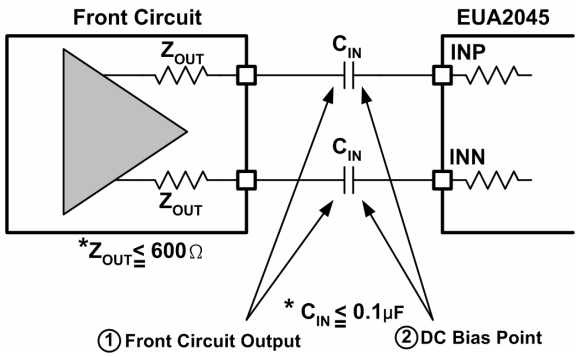


Figure 32. Circuit Diagram

$$T_{DLY} \geq C_{IN} \times 330 \times 10^{3} \times 3 \quad \text{----------(1)}$$

In order to return from the shut-down mode a desired mode needs to be set after setting both CTRL1 and CTRL2 to H level during t_{WK}. In addition, at startup, cancel the shut-down mode after supply voltages has been sufficiently stabilized.

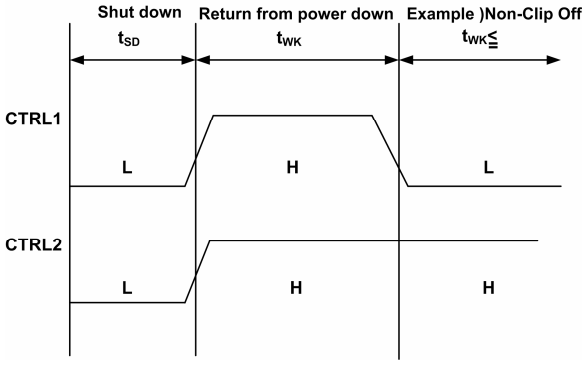


Figure 33.

● CTRL terminal function

By connection external resistors (Rctrl1, Rctrl2, and Rctrl3: Accuracy of 1%) to CTRL terminal, and impression setting threshold voltage of each mode to CTRL terminal, the followings can be set : Non-Clip 1, Non-clip2, Non-Clip OFF, and shut-down mode. When turning on the supply voltage or canceling the shut-down mode, control the CTRL terminal according to procedure for canceling shut-down (See Page6.)

Connect the terminal to the ground through a capacitor Cctrl (a ceramic capacitor of 0.1μF or more).

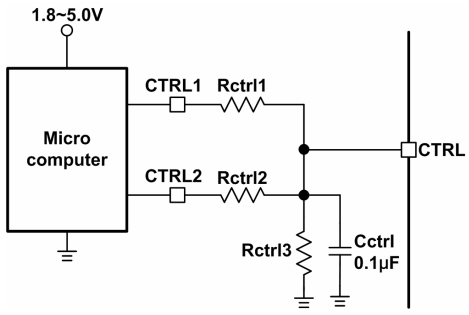


Figure 34.

CTRL1	CTRL2	Function
H	H	Non-Clip 1 mode
H	GND	Non-Clip 2 mode
GND	H	Non-Clip Off mode
GND	GND	Shut-down mode

"H" level indicates a microcomputer's I/O port H level output voltage that is input to CTRL1 and CTRL2 terminals and GND indicates GND of the microcomputer.

GND level of the microcomputer must be the same as that of EUA2045.

The control of CTRL terminal is based on I/O port H level output voltage of microcomputer that is connected.

Set resistance constants according to I/O port H level output voltage of each microcomputer as shown below.

I/O port H level output voltage of microcomputer	1.8V	2.6V	3.0V	3.3V	5.0V
Rctrl 1	27kΩ	33kΩ	33kΩ	33kΩ	56kΩ
Rctrl 2	56kΩ	68kΩ	68kΩ	68kΩ	120kΩ
Rctrl 3	82kΩ	27kΩ	22kΩ	18kΩ	15kΩ

Functions of CTRL pin are designed with their control by two control pins (CTRL1 and CTRL2).

Only a switching control between Non-Clip1 mode and Shut-down mode is available when a single control terminal is used. A setting voltage should be set according to V_{NCN1} AND V_{SD} , and use a RC filter with time constant of 1msec or more in order to eliminate noise at transmission side such as Micon etc. (Example. Rctrl=10kΩ and Cctrl=0.1μF).

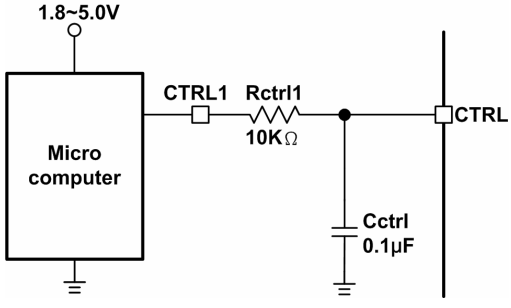


Figure 35.

CTRL1	Function
H	Non-Clip 1 mode
GND	Shut-down mode

PCB Layout

As output power increases, interconnect resistance (PCB traces and wires) between the amplifier, load and power supply create a voltage drop. The voltage loss on the traces between the EUA2045 and the load results is lower output power and decreased efficiency. Higher trace resistance between the supply and the EUA2045 has the same effect as a poorly regulated supply, increase ripple on the supply line also reducing the peak output power. The effects of residual trace resistance increases as output current increases due to higher output power, decreased load impedance or both. To maintain the highest output voltage swing and corresponding peak output power, the PCB traces that connect the output pins to the load and the supply pins to the power supply should be as wide as possible to minimize trace resistance.

The use of power and ground planes will give the best THD+N performance. While reducing trace resistance, the use of power planes also creates parasite capacitors that help to filter the power supply line.

The inductive nature of the transducer load can also result in overshoot on one or both edges, clamped by the parasitic diodes to GND and V_{DD} in each case. From an EMI stand- point, this is an aggressive waveform that can radiate or conduct to other components in the system and cause interference. It is essential to keep the power and output traces short and well shielded if possible. Use of ground planes, beads, and micro-strip layout techniques are all useful in preventing unwanted interference.

As the distance from the EUA2045 and the speaker increase, the amount of EMI radiation will increase since the output wires or traces acting as antenna become more efficient with length. What is acceptable EMI is highly application specific.

Ferrite bead and capacitance placed close to the EUA2045 may be needed to reduce EMI radiation. Select a ferrite bead with the high impedance around 100MHz and a very low DCR value in the audio frequency range is the best choice. The MPZ1608S221A1 from TDK is a good choice.

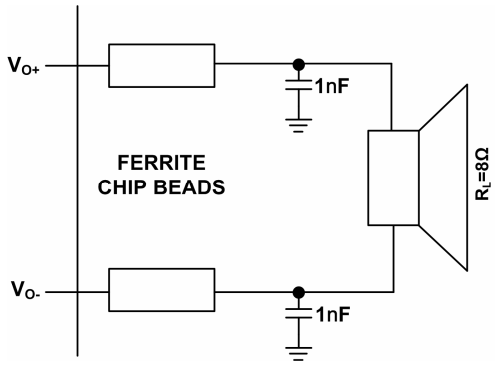
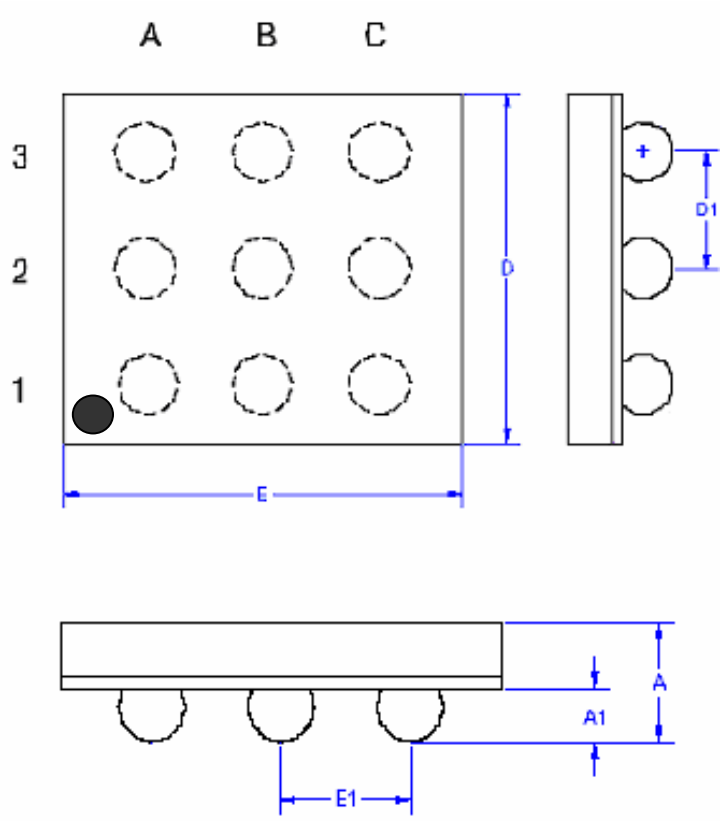


Figure 36. Optional EMI Ferrite Bead Filter

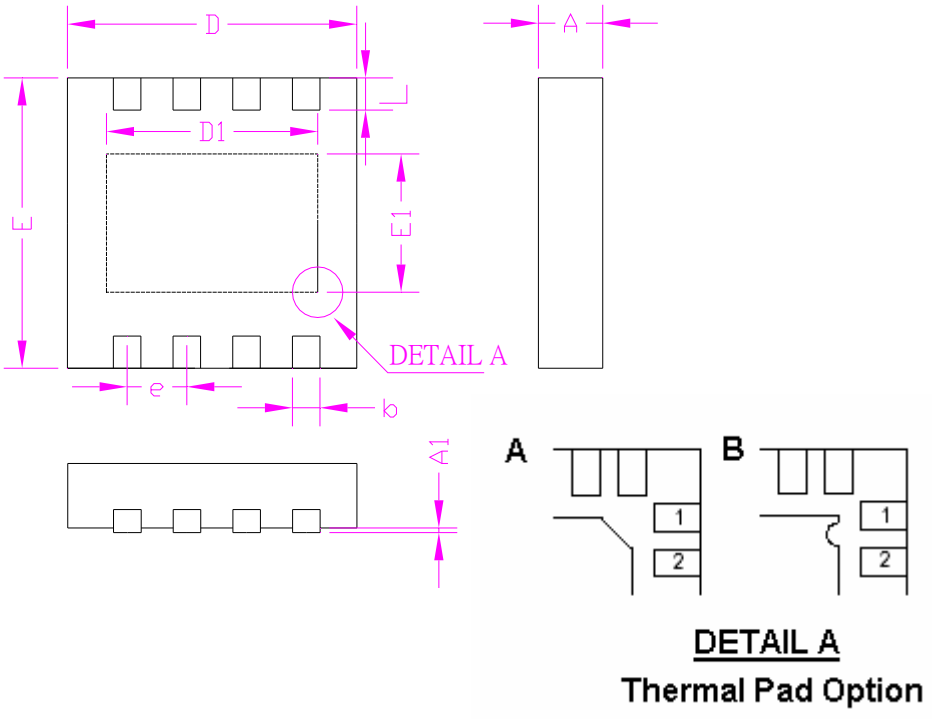
Packaging Information

WCSP-9



SYMBOLS	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A	-	0.675	-	0.027
A1	0.15	0.35	0.006	0.014
D	1.45	1.55	0.057	0.061
D1	0.50		0.020	
E	1.45	1.55	0.057	0.061
E1	0.50		0.020	

TDFN-8



SYMBOLS	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A	0.70	0.80	0.028	0.031
A1	0.00	0.05	0.000	0.002
b	0.20	0.40	0.008	0.016
D	2.90	3.10	0.114	0.122
D1	1.90	2.35	0.075	0.093
E	2.90	3.10	0.114	0.122
E1	1.50	1.75	0.059	0.069
e	0.65		0.026	
L	0.25	0.45	0.010	0.018