



STV82x7

Digital Audio Decoder/Processor for A2 and NICAM Television/Video Recorders

PRELIMINARY DATA

Key Features

■ Full-Automatic Multi-Standard Demodulation

- B / G / I / L / M / N / D / K Standards
- Mono AM and FM
- FM 2-Carrier (German and Korean Zweiton) and NICAM

■ Multi-Channel Capability

- 3 I²S digital inputs, S/PDIF (in/out)
- 5.1 analog outputs
- Dolby® Pro Logic®
- Dolby® Pro Logic II®

■ Sound Processing

- ST royalty-free processing: ST WideSurround, ST OmniSurround, ST Dynamic Bass, SRS® WOW™, SRS® TruSurround XT™ which is Virtual Dolby® Surround and Virtual Dolby® Digital compliant
- Independent Volume / Balance for Loudspeakers and Headphone
- Loudspeakers: Smart Volume Control (SVC), 5-band equalizer and loudness
- Headphone: Smart Volume Control (SVC), Bass-Treble, Loudness and SRS® TruBass™

■ Analog Audio Matrix

- 4 stereo inputs
- 3 stereo outputs
- THRU mode

■ Audio Delay for Audio Video Synchronization

- Embedded stereo delay up to 120 ms for lip-sync function (up to 180 ms for tuner input)
- Independent delay on headphone and loudspeaker channels

The STV82x7 family, based on audio digital signal processors (DSP), performs high quality and advanced dedicated digital audio processing. These devices provide all of the necessary resources for automatic detection and demodulation of analog audio transmissions for European and Asian terrestrial TV broadcasts.

Virtual or true, multi-channel capabilities and easy digital links make them ideal for digital audio low cost consumer applications. Starting from enhanced stereo up to independent control of 5 loudspeakers and a subwoofer (5.1 channels), the STV82x7 family offers standard and advanced features plus sound enhancements, spatial and virtual effects to enhance television viewer comfort and entertainment.

Typical Applications

- Analog and digital TV with virtual surround sound
- Analog and digital TV with multi-channel surround sound
- DVD and HDD recorders
- "Palm size" portable TV

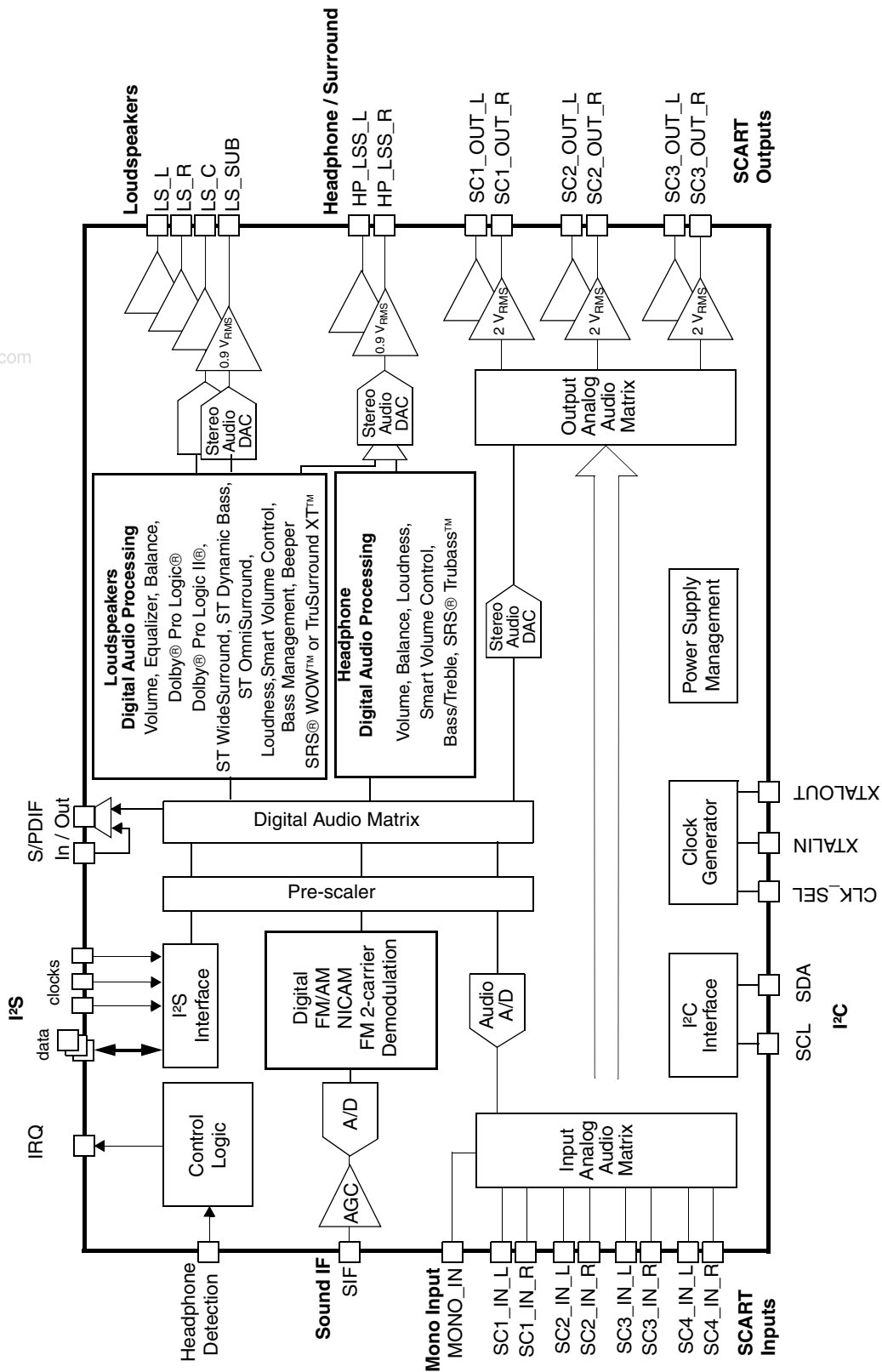


© 2004 SRS Labs, Inc. All rights reserved, SRS and the SRS logo are registered trademarks of SRS Labs, Inc.



"Dolby", "Pro Logic", and the double-D symbol are trademarks of Dolby Laboratories.

Block Diagram



www.DataSheet4U.com

Table of Contents

| | | |
|------------------|---|-----------|
| Chapter 1 | General Description | 6 |
| 1.1 | STV82x7 Overview | 8 |
| 1.1.1 | Core Features | 8 |
| 1.1.2 | Software Information | 9 |
| 1.1.3 | Device Input Modes | 9 |
| 1.1.4 | Electrical Features | 10 |
| 1.2 | Typical Applications | 10 |
| 1.3 | Pin Descriptions and Application Diagrams | 14 |
| Chapter 2 | System Clock | 20 |
| Chapter 3 | Digital Demodulator | 21 |
| 3.1 | Sound IF Signal | 21 |
| 3.2 | Demodulation | 22 |
| Chapter 4 | Dedicated Digital Signal Processor (DSP) | 24 |
| 4.1 | Back-end Processing | 24 |
| 4.2 | Audio Processing | 25 |
| 4.3 | ST WideSurround | 28 |
| 4.4 | ST OmniSurround | 28 |
| 4.5 | Dolby Pro Logic II Decoder | 28 |
| 4.6 | Bass Management | 28 |
| 4.6.1 | Bass Management Configuration 0 | 29 |
| 4.6.2 | Bass Management Configuration 1 | 30 |
| 4.6.3 | Bass Management Configuration 2 | 31 |
| 4.6.4 | Bass Management Configuration 3 | 32 |
| 4.6.5 | Bass Management Configuration 4 | 33 |
| 4.7 | SRS WOW and TruSurround XT | 33 |
| 4.7.1 | SRS TruSurround | 33 |
| 4.7.2 | SRS WOW | 34 |
| 4.8 | Smart Volume Control (SVC) | 34 |
| 4.9 | ST Dynamic Bass | 35 |
| 4.10 | 5-Band Audio Equalizer | 35 |
| 4.11 | Bass/Treble Control | 35 |
| 4.12 | Automatic Loudness Control | 36 |
| 4.13 | Volume/Balance Control | 36 |
| 4.14 | Soft Mute Control | 37 |

| | | |
|-------------------|---|-----------|
| 4.15 | Beeper | 37 |
| Chapter 5 | Analog Audio Matrix (In / Out) | 39 |
| Chapter 6 | I²S Interface (In / Out) | 40 |
| 6.1 | I ² S Inputs | 40 |
| 6.2 | I ² S Output | 41 |
| Chapter 7 | S/PDIF Input/Output | 42 |
| Chapter 8 | Power Supply Management | 43 |
| 8.1 | Standby Mode (Loop-through mode) | 43 |
| Chapter 9 | Additional Controls and Flag | 44 |
| 9.1 | Headphone Detection | 44 |
| 9.2 | IRQ Generation | 44 |
| 9.3 | I ² C Bus Expander | 44 |
| Chapter 10 | STV82x7 Reset | 45 |
| Chapter 11 | I²C Interface | 46 |
| 11.1 | I ² C Address and Protocol | 46 |
| 11.2 | Start-up and Configuration Change Procedure | 47 |
| Chapter 12 | Register List | 48 |
| 12.1 | I ² C Register Map | 49 |
| 12.2 | STV82x7 General Control Registers | 55 |
| 12.3 | Clocking 1 | 56 |
| 12.4 | Demodulator | 59 |
| 12.5 | Demodulator Channel 1 | 62 |
| 12.6 | Demodulator Channel 2 | 66 |
| 12.7 | NICAM Registers | 71 |
| 12.8 | Stereo Mode | 73 |
| 12.9 | Analog Control | 74 |
| 12.10 | Clocking 2 | 76 |
| 12.11 | DSP Control | 77 |

| | | |
|-------------------|--|------------|
| 12.12 | Automatic Standard Recognition | 81 |
| 12.13 | Audio Preprocessing and Selection Registers | 85 |
| 12.14 | Matrixing | 93 |
| 12.15 | Audio Processing | 98 |
| 12.16 | 5-Band Equalizer / Bass-Treble for Loudspeakers | 112 |
| 12.17 | Headphone Bass-Treble | 113 |
| 12.18 | Volume | 116 |
| 12.19 | Beeper | 126 |
| 12.20 | Mute | 127 |
| 12.21 | S/PDIF | 128 |
| 12.22 | Headphone Configuration | 128 |
| 12.23 | DAC Control | 129 |
| 12.24 | AutoStandard Coefficients Settings | 130 |
| Chapter 13 | Electrical Characteristics | 132 |
| 13.1 | Absolute Maximum Ratings | 132 |
| 13.2 | Thermal Data | 132 |
| 13.3 | Power Supply Data | 132 |
| 13.4 | Crystal Oscillator | 133 |
| 13.5 | Analog Sound IF Signal | 133 |
| 13.6 | SIF to I ² S Output Path Characteristics | 134 |
| 13.7 | SCART to SCART Analog Path Characteristics | 134 |
| 13.8 | SCART and MONO IN to I ² S Path Characteristics | 135 |
| 13.9 | I ² S to LS/HP/SUB/C Path Characteristics | 135 |
| 13.10 | I ² S to SCART Path Characteristics | 136 |
| 13.11 | MUTE Characteristics | 136 |
| 13.12 | Digital I/Os Characteristics | 136 |
| 13.13 | I ² C Bus Characteristics | 137 |
| 13.14 | I ² S Bus Interface | 138 |
| Chapter 14 | Input/Output Groups | 140 |
| Chapter 15 | Package Mechanical Data | 145 |
| Chapter 16 | Revision History | 146 |

1 General Description

The STV82x7 is a multistandard TV sound demodulator and audio processor which integrates **SRS® WOW™**, **SRS® TruSurround XT™**, **Dolby® Pro Logic®**, **Dolby® Pro Logic II®**, **Virtual Dolby® Surround (VDS)** and **Virtual Dolby® Digital (VDD)** capability.

ST advanced algorithms such as **ST OmniSurround**, **ST WideSurround**, **ST Dynamic Bass** are also available in this audio sound processor. **ST OmniSurround** is a certified **Dolby®** algorithm for the **Virtual Dolby® Digital (VDD)** and the **Virtual Dolby® Surround (VDS)**. When using VDD or VDS, either a **Dolby® Digital** or a **Pro Logic®** (or **Pro Logic II®**) decoder is mandatory respectively.

This chip performs **automatic multistandard analog TV stereo sound identification and demodulation** (no specific I²C programming is required). It offers various audio processing functions such as equalization, loudness, beeper, volume, balance, and surround effects. It provides a cost-effective solution for analog and digital TV designs.

The STV82x7 is perfectly suited to current and future digital TV platforms, based on audio/video digital chips (**STD2000**, **(DTV100 platform)** and the future **WorldWide iDTV one chip**) which include an internal digital decoder (**MPEG**, **Dolby® Digital...**). In the case where a **Dolby® Digital** decoder is embedded in the audio/video digital chip, **Virtual Dolby® Digital** could be obtained.

For the **CTV100/120** platform, the device is offered as an alternative solution to the first-generation chassis that uses the STV82x6.

Table 1: STV82x7 Version List

| | S T V 8 2 0 7 | S T V 8 2 1 7 | S T V 8 2 2 7 | S T V 8 2 3 7 | STV8247 | | STV8257 | | | STV8267 | | STV8277 | | | STV8287 | |
|---|---------------------------------|---------------------------------|---------------------------------|---------------------------------|--------------------------------------|--|---------------------------------|--------------------------------------|--|--------------------------------------|--|--------------------------------------|--|--------------------------------------|--|---|
| | | | | | S T V 8 2 4 7 D | S T V 8 2 4 7 D S X | S T V 8 2 5 7 | S T V 8 2 5 7 D | S T V 8 2 5 7 D S X | S T V 8 2 6 7 D | S T V 8 2 6 7 D S X | S T V 8 2 7 7 D | S T V 8 2 7 7 D S X | S T V 8 2 8 7 D | S T V 8 2 8 7 D S X | |
| Demodulation | | | | | | | | | | | | | | | | |
| AM/FM - Mono, FM 2-carrier | X | X | X | X | X | X | X | X | X | X | X | X | X | X | X | X |
| NICAM | | X | | X | X | X | X | X | X | X | X | X | X | X | X | X |
| Multi-Channel Capability | | | | | | | | | | | | | | | | |
| 3 x I ² S In or 1 I ² S Out, S/PDIF (Pass-thru) | | | | | | | X | X | X | | | X | X | X | X | X |
| 5.1 Analog Out for Loudspeakers | | | | | | | | | | X | X | X | X | X | X | X |
| Virtual Dolby® Surround | | | | | X | X | | X | X | X | X | | X | X | X | X |
| Virtual Dolby® Digital capability ¹ | | | | | | | X | X | X | | | X | X | X | X | X |
| Dolby® Pro Logic® | | | | | | | | | | X | X | | X | X | | |
| Dolby® Pro Logic II® | | | | | | | | | | | | | | | X | X |
| Audio Processing | | | | | | | | | | | | | | | | |
| SRS® WOW™ | | | X | X | | | | | | | | | | | | |
| SRS® TruSurround XT™ | | | | | | X | | | X | | X | | | X | | X |
| ST Voice, ST Dynamic Bass, ST WideSurround | X | X | X | X | X | X | X | X | X | X | X | X | X | X | X | X |
| ST OmniSurround ² | | | | | X | X | X | X | X | X | X | X | X | X | X | X |

1. Virtual Dolby Digital capability is obtained with the use of external Dolby Digital decoder (for example STD05x0).
2. When using VDD or VDS with **ST OmniSurround** or **SRS TruSurround XT™**, either a **Dolby® Digital** or a **Pro Logic®** (or **Pro Logic II®**) decoder is mandatory respectively.

Figure 1: Package Ordering Information

Order Code:
 STV82x7 (Tray)
 STV82x7/T (Tape & Reel)



For Example: STV8257DSX/T will be delivered in Tape & Reel conditioning

1.1 STV82x7 Overview

1.1.1 Core Features

- Single audio source processing:
 - IF source and/or analog stereo input (SCART)
 - one digital source with a maximum of 6 synchronous channels (5.1 is obtained across three I²S)
- SIF input signal with Automatic Gain Control (AGC)
- Digital Demodulator with automatic standard detection and demodulation for AM, FM mono, FM 2 carriers (German or Korean FM 2-carrier) and NICAM
- Audio processor working at 32 kHz, 44.1 kHz or 48 kHz with specific features:
 - For Loudspeakers (L, R, L_S, R_S, SubW, C):
 - Dolby® Pro Logic II ® Decoder with Bass Management
 - SRS® WOW™ or TruSurround XT™ including Virtual Dolby® Surround and Virtual Dolby® Digital
 - ST WideSurround
 - ST OmniSurround
 - ST Dynamic Bass
 - 5-band Equalizer or Bass-Treble
 - Loudness
 - Smart Volume Control
 - Volume/Balance/Soft-mute
 - Beeper
 - Video Processing Delay Compensation
 - For Headphone:
 - SRS® TruBass™
 - Smart Volume Control
 - Bass-Treble
 - Loudness
 - Volume/Balance/Soft-mute
 - Beeper
 - Video Processing Delay Compensation
- Shared outputs for headphone and loudspeakers (surround channels);
- Analog matrix with:
 - five external inputs:
 - four SCART inputs (2 V_{RMS} capable)
 - one analog mono input (0.5 V_{RMS})
 - one internal input from a digital matrix via a DAC
 - three external outputs (2 V_{RMS} capable)
 - one internal output for the digital matrix (using an internal ADC)
- Digital matrix with:
 - three input modes (Demodulator/SCART, SCART only and I²S)
 - three stereo outputs (Loudspeakers, Headphone and SCART)
- High-end audio DAC
- S/PDIF output for connection with an external amplifier/decoder
- Internal multiplexer for the S/PDIF output (to share the internal S/PDIF output and the S/PDIF output generated by the external decoder of the digital broadcast)

- Specific stand-by mode (Loop-through)
- Control by I²C bus (two I²C addresses)
- System PLL and Clock Generation using either a single quartz oscillator or a differential clock input

1.1.2 Software Information

The different software combinations are listed in [Table 2](#).

Table 2: Input/Output Software Configurations

| Input (Number of Channels) | Output (Number of Channels) | | |
|--|---|-------------------|---------------|
| | 2 (+1) | 4 (+1) | 5 (+1) |
| 1 | ST WideSurround or SRS® WOW™ | | |
| 2 (L and R) | ST WideSurround or SRS® WOW™ | | |
| 2 (L _T and R _T) | ST WideSurround or SRS® TruSurround XT™ or ST OmniSurround or Dolby® Pro Logic® +SRS® TruSurround XT™ or Dolby® Pro Logic® +ST OmniSurround | Dolby® Pro Logic® | |
| 4 (+1) | SRS® TruSurround XT™ or ST OmniSurround or Downmix | No processing | |
| 5 (+1) | SRS® TruSurround XT™ or ST OmniSurround or Downmix | Downmix | No processing |

Note: In addition to the above sound processing, it is always possible to add ST Voice and also ST Dynamic Bass algorithms.

Note: The SRS® TruSurround® and ST OmniSurround are approved by Dolby as Virtual Dolby Surround (VDS) and Virtual Dolby Digital (VDD).

The SRS® TruSurround XT™ system is composed of:

- SRS® TruSurround®
- SRS® WOW™

The SRS® WOW™ system also includes:

- SRS® Dialog Clarity™
- SRS® TruBass™

1.1.3 Device Input Modes

- Demodulator and SCART Mode (with output $f_S = 32$ kHz)
- SCART Only Mode (with output $f_S = 48$ kHz)
- I²S Mode (with output $f_S = 32, 44.1$ or 48 kHz)

- External audio input interface using 3 x I²S (for decoded streams such as Dolby® Digital and/or standard stereo streams)

1.1.4 Electrical Features

Multi Power Supply: 1.8 V, 3.3 V and 8 V.

Power Consumption:

- lower than 1 W in Functional mode (full features)
- 200 mW in Loop-through mode corresponding to Switch-off of all digital blocks

1.2 Typical Applications

The STV82x7 is specified to enable flexible, analog and digital TV chassis design (refer to [Figure 2](#), [Figure 3](#), [Figure 4](#) and [Figure 5](#)).

The main considerations are:

- all necessary connections between devices can be provided through the TV set,
- pseudo stand-by mode used to copy to VCR or the DVD sources when the TV set is OFF,
- possible application compatibility with STV82x6 (TQFP80 package) TV design,
- pin-to-pin compatibility with STV82x8 (TQFP80 package) TV design.

The STV82x7 is used to process a single audio source (analog or digital). However, it is possible to process two audio sources simultaneously using an STV82x7 interconnection (two chips can be easily connected).

In the case of a single audio source, it is possible to hear and record in the same time: the same audio stream can be simultaneously output on headphone, loudspeakers, S/PDIF and the SCART connectors.

Note: *Headphone and loudspeakers can be used simultaneously for dual-language purposes or for different sound settings (e.g. volume). In this case, certain restrictions occur (see [Section 4.2: Audio Processing](#)).*

For more connections, the SCART-to-SCART path can be used. The use of these full analog paths implies that the sound is not digitally processed.

Figure 2: STV8237 Typical Application (Enhanced Stereo)

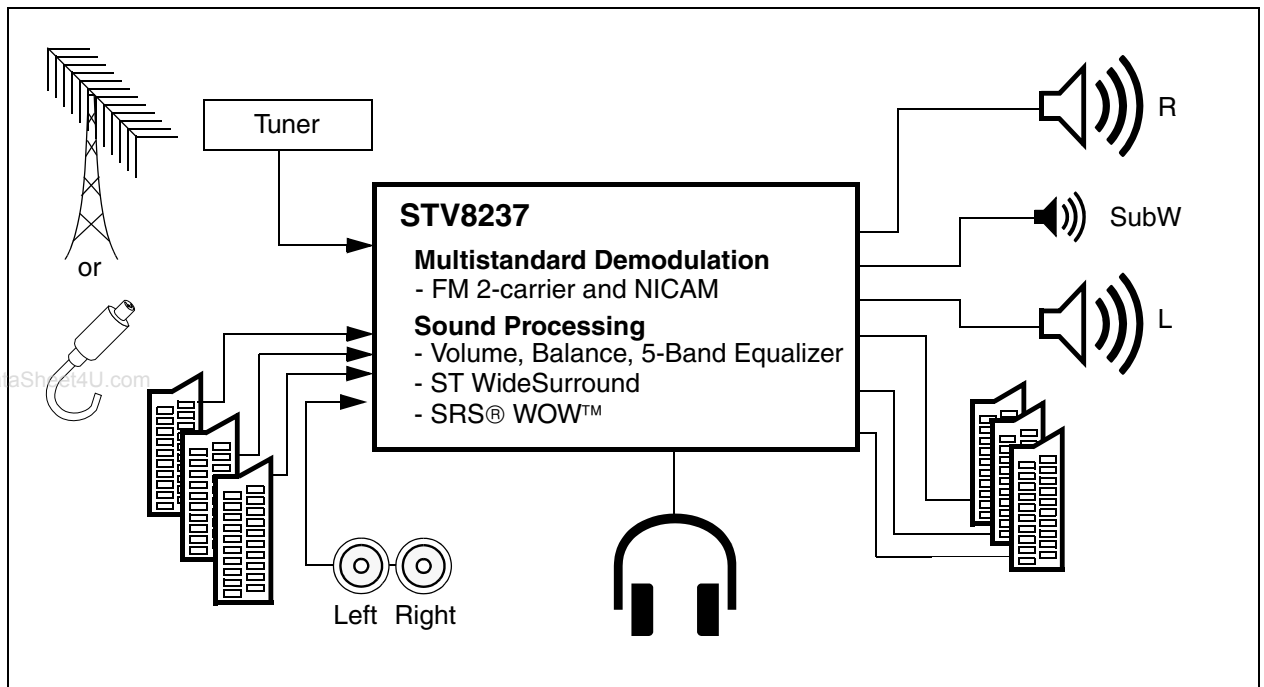


Figure 3: STV8247 Typical Application (Analog Virtual Sound)

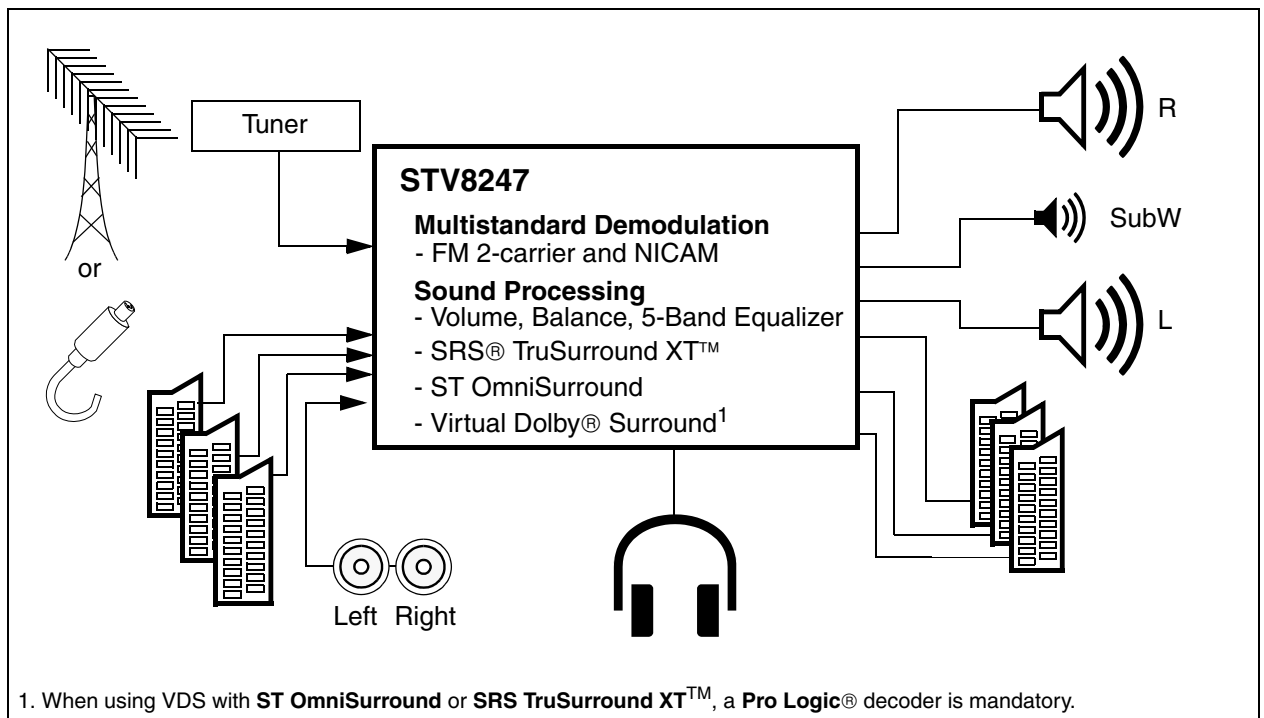


Figure 4: STV8257 Typical Application (Digital: Virtual Sound)

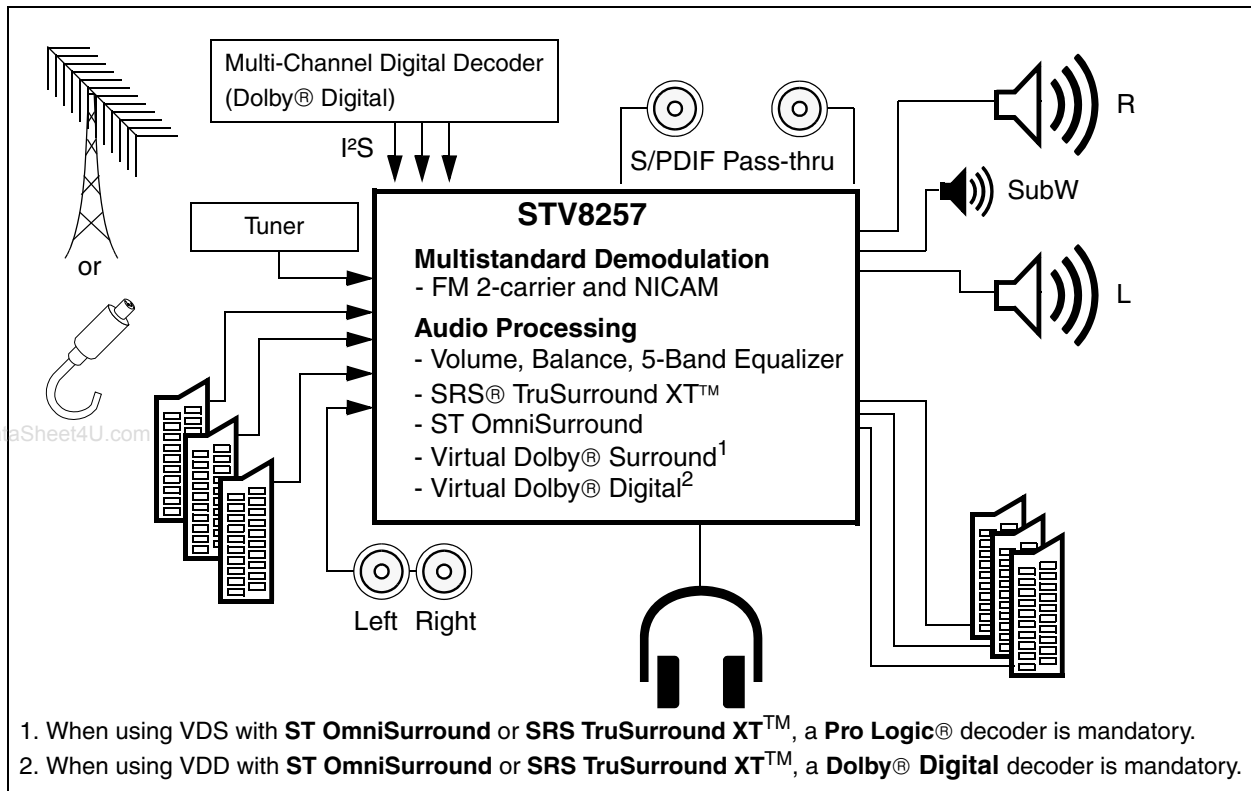


Figure 5: STV8277 Typical Application (Digital TV: Multi-Channel and Virtual Sound)

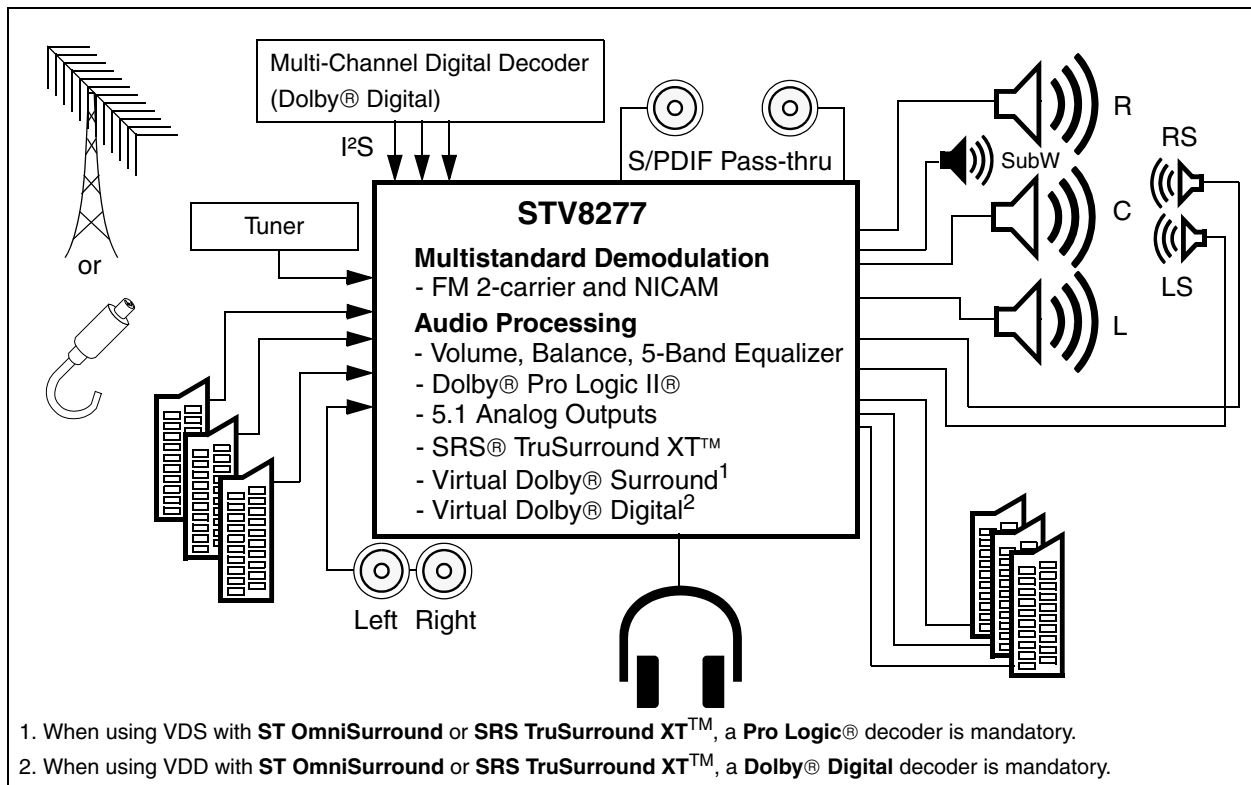
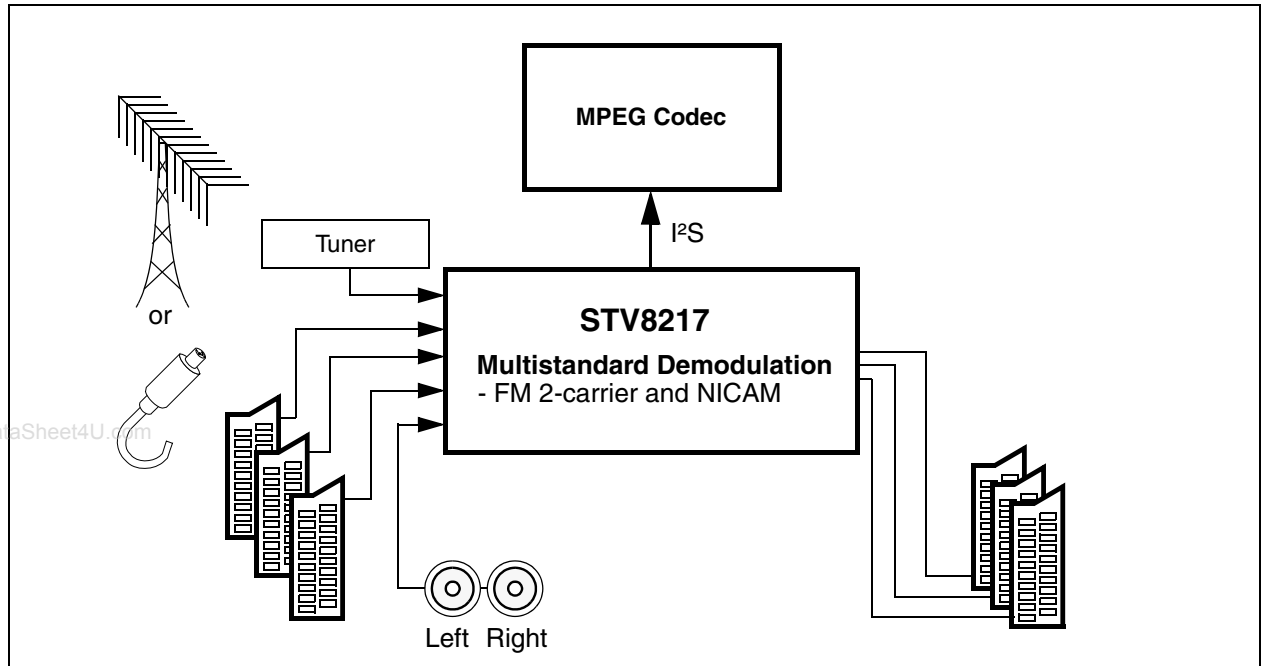


Figure 6: STV8217 Typical Application (Digital Recorder)



1.3 Pin Descriptions and Application Diagrams

- AP = Analog Power
- DP = Digital Power
- I = Input
- O = Output
- OD = Open-Drain
- B = Bi-Directional
- A = Analog

Table 3: TQFP80 Pin Description (Sheet 1 of 3)

| Pin No. | STV82x7 Pin Name | Type (STV82x7) | Function for STV82x7 (Function for STV82x6 in italic characters) | STV82x6 Pin Name |
|---------|------------------|----------------|--|----------------------------|
| 1 | SC1_OUT_L | A | SCART1 Audio Output Left | AO1L |
| 2 | SC1_OUT_R | A | SCART1 Audio Output Right | AO1R |
| 3 | VCC_H | AP | 8V Power for Audio I/O & ESD | <i>Not connected</i> |
| 4 | GND_H | AP | High Current Ground for Audio Outputs | <i>Connected to Ground</i> |
| 5 | SC3_OUT_L | A | SCART3 Audio Output Left | <i>Not connected</i> |
| 6 | SC3_OUT_R | A | SCART3 Audio Output Right | <i>Not connected</i> |
| 7 | VCC33_SC | AP | 3.3V Power for Audio Buffers & DAC / ADC | VDDC |
| 8 | GND33_SC | AP | Ground for Audio Buffers & DAC / ADC | GNDC |
| 9 | SC1_IN_L | A | SCART1 Audio Input Left | AI1L |
| 10 | SC1_IN_R | A | SCART1 Audio Input Right | AI1R |
| 11 | VREFA | A | Audio Bias Voltage Decoupling 1.55V (Switched V_{REF} decoupling pin for Audio Converters (VMCP)) | VMC1 |
| 12 | GND_SA | AP | Ground for DACs | <i>Connected to Ground</i> |
| 13 | VBG | A | Bandgap Voltage Reference Decoupling 1.2V (V_{REF} decoupling pin for Audio Converters (VMC)) | VMC2 |
| 14 | SC2_IN_L | A | SCART2 Audio Input Left | AI2L |
| 15 | SC2_IN_R | A | SCART2 Audio Input Right | AI2R |
| 16 | VCC33_LS | AP | 3.3V Power for Audio DACs (3.3V Power Supply for Audio Buffers and SCART) | VDDA |
| 17 | GND33_LS | AP | Ground for Audio DACs (Ground for Audio Buffers and SCART) | GNDAH |
| 18 | SC2_OUT_L | A | SCART2 Audio Output Left | AO2L |
| 19 | SC2_OUT_R | A | SCART2 Audio Output Right | AO2R |
| 20 | VCC_NISO | AP | Polarization of the NISO (connected to 3.3V) (8V / 5V Power supply for SCART & Audio buffers) | VDDH |
| 21 | VSS33_CONV | AP | Ground for DAC 1.8 to 3.3V Converters | <i>Connected to Ground</i> |
| 22 | VDD33_CONV | AP | 3.3V Power for DAC 1.8 to 3.3V Converters (Voltage Reference for Audio buffers) | VREFA |

Table 3: TQFP80 Pin Description (Sheet 2 of 3)

| Pin No. | STV82x7 Pin Name | Type (STV82x7) | Function for STV82x7 (Function for STV82x6 in italic characters) | STV82x6 Pin Name |
|---------|------------------|----------------|--|----------------------------|
| 23 | SC3_IN_L | A | SCART3 Audio Input Left | AI3L |
| 24 | SC3_IN_R | A | SCART3 Audio Input Right | AI3R |
| 25 | SCL_FLT | A | SCART Filtering Left | <i>Not connected</i> |
| 26 | SCR_FLT | A | SCART Filtering Right (<i>Bandgap Voltage Source Decoupling</i>) | BGAP |
| 27 | LS_C | A | Center Output | <i>Not connected</i> |
| 28 | LS_L | A | Left Loudspeaker Output | LSL |
| 29 | LS_R | A | Right Loudspeaker Output | LSR |
| 30 | LS_SUB | A | Subwoofer Output | SW |
| 31 | HP_LSS_L | A | Left Headphone Output or Left Surround Output | HPL |
| 32 | HP_LSS_R | A | Right Headphone Output or Right Surround Output | HPR |
| 33 | VSS18_CONV | DP | Ground for Digital part of the DAC/ADC (<i>Substrate Analog/Digital Shield</i>) | GNDSA |
| 34 | VDD18_CONV | DP | 1.8V Power for Digital part of the DAC/ADC | <i>Not connected</i> |
| 35 | HP_DET | I | Headphone Detection | HPD |
| 36 | ADR_SEL | I | Hardware Address selection for I ² C Bus | ADR |
| 37 | VSS18 | DP | Ground for Digital part | <i>Connected to Ground</i> |
| 38 | VDD18 | DP | 1.8V Power for Digital part | <i>Not connected</i> |
| 39 | SCL | OD | I ² C Clock Input | SCL |
| 40 | SDA | OD | I ² C Data I/O | SDA |
| 41 | VSS18 | DP | Ground for Digital part | <i>Connected to Ground</i> |
| 42 | VDD18 | DP | 1.8V Power for Digital part (<i>5V Power Regulator Control</i>) | REG |
| 43 | RST | I | Main Reset Input | RESET |
| 44 | S/PDIF_IN | I | Serial Audio Data Input (<i>System Clock output</i>) | SYSCK |
| 45 | S/PDIF_OUT | O | Serial Audio Data Output (<i>I²S Master Clock output</i>) | MCK |
| 46 | VDD33_IO1 | DP | 3.3V Power for Digital part | VDD1 |
| 47 | VSS33_IO1 | DP | Ground for Digital part | GND1 |
| 48 | CK_TST_CTRL | D | To be Grounded | <i>Not connected</i> |
| 49 | VSS18 | DP | Ground for Digital part | GNDSP |
| 50 | VDD18 | DP | 1.8V Power for Digital part | <i>Not connected</i> |
| 51 | CLK_SEL | I | Clock Input Format Selection | <i>Not connected</i> |
| 52 | XTALIN_CLKXTP | I | Crystal Oscillator Input or Differential Input Positive (<i>Crystal Oscillator Input</i>) | XTI |

Table 3: TQFP80 Pin Description (Sheet 3 of 3)

| Pin No. | STV82x7 Pin Name | Type (STV82x7) | Function for STV82x7 (Function for STV82x6 in italic characters) | STV82x6 Pin Name |
|---------|------------------|----------------|--|----------------------------|
| 53 | XTALOUT_CLKXTM | O | Crystal Oscillator Output or Differential Input Negative (<i>Crystal Oscillator Output</i>) | XTO |
| 54 | VCC18_CLK1 | AP | 1.8V Power for Clock PLL Analog & Crystal Oscillator 1/2 (<i>3.3V Power supply for Analog PLL Clock</i>) | VDDP |
| 55 | GND18_CLK1 | AP | Ground for Clock PLL Analog & Crystal Oscillator 1/2 | GNDP |
| 56 | GND18_CLK2 | AP | Ground for Clock PLL Digital 1/2 | GND2 |
| 57 | VCC18_CLK2 | DP | 1.8V Power for Clock PLL Digital 1/2 (<i>3.3V Power supply for Digital core, DSPs & IO Cells</i>) | VDD2 |
| 58 | VSS33_IO2 | DP | Ground for Digital IO pins 60 to 69 | <i>Connected to Ground</i> |
| 59 | VDD33_IO2 | DP | 3.3V power for Digital IO pins 60 to 69 | <i>Not connected</i> |
| 60 | I2S_PCM_CLK | I/O | I ² S Slave Clock Input/Output Channel 1, 2 & 3 | <i>Not connected</i> |
| 61 | I2S_SCLK | I/O | I ² S Clock Input/Output Channel 1, 2 & 3 (I ² S bus data output) | SDO |
| 62 | I2S_LR_CLK | I/O | I ² S Word Select Input/Output Channel 1,2 & 3 (<i>Stereo Detection output / I²S Bus Data input</i>) | ST/SDI |
| 63 | I2S_DATA0 | I/O | I ² S Data Input/Output Stereo Channel 1 (<i>I²S Bus Word Select output</i>) | WS |
| 64 | I2S_DATA1 | I | I ² S Data Input Stereo Channel 2 (<i>I²S Bus Clock output</i>) | SCK |
| 65 | I2S_DATA2 | I | I ² S Data Input Stereo Channel 3 (<i>Bus Expander Output 1</i>) | BUS1 |
| 66 | VDD18 | DP | 1.8V Power for Digital Core & I/O Cells Pin | <i>Not connected</i> |
| 67 | VSS18 | DP | Ground for Digital Core & I/O Cells Pin | <i>Connected to Ground</i> |
| 68 | BUS_EXP | O | Bus Expander Function (<i>Bus Expander Output 2</i>) | BUS0 |
| 69 | IRQ | O | Interrupt Request to Microprocessor | IRQ |
| 70 | GND_PSUB | AP | Ground Substrate Connection | <i>Connected to Ground</i> |
| 71 | VDD18_ADC | DP | VDD 1.8V for ADC (Digital Part) | <i>Not connected</i> |
| 72 | VSS18_ADC | DP | Ground to Complement 1.8V VDD for ADC | <i>Connected to Ground</i> |
| 73 | SIF_P | A | Sound IF input (positive) | SIF |
| 74 | SIF_N | A | Sound IF input (negative) (ADC V _{TOP} Decoupling pin) | VTOP |
| 75 | GNDPW_IF | AP | Polarization for the IF block (<i>Voltage Reference for AGC Decoupling pin</i>) | VREFIF |
| 76 | VCC18_IF | AP | 1.8V Power for IF AGC & ADC | VDDIF |
| 77 | GND18_IF | AP | Ground for IF AGC & ADC | GNDIF |
| 78 | MONO_IN | A | Mono Input (for AM Mono) | MONOIN |
| 79 | SC4_IN_L | A | SCART4 Audio Input Left | <i>Not connected</i> |
| 80 | SC4_IN_R | A | SCART4 Audio Input Right | <i>Not connected</i> |

Figure 7: STV82x7 Application Diagram

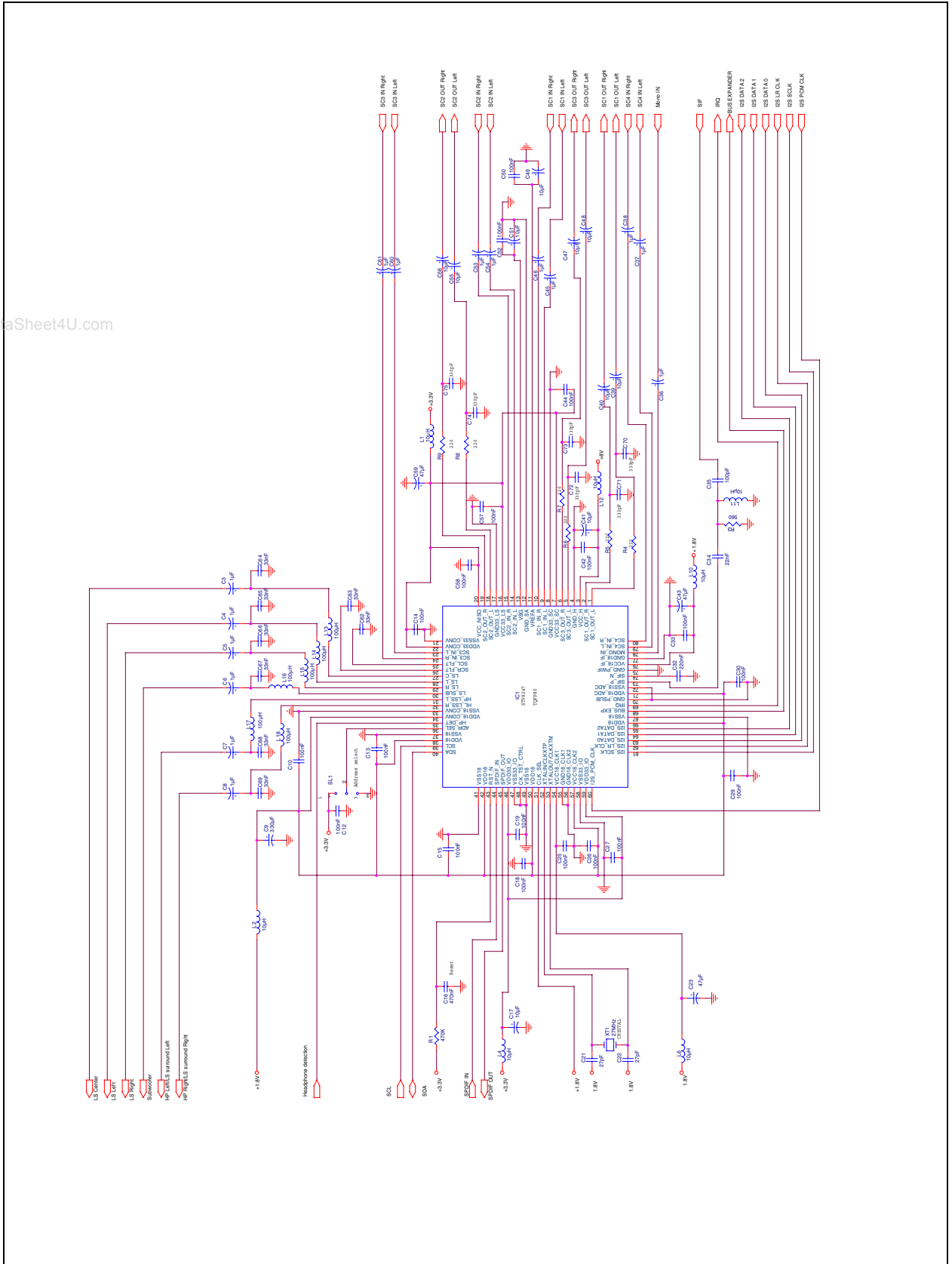


Figure 8: STV82x6/STV82x7 Compatible Application Electrical Diagram

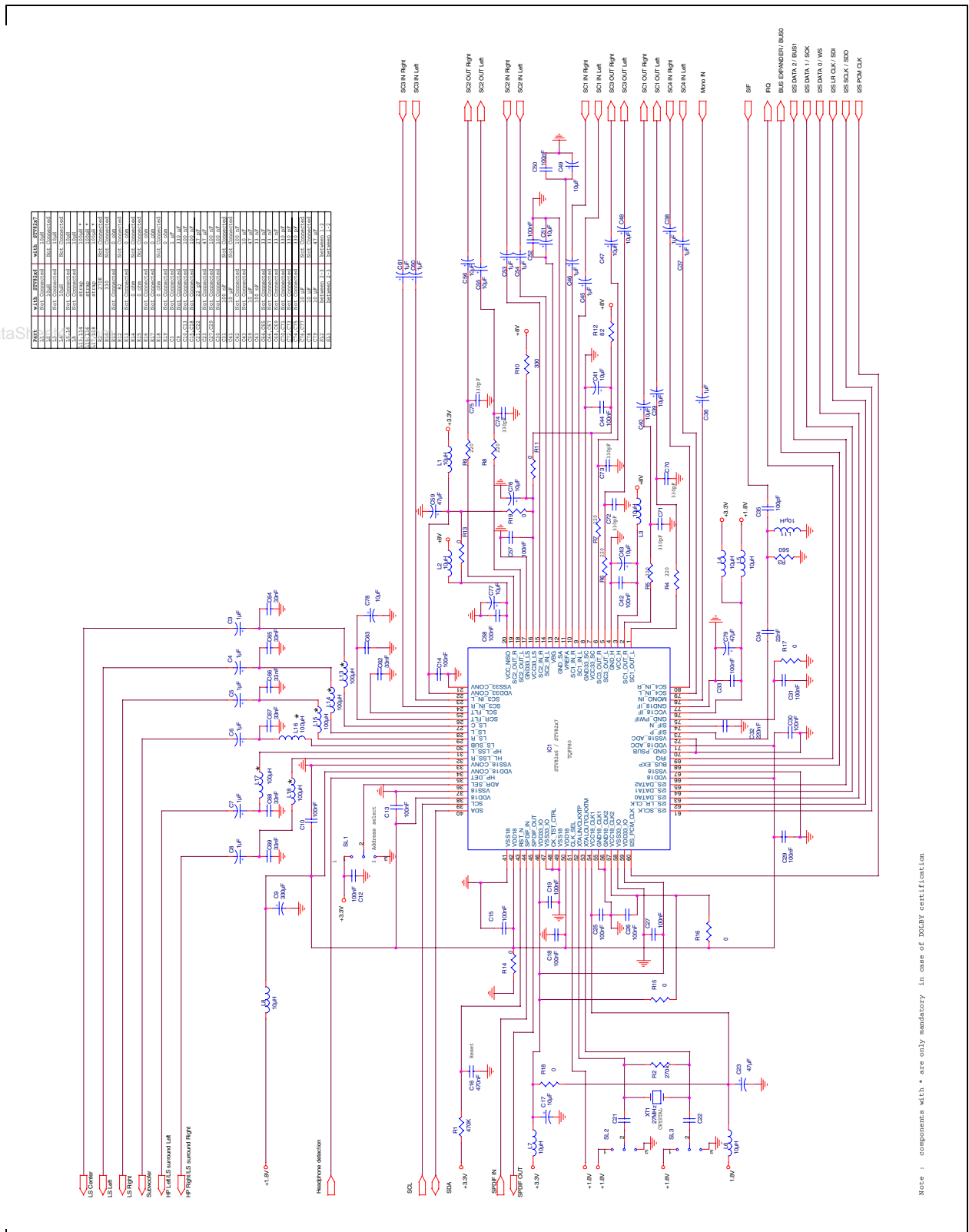
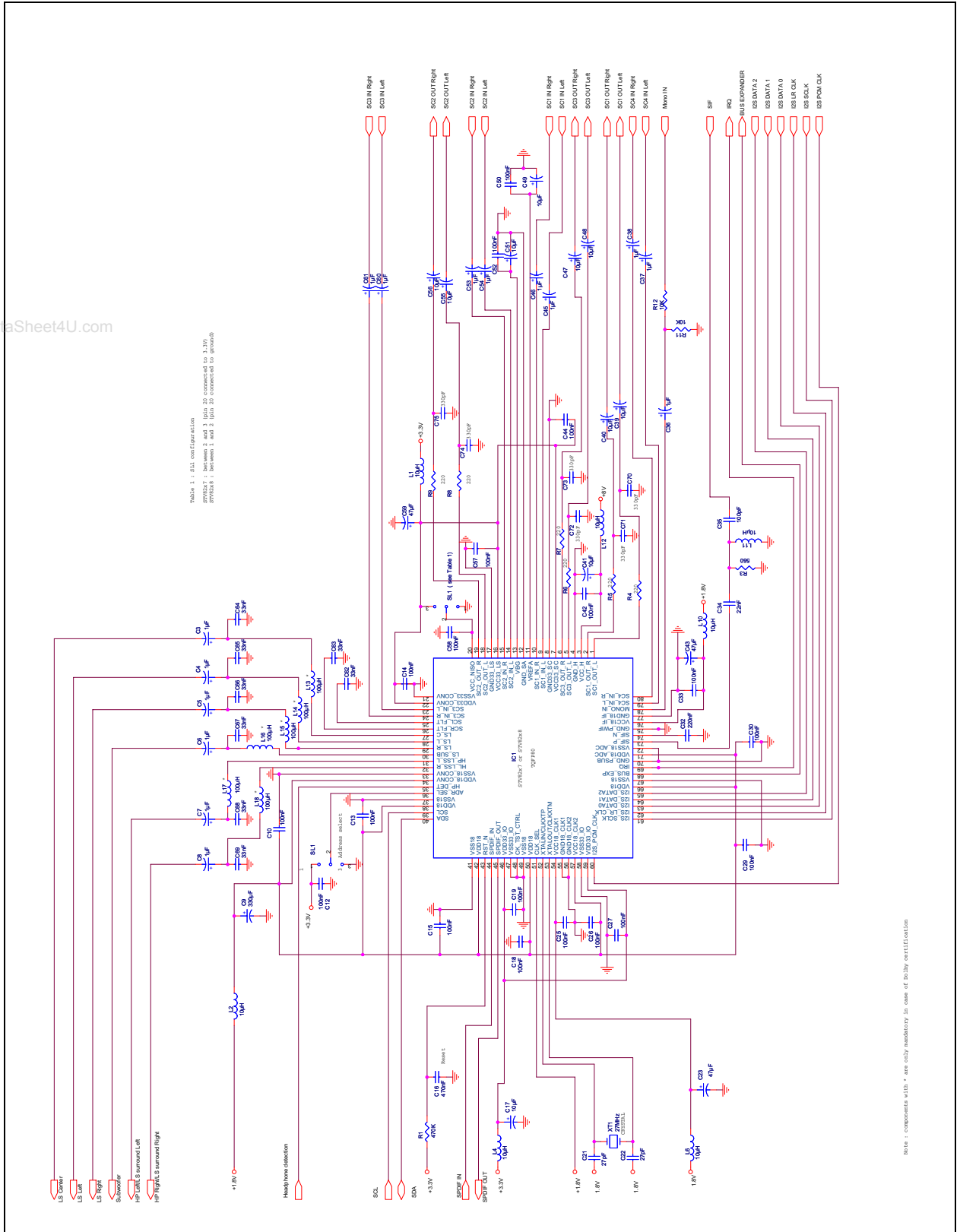


Figure 9: STV82x7/STV82x8 Compatible Application Electrical Diagram (TQFP80)



Note 1: components with * are only mandatory in case of Doxy verification



2 System Clock

The System Clock integrates 2 independent frequency synthesizers.

The first frequency synthesizer can be used in one of two modes:

- In Mode 1, it is used by the demodulator, and the frequency is 49.152 MHz.
- In Mode 2, it is used by the I²S input and is synchronous with the input frequency ($f_S = 32, 44.1$ or 48 kHz) and the frequency is 49.152 MHz (for $f_S = 32$ or 48 KHz) or 45.1584 MHz (for $f_S = 44.1$ KHz).

The second frequency synthesizer is used by the DSP core and can be adjusted between 100 and 150 MHz depending on the application (around 106 MHz at reset value).

The default values are designed for a **standard 27-MHz reference frequency** provided by a stable single crystal or an external differential clock signal (for example, from the STV35x0) depending on the CLK_SEL pin configuration (CLK_SEL = 1 means a single crystal, 0 means an external differential clock). The 27-MHz value is the recommended frequency for minimizing potential RF interference in the application. The sinusoidal clock frequency, and any harmonic products, remain outside the TV picture and sound IFs (PIF/SIF) and Band-I RF.

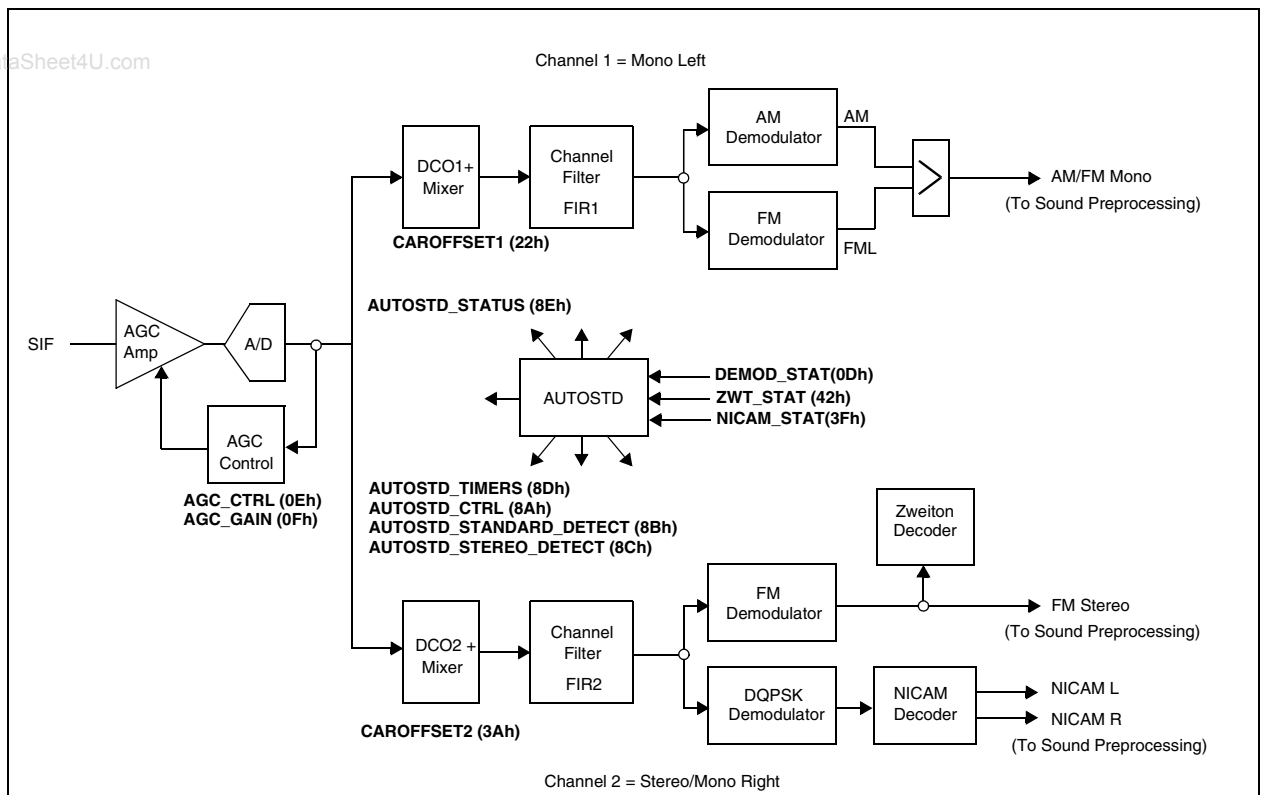
Note: A change in the reference frequency is compatible with other default I²C programming values, including those of the built-in Automatic Standard Recognition System.

3 Digital Demodulator

The Digital Demodulator (see [Figure 10](#)) is composed of two channels. The first channel demodulates an FM or an AM signal. The second channel demodulates FM 2-carrier or NICAM signals (stereo demodulation).

All channel parameters are programmed automatically by the **built-in Automatic Standard Recognition System** (Autostandard) in order to find the correct sound standard. Channels can also be programmed manually via the I²C interface for very specific standards not included among the known standards.

Figure 10: Demodulator Block Diagram



3.1 Sound IF Signal

The Analog Sound Carrier IF is connected to the STV82x7 via the SIF pin. Before Analog-to-Digital Conversion (ADC), an Automatic Gain Control (AGC) is performed to adjust the incoming IF signal to the full scale of the ADC. A preliminary video rejection is recommended to optimize conversion and demodulation performances. The AGC system provides a gain value allowing for a wide range of SIF input levels and is activated for all standards, except L/L'. In this particular case, the sound carrier is AM-modulated and an automatic level adjustment would only damage the transmitted audio signal. A preset I²C parameter is provided to define the gain of the AGC used in Manual mode (Registers [AGC_CTRL](#) and [AGC_GAIN](#)).

Note: For optimum AM demodulation performance, it is recommended to use the MONO Input.

3.2 Demodulation

The demodulation system operates by default in Automatic mode. In this mode, the STV82x7 is able to **identify and demodulate any TV sound standard including NICAM and A2 systems** (see Table 4) without any external control via the I²C interface. It consists of the two demodulation channels (Channel 1 = Mono Left and Channel 2 = Mono Right/Stereo) to simultaneously process two sound carriers in order to handle all transmission modes (stereo and up to three mono languages). The **built-in Automatic Standard Recognition System** (Autostandard) automatically programs the appropriate bits in the I²C registers which are forced to Read-only mode for users (see Section 12.1). The programming is optimized for each standard to be identified and demodulated.

Each mono and stereo standard can be removed (or added) from the List of Standards to be recognized by programming registers [AUTOSTD_STANDARD_DETECT](#) and [AUTOSTD_STEREO_DETECT](#), respectively. The identified standard is displayed in register [AUTOSTD_STATUS](#) and any change to standard is flagged to the host system via pin IRQ. This flag must be reset by re-programming the MSBs of register [AUTOSTD_CTRL](#) while checking the detected standard status by reading registers [AUTOSTD_STATUS](#), [NICAM_STAT](#) and [ZWT_STAT](#). Moreover, the detection of Stereo mode during demodulation is also flagged in register [AUTOSTD_STATUS](#).

Important: L/L' and D/K standards cannot be automatically processed because the same frequency is used for the MONO carrier. An exclusive L/DK selection must be programmed in register [AUTOSTD_CTRL](#). This may be externally controlled by detecting the RF modulation sign, which is negative for all TV standards except L/L'.

To recover out-of standard FM deviations or the Sound Carrier Frequency Offset, additional I²C controls are provided without interfering with the Automatic Standard Recognition System (Autostandard).

DK-NICAM Overmodulation Recovery: Four different FM deviation ranges can be selected (via register [AUTOSTD_CTRL](#)) for the DK standard while the Autostandard system remains active. The maximum FM deviation is 500 kHz in DK Mono mode and 350 kHz in DK NICAM mode (limited by overlapping FM and NICAM spectrum values). The demodulated signal peak level (proportional to the FM deviation) is detected by the Peak Detector and written to registers [PEAK_DET_L](#) and [PEAK_DET_R](#). This value is used to implement Automatic Overmodulation Detection via an external I²C control.

Important: Only the selection of the 50 kHz FM deviation standard is compatible with the other DK-A2* standards (DK1, DK2 or DK3). These standards must be removed from the list of standards (registers [AUTOSTD_STANDARD_DETECT](#) and [AUTOSTD_STEREO_DETECT](#)) when programming larger FM deviations reserved only for DK-NICAM standards.

Table 4: Recognized Standards

| System | Sound Type | Type Name | Carrier 1 (MHz) | Carrier 2 (MHz) | FM Deviation | | | De-emphasis | Roll-off (%) | Pilot Frequency (kHz) |
|--------|--------------|-----------|-----------------|-----------------|--------------|------|------|-------------|--------------|-----------------------|
| | | | | | Nom. | Max. | Over | | | |
| B/G | FM Mono | | 5.5 | | | | | | | |
| | FM/NICAM | | 5.5 | 5.850 | 27 | 50 | 80 | J17 | 40 | |
| | FM 2-Carrier | A2 | 5.5 | 5.742 | 27 | 50 | 80 | 50 μ s | | 54.6875 |
| D/K | FM Mono | | 6.5 | | | | | | | |
| | FM/NICAM | | 6.5 | 5.850 | 27 | 50 | 80 | J17 | 40 | |
| D/K1 | FM 2-Carrier | A2* | 6.5 | 6.258 | | | | 50 μ s | | 54.6875 |

Table 4: Recognized Standards (Continued)

| System | Sound Type | Type Name | Carrier 1 (MHz) | Carrier 2 (MHz) | FM Deviation | | | De-emphasis | Roll-off (%) | Pilot Frequency (kHz) |
|--------|--------------|-----------|-----------------|-----------------|--------------|------|------|-------------|--------------|-----------------------|
| | | | | | Nom. | Max. | Over | | | |
| D/K2 | FM 2-Carrier | A2* | 6.5 | 6.742 | | | | 50 μ s | | 54.6875 |
| D/K3 | FM 2-Carrier | A2* | 6.5 | 5.742 | | | | 50 μ s | | 54.6875 |
| I | FM Mono | | 6.0 | | | | | | | |
| | FM/NICAM | | 6.0 | 6.552 | 27 | 50 | 80 | J17 | 100 | |
| L | AM/NICAM | | 6.5 | 5.850 | | | | J17 | 40 | |
| M/N | FM Mono | | 4.5 | | 15 | 27 | 50 | 75 μ s | | |
| | FM 2-Carrier | A2+ | 4.5 | 4.724 | 15 | 27 | 50 | 75 μ s | | 55.069 |

For Chinese TV transmissions (DK-NICAM) which are subject to overmodulation, different FM deviations are proposed for sound demodulation.

Sound Carrier Frequency Offset Recovery: Both Mono and Stereo IF Carrier frequencies can be adjusted independently (registers [CAROFFSET1](#) and [CAROFFSET2](#)) within a large range (up to 120 kHz for standard mono FM deviations) while the Automatic Standard Recognition System remains active. The frequency offset estimation is written in registers [DC_REMOVAL_L](#) and [DC_REMOVAL_R](#) (Mono Left / Channel 1 and Mono Right / Channel 2, respectively) and can be used to implement the Automatic Frequency Control (AFC) via an external I²C control.

Manual Mode: If required, the Automatic Standard Recognition System system can be disabled (Manual mode) and the user can control all registers including those only controlled by the Automatic Standard Recognition System function when active. Manual mode is selected in register [AUTOSTD_STANDARD_DETECT](#) (bit LDK_SCK, I_SCK, BG_SCK and MN_SCK set to 0).

4 Dedicated Digital Signal Processor (DSP)

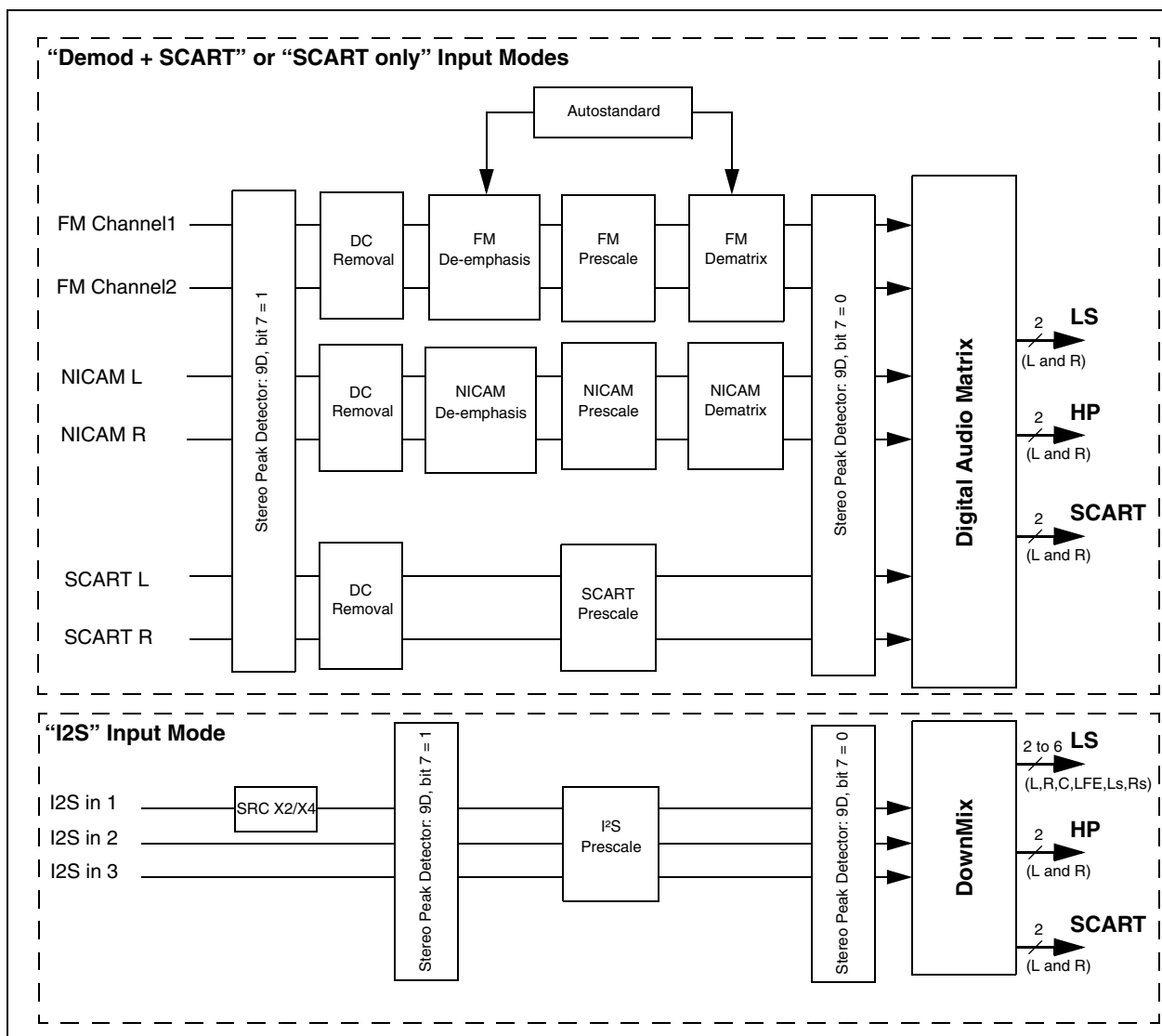
A dedicated Digital Signal Processor (DSP) takes charge of all audio processing features and the low frequency signal processing features of the demodulator. The internal 24-bit architecture will ensure a high quality signal treatment and an excellent dynamic.

4.1 Back-end Processing

The “back-end” processing corresponds to the low frequency signal processing (32 kHz or higher frequencies) of the demodulator and other inputs (I²S, ADC).

Figure 11 shows a flowchart of the back-end processing tasks. However, the figure shows that the processing is only a SINGLE SOURCE PROCESSING flow (no processing is possible with “Demod + SCART” and I²S inputs simultaneously) and that the selection of a headphone output restricts the loudspeakers configuration to 2+1 instead of 5+1.

Figure 11: Back-end Audio Processing



The main features depend on the path:

- FM Channel
 - DC Removal
 - Prescaling
 - De-emphasis (50 or 75 us)
 - Stereo Dematrix
- NICAM Channel
 - DC Removal
 - Prescaling
 - De-emphasis (J17)
 - Dematrix
- Input SCART Channel
 - DC Removal
 - Prescaling
- Input I²S Channel
 - I²S Prescaling
- Digital Audio Matrix
 - Audio Channel Multiplexer between the different sources (IF, I²S, SCART) towards all outputs (S/PDIF, LS, HP or SCART).
- Autostandard management
 - device configuration depending on the standard to be detected
 - freeze the device when a standard is detected
 - once a standard detected, check that there is no change in the detection status
 - set the correct action depending on any change in the detection status (mono backup or mute setup and new standard detection)
- SCART
 - Downmixing: L_T / R_T or L_0 / R_0 (see AC-3 specification)
 - Soft Mute

4.2 Audio Processing

The following software is provided for main loudspeakers (L, R, C, L_S, R_S, SubW):

- Downmix
- Dolby® Pro Logic II® Decoder ($L_T, R_T \rightarrow L, R, C, L_s, R_s, SubW$) with Bass Management
- ST WideSurround, ST OmniSurround, SRS® WOW™ or SRS® TruSurround XT® (certified Virtual Dolby® Surround and Virtual Dolby® Digital)
- ST Dynamic Bass
- Smart Volume Control (SVC)
- 5-band Equalizer or Bass-Treble
- Loudness
- Volume with independent channels (Smooth Volume Control)
- Master Volume Control
- Mute/soft-mute

- Balance
- Beeper
- Pink Noise Generator (used to position the loudspeakers)
- Programmable Delay for each loudspeaker
- Adjustable Delay for “lip sync” up to 120 ms (to compensate audio/video latency) in SCART Only Mode and up to 180 ms in Demodulator and SCART Mode

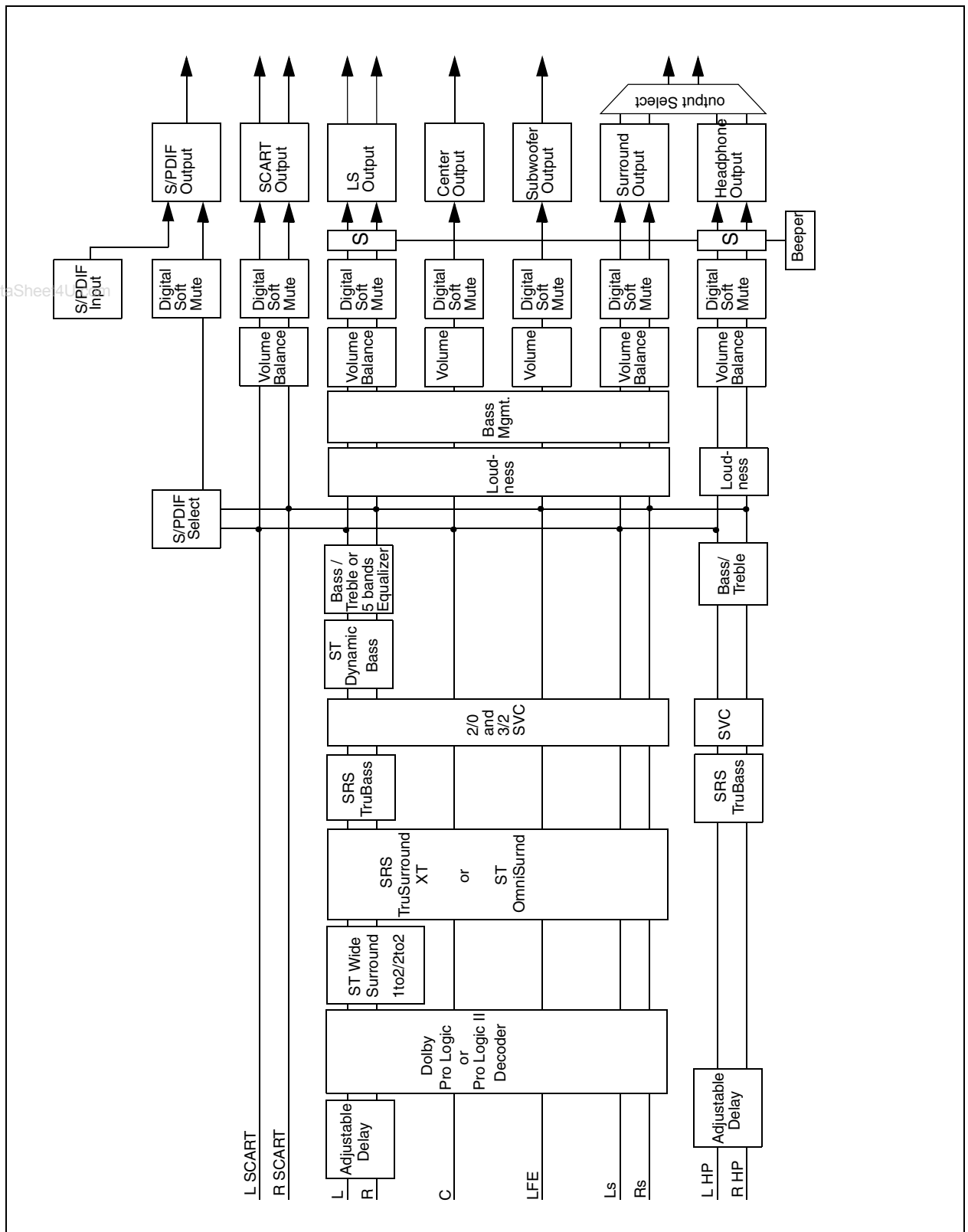
The following software is provided for the headphone or auxiliary output:

- Downmix
- SRS® TruBass™
- Smart Volume Control (SVC)
- Bass/Treble
- Loudness
- Independent Volume for each channel (Smooth Volume Control)
- Soft Mute
- Balance
- Beeper
- Adjustable Delay for “lip sync” up to 120 ms (to compensate audio/video latency) in SCART Only Mode and up to 180 ms in Demodulator and SCART Mode

The following software is provided for SCART or S/PDIF outputs:

- Downmix
- Soft Mute

Figure 12: Audio Processing for Loudspeakers, Headphone, SCART and S/PDIF outputs



4.3 ST WideSurround

STV82x7 offers three preset ST WideSurround Sound effects on the Loudspeakers path:

- Music, a concert hall effect
- Movie, for films on TV
- Simulated Stereo, which generates a pseudo-stereo effect from mono source

“ST WideSurround Sound” is an extension of the conventional stereo concept which improves the spatial characteristics of the sound. This could be done simply by adding more speakers and coding more channels into the source signal as is done in the cinema, but this approach is too costly for normal home use. The ST WideSurround system exploits a method of phase shifting to achieve a similar result using only two speakers. It restores spatiality by adding artificial phase differences.

The Surround/Pseudo-stereo mode is automatically selected by the Automatic Standard Recognition System (Autostandard) depending on the detected stereo or mono source. By default, “Movie” is selected for Surround mode. This value may be changed to “Music” by the STSRND_MODE bit in the [STSRND_CONTROL](#) register.

Additional user controls are provided to better adapt the spatial effect to the source. The ST WideSurround Gain ([STSRND_LEVEL](#)) and ST WideSurround Frequency ([STSRND_FREQ](#)) registers can be used to enhance Music Predominancy in Music mode and Theater effect and Voice Predominancy in Movie mode.

4.4 ST OmniSurround

STV82x7 offers a spatial virtualizer to output any multi-channel input in stereo on the Loudspeakers path:

“ST OmniSurround” will recreate a multi-channel spatial sound environment using only the Left and Right front speakers. It can be adapted to any input configuration (OMNISRND_INPUT_MODE).

ST Voice will allow you to enhance the voice content of your program to increase the intelligibility and the presence of the sound.

4.5 Dolby Pro Logic II Decoder

Dolby® Pro Logic II® is a matrix decoder that decodes the five channels of surround sound that have been encoded onto the stereo sound tracks of Dolby® Surround program material such as DVD movies and TV shows.

It is even possible to decode standard stereo signals like music or non encoded movies. Furthermore, it is an active process designed to enhance sound localization through the use of very high-separation decoding techniques.

The Dolby® Pro Logic II® decoder is also able to emulate the former Dolby® Pro Logic® decoder in a specific mode.

4.6 Bass Management

This processing will generate the subwoofer signal and adjust all loudspeakers channels gain and bandwidth.

Speakers capable of reproducing the entire frequency range will be referred to as “full range speakers”, then signals sent to full range speaker will be full bandwidth (no filtering).

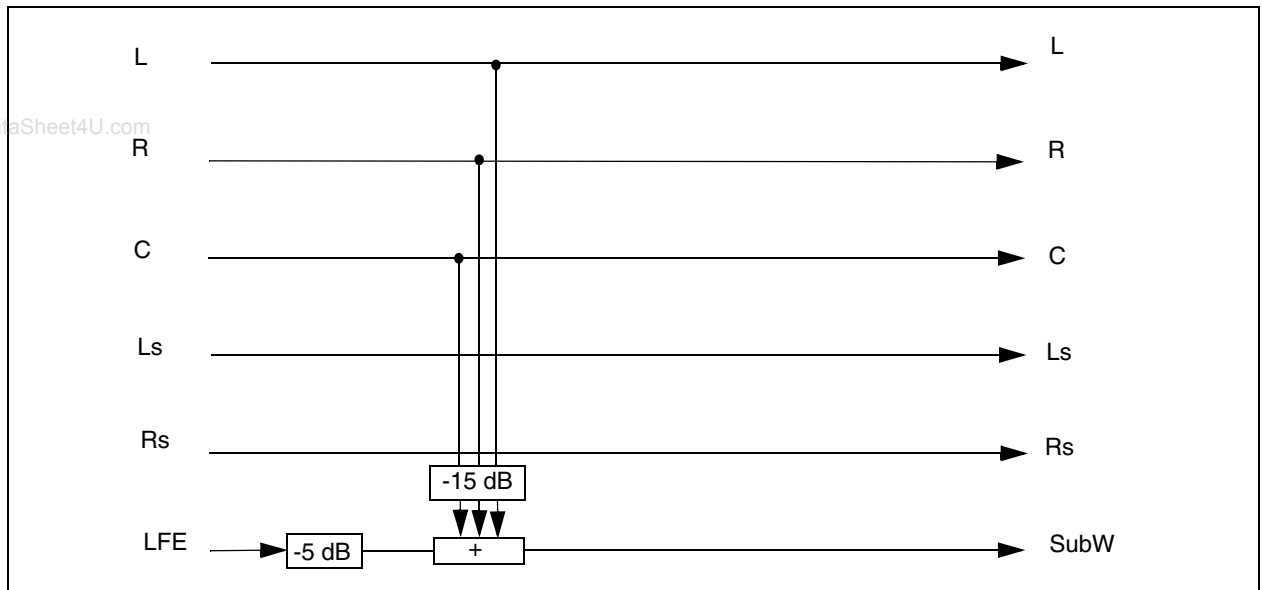
Speakers that have limited bass handling capabilities will be referred to as “satellite speakers”, then signals sent to satellite speaker will be high-pass filtered to remove bass information below 100 Hz.

In the STV82x7, five output configuration modes have been implemented according to “Dolby Digital Consumer Decoder” specifications. They are described below.

4.6.1 Bass Management Configuration 0

In some cases, the bass management filters are available in the decoder itself, so there is no need to reproduce these filters. The output configuration shown in [Figure 13](#) offers this possibility.

Figure 13: Bass Management Configuration 0 (with Pro Logic switch indicating its reset state)

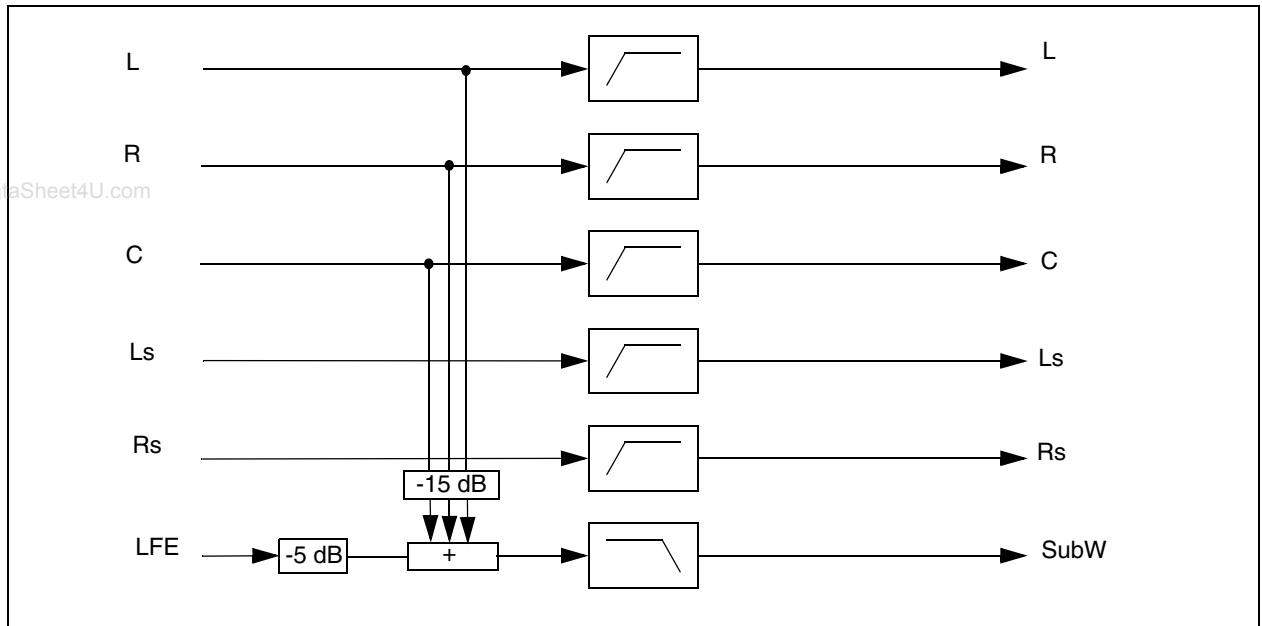


4.6.2 Bass Management Configuration 1

Configuration 1, shown in Figure 14, assumes that all five speakers are not full range and that all of the bass information will be redirected to and reproduced by a single subwoofer. This configuration is intended for use with 5 satellite speakers.

To prevent signal overload, the five main channels are attenuated by 15 dB, while the LFE channel is attenuated by 5dB to maintain the proper mixing ratio.

Figure 14: Bass Management Configuration 1 (with Pro Logic switch indicating its reset state)

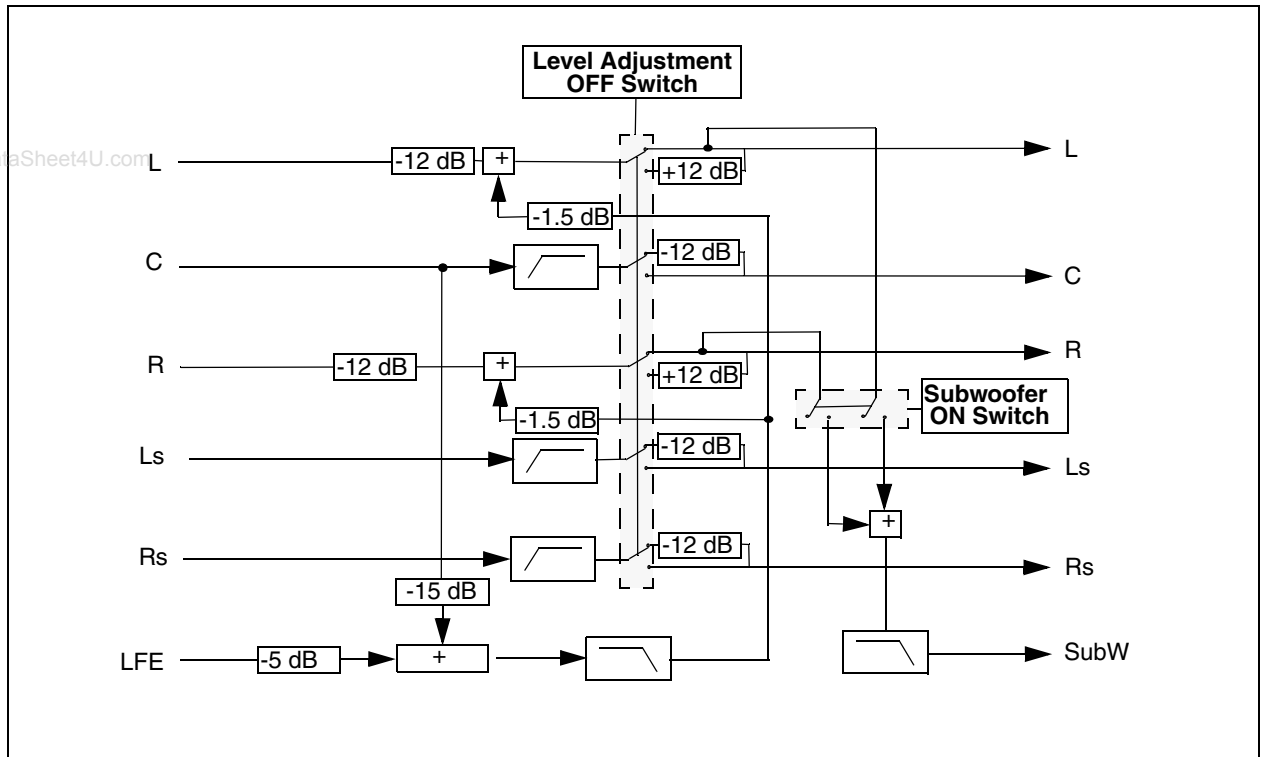


4.6.3 Bass Management Configuration 2

Configuration 2 assumes that the left and right speakers, are full range while the center and surround speakers are smaller speakers. Also, all bass data is redirected to the left and right speakers.

This configuration include output level adjustment that allows 12 dB attenuation for the 3 smaller speakers (C, Ls, Rs). When the level adjustment will be disabled the decoder boosts by 12 dB the full range speakers (Left, Right).

Figure 15: Bass Management Configuration 2 (all switches indicate their reset state)

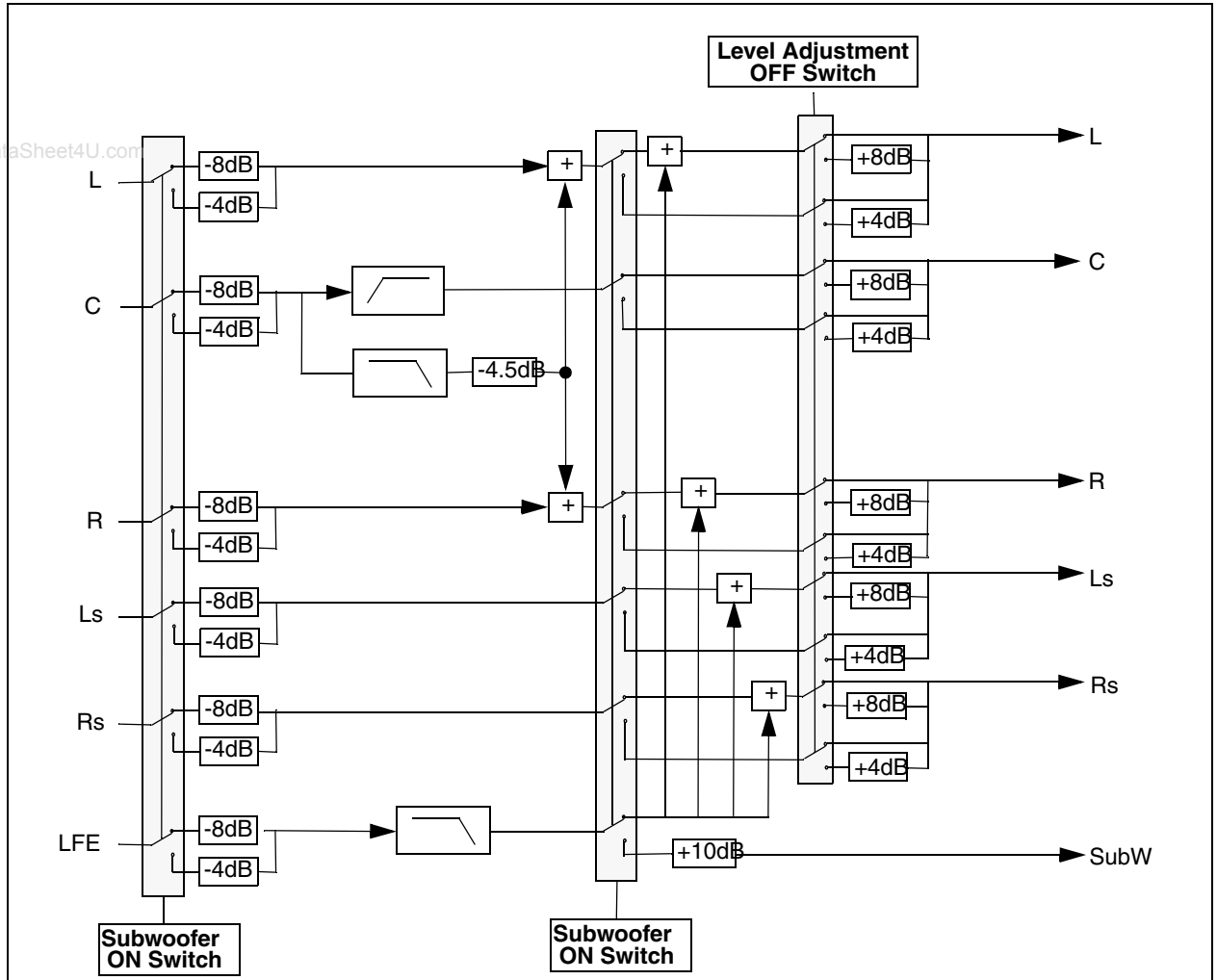


4.6.4 Bass Management Configuration 3

The third configuration, shown in Figure 16, assumes that all speakers except the center are full range, then all bass information will be directed to and reproduced by the front left and front right and both surround speakers. In order to provide more flexibility to this configuration, a switch will offer an option which will produce a subwoofer channel by the LFE channel.

When the Subwoofer Switch is OFF, the input channels will be attenuated by 8 dB. Configuration 3 is required in certain high-end products.

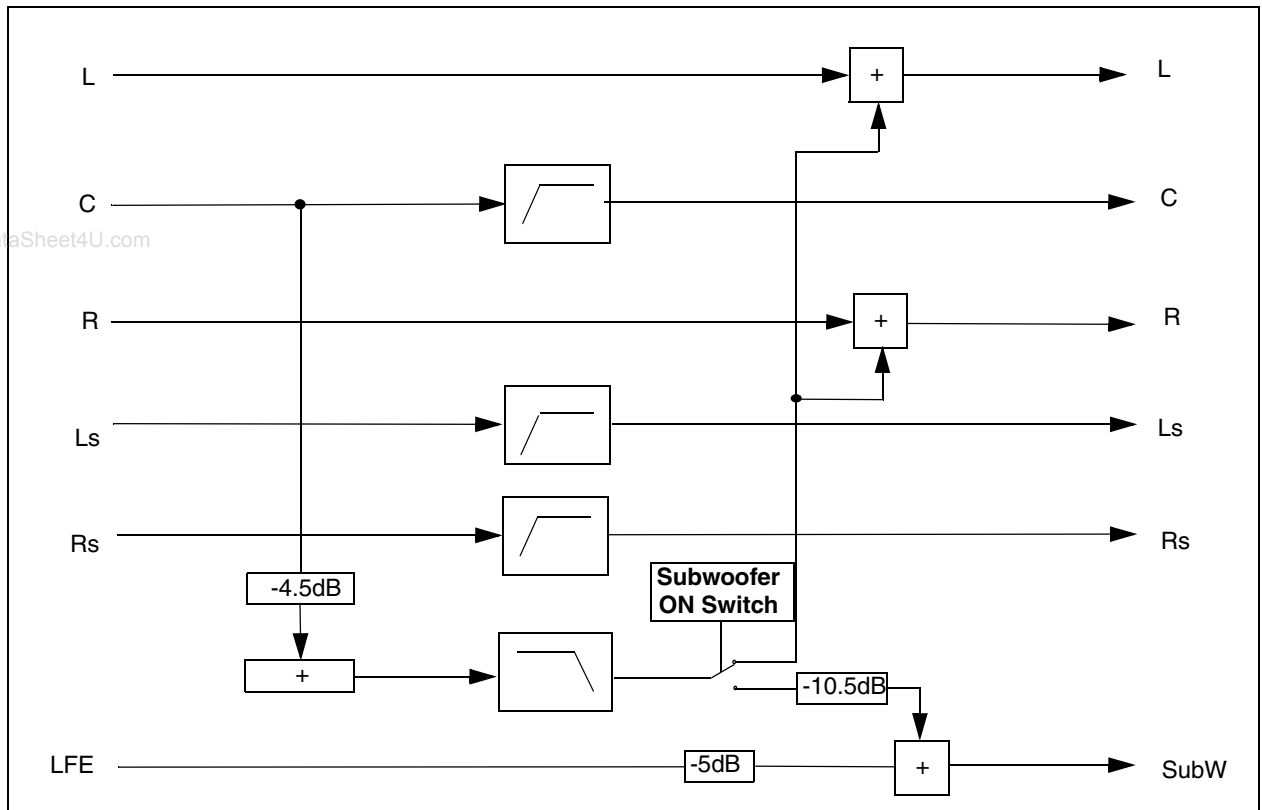
Figure 16: Bass Management Configuration 3 (all switches indicate their reset state)



4.6.5 Bass Management Configuration 4

This configuration implements the Simplified Dolby configuration. The center, left surround and right surround channels are summed and then filtered by the LPF. The composite bass information is either summed back into the left and right channels or summed with the LFE channel and sent to the subwoofer output, see Figure 17.

Figure 17: Implementation of the Bass Management Configuration 4 (Simplified Configuration)



4.7 SRS WOW and TruSurround XT

The SRS® TruSurround XT™ is a processing system that can accept from 1 to 6 channels on input and that will generate a 2-channel output signal.

This processing system includes the latest SRS® algorithms:

- SRS® WOW™
- SRS® TruSurround® (Multi-channel signal virtualizer)

4.7.1 SRS TruSurround

The SRS® TruSurround® is a processing that can accept from 2 to 5 channels on input and that will generate a 2-channel output signal.

SRS® TruSurround® uses Head-Related Transfer Function (HRTF) -based frequency tailoring of (L/R) difference signals to extend the sound image out past the physical boundaries of the speaker placements to surround channel information. These rear channel HRTF curves have much greater peak to valley differences at center frequencies. These were chosen to cause rear channel difference signals to virtualize farther behind the listener and directed to a different virtual position as compared to front channel signals. Information that is equal (L+R) in the rear surround channels

is processed by an identical HRTF curve but mixed in at a much lower amount. This HRTF processing of equal (L/R) signals was again used to virtualize information to the rear of the listener.

The SRS® TruSurround® is certified by Dolby Laboratories to be a Virtual Dolby® Digital and Virtual Dolby® Surround.

4.7.2 SRS WOW

The SRS® WOW™ is an a sound processing system including:

- SRS® 3D Mono/Stereo™
- SRS® Dialog Clarity™
- SRS® TruBass™

4.7.2.1 SRS 3D Mono/Stereo

This system is used to create a pseudo-stereo signal for mono inputs or a three-dimensional spatial signal for stereo inputs.

4.7.2.2 SRS Dialog Clarity

This system is used to enhance dialog perception.

4.7.2.3 SRS TruBass

The SRS® TruBass™ audio enhancement technology provides deep, rich bass to small speaker systems without the need for a subwoofer or additional extra physical components. For systems with a subwoofer, TruBass™ complements and enhances bass performance. Psycho-acoustically, when the human ear is presented with a low frequency sound signal that is missing the fundamental harmonic, it will fill in the fundamental frequency based on the higher harmonics that are present. By accentuating the second and higher frequency harmonics of the bass portion of a signal, TruBass™ gives the perception of greatly improved bass response.

SRS® TruBass™ is implemented on loudspeakers path, headphone path or on both in parallel.

4.8 Smart Volume Control (SVC)

The Smart Volume Control regulates the audio signal level before audio processing. This regulation is necessary in order for the signal level to be independent from the source (terrestrial channels, I2S or SCART), its modulation (AM, FM or NICAM) and annoying volume changes (advertising, etc.). The Smart Volume Control works as an audio compressor/expander; i.e. when the input signal exceeds the threshold level, a very rapid attenuation (-2 dB/ms) is applied to rescale the signal down to the threshold value. When the input signal is below the threshold level, the previous attenuation is reduced slowly in order to retrieve the original input level (0dB gain). If the input signal is too low, an addition gain of 6 dB can be provided.

To personalize the action of the SVC, five parameters are available:

1. Threshold: Maximum quasi-peak level that can be expected on output
2. Peak measurement mode: Select the channel on which the peak measurement must be performed (Left, Right, Center...)
3. Release time: Gain slope applied to the amplification phase
4. Expander switch: To allow a +6dB amplification of small signals in order to reduce the output dynamic range
5. Make up gain: Allows compensation of the signal amplitude limitation thanks to a 0 to 24 dB adjustable gain.

The SVC is implemented on the loudspeakers path, headphone path or on both in parallel (independent settings). Also, the SVC can be applied in six-channel mode (L, R, L_S, R_S, C and SubW).

4.9 ST Dynamic Bass

STV82x7 offers dynamic bass boost processing on the Loudspeakers path:

ST Dynamic Bass is a bass boost process that can dramatically increase the bass content of any program without any output level saturation.

3 cutoff frequencies (BASS_FREQ) can be chosen, 100Hz, 150Hz and 200Hz to adapt the effect to your loudspeakers. The amount of bass (BASS_LEVEL) can also be fine tuned in order to adapt the effect loudness.

www.DataSheet4U.com

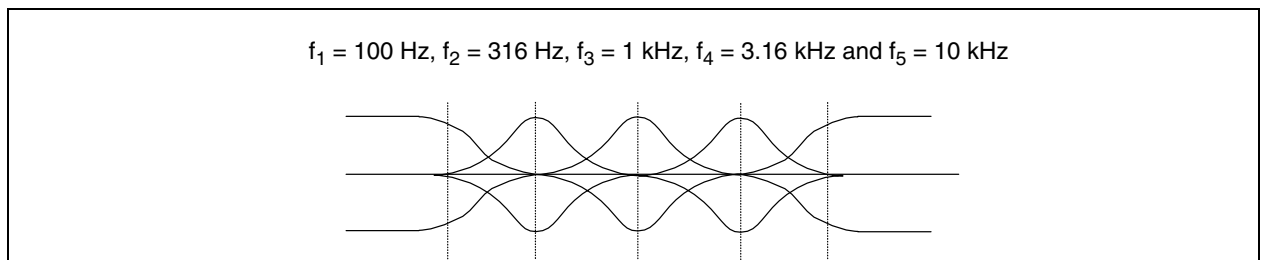
4.10 5-Band Audio Equalizer

The loudspeakers audio spectrum is split into 5 frequency bands and the gain of each of band can be adjusted within a range from -12 dB to +12 dB in steps of 0.25 dB. The Audio Equalizer may be used to pre-define frequency band enhancement features dedicated to various kinds of music or to attenuate frequency resonances of loudspeakers or the listening environment. The Equalizer is enabled by the LS_EQ_ON bit in the [LS_EQ_BT_CTRL](#) register. The gain value for Band X is programmed in register [EQ_BANDX_GAIN](#).

The 5-Band Audio Equalizer is exclusive with Bass-Treble control. Bit LS_EQ_BT_SW in register [LS_EQ_BT_CTRL](#) is used to select either the 5-Band Audio Equalizer or the Bass-Treble control for the Loudspeakers path.

Depending on the LS Equalizer or LS Bass-Treble value, the volume level can be clamped to the LS output to prevent any possible signal clipping from occurring using the ANTICLIP_LS_VOL_CLAMP bit in the [VOLUME_MODES](#) (D7h) register.

Figure 18: Equalizer



4.11 Bass/Treble Control

The gain of bass and treble frequency bands for Headphone can be also tuned within a range from -12 dB to +12 dB in steps of 0.25 dB. It may be used to pre-define frequency band enhancement features dedicated to various kinds of music. The Headphone Bass/Treble feature is enabled by setting the HP_BT_ON bit in the [HP_BT_CONTROL](#) register. The Bass and Treble gain values are adjusted in registers [HP_BASS_GAIN](#) and [HP_TREBLE_GAIN](#), respectively.

Depending on the HP Bass-Treble value, the volume level can be clamped to the HP output to prevent any possible signal clipping from occurring using the ANTICLIP_HP_VOL_CLAMP bit in the [VOLUME_MODES](#) (D7h) register.

4.12 Automatic Loudness Control

As the human ear does not hear the audio frequency range the same way depending on the power of the audio source, the Loudness Control corrects this effect by sensing the volume level and then boosting bass and treble frequencies proportionally to middle frequencies at lower volume.

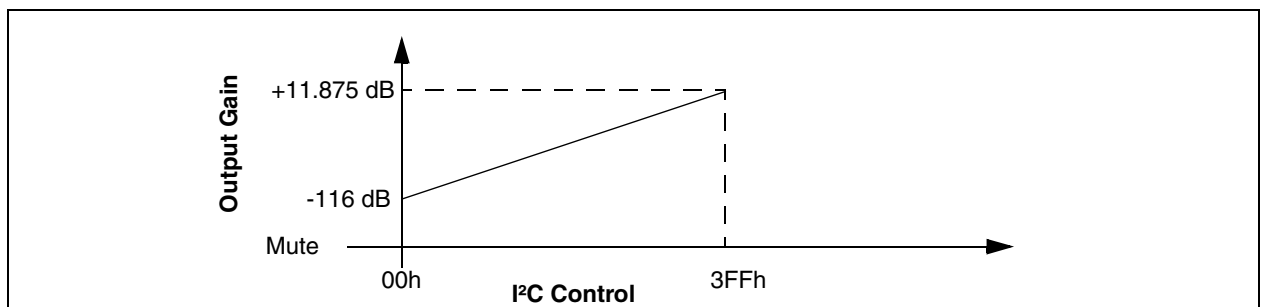
While maintaining the amplitude of the 1 kHz components at an approximately constant value, the gain values of lower and higher frequencies are automatically progressively amplified up to +18 dB when the audio volume level decreases. The maximum treble amplification can be adjusted from 0 dB (first order loudness) to +18 dB (second order loudness) in steps of 0.125 dB. As the volume is proportional to the external audio amplification power, the loudness amplification threshold is programmable in order to tune the absolute level. The Loudspeakers Loudness function is enabled by setting the LS_LOUD_ON bit in register [LS_LOUDNESS](#). The Loudspeakers Loudness Threshold and Maximum Treble Gain values are also programmed in this register. The Headphone Loudness function is enabled by setting the HP_LOUD_ON bit in register [HP_LOUDNESS](#). The Headphone Loudness Threshold and Maximum Treble Gain values are also programmed in this register.

The loudness cut-off frequency is 100 Hz.

4.13 Volume/Balance Control

The STV82x7 provides a Volume/Balance Control for all output channels configuration (except for S/PDIF) with different volume level per channel (L, R, C, L_S, R_S, SubW, SCART). Its wide range (from +11.875 to -116 dB, in a dB linear scale with a 0.125 dB step) largely covers typical home applications (approx. 60 dB) while maintaining a good S/N ratio.

Figure 19: Volume Control



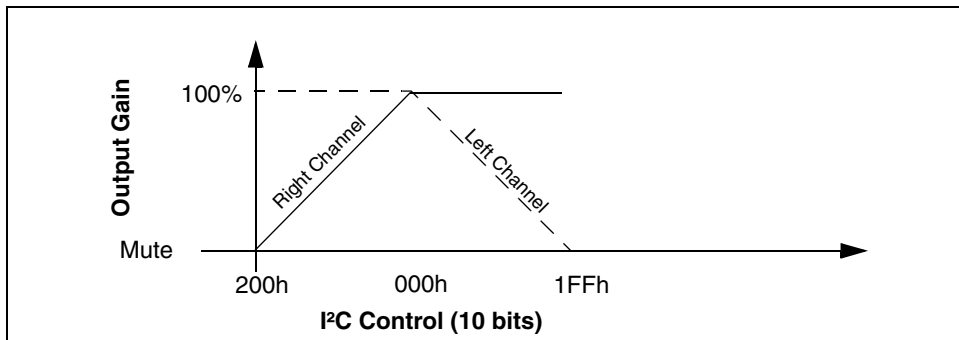
An extra Master Volume Control can apply an extra gain/attenuation on L, R, C, L_S, R_S and SubW channels.

The Volume/Balance Control can operate in one of two different modes:

- In **Differential mode** (default value), the volume control is a common volume value for both the Left and Right Loudspeakers or Headphone channels (see [Figure 19](#)) and complimentary balance control is used (see [Figure 20](#)).

- In **Independent mode**, the volume for the Left and Right channels for Loudspeakers or Headphone is controlled independently.

Figure 20: Differential Balance



4.14 Soft Mute Control

The Digital Soft Mute is applied smoothly (20 ms for 120 dB range) to avoid any switch noise on output. It is available on all output channels pairs:

- S/PDIF channel (Left/Right)
- SCART channels (Left/Right)
- Loudspeakers channels (Left/Right)
- Center
- Subwoofer
- Headphone/Surround channels (Left/Right)

Another soft mute (analog) is also available on each DAC output.

4.15 Beeper

The beeper is used to generate a tone on the Loudspeakers or/and Headphone outputs. The beeper sound (square wave) is added to the audio signal which is attenuated by 20 dB. The beep sound amplitude includes a smooth attack and decay to avoid any parasitic noise when starting and stopping.

It can be used for various applications such as beep sounds for remote control, alarm clock or other features.

The Beeper operates in one of two modes:

- **Pulse mode** (beep applications): A tone with a programmable short duration (0.1, 0.25, 0.5 and 1.0 s) is generated. Afterwards, the beeper is automatically disabled and the output is switched back to the audio signal, see [Figure 21](#).
- **Continuous mode** (alarm application): A tone with a programmable long duration is generated. Its start and stop controls must be programmed by I²C, see [Figure 22](#).

The Beeper function is enabled by setting the BEEPER_ON bit in register [BEEPER_ON](#).

Beeper parameters are controlled in register [BEEPER_MODE](#).

The beeper tone level and frequency are programmed in register [BEEPER_FREQ_VOL](#). The level (or volume) ranges between 0 dB and -93 dB in steps of 3 dB and the tone frequency ranges between 62.2 Hz and 8 kHz in steps of 1 octave.

A beep generator is shared only by the Loudspeakers or Headphone outputs. Therefore, in the event of simultaneous beeps when in Pulse mode, only the first beep will define the effective duration that will be the same for both outputs.

Figure 21: Pulse Mode

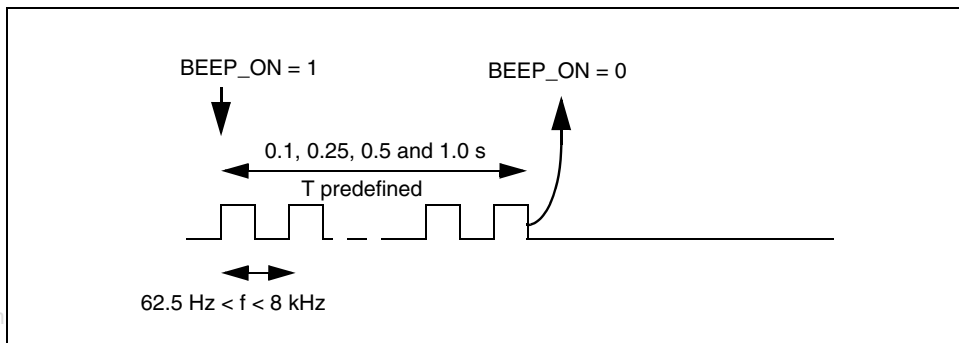
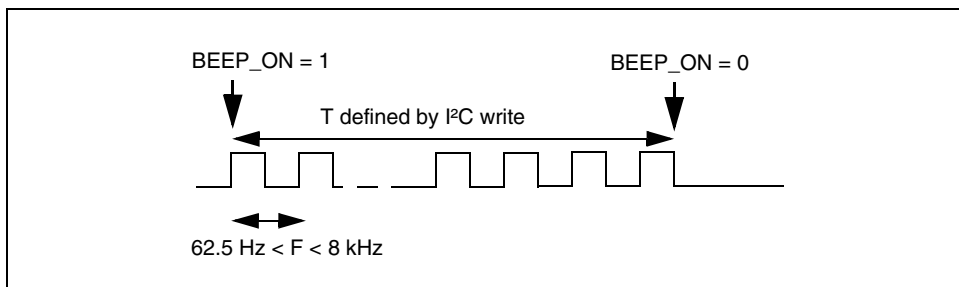


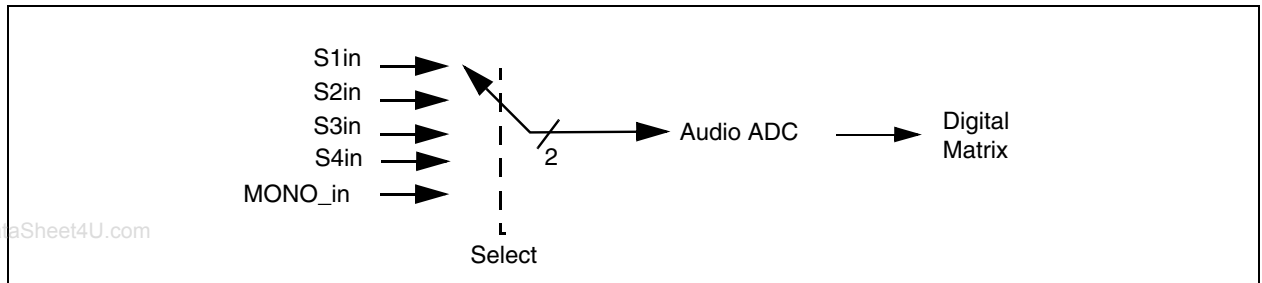
Figure 22: Continuous Mode



5 Analog Audio Matrix (In / Out)

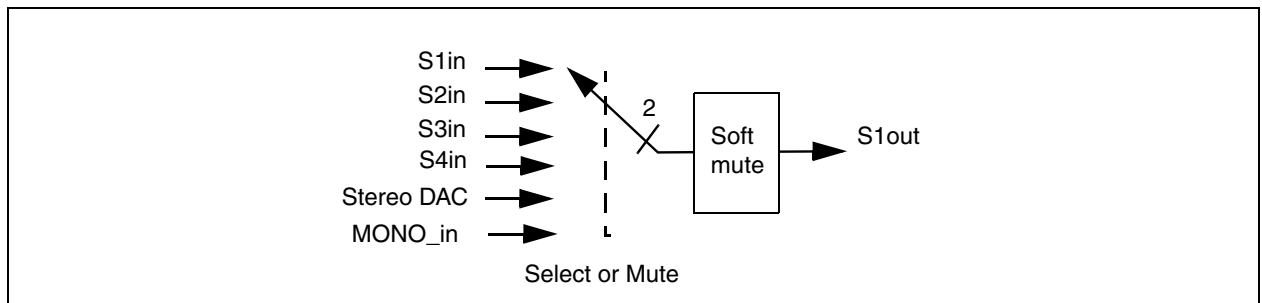
The analog part of the audio matrix can be divided into two parts: the SCART input matrix and the SCART output matrix.

Figure 23: SCART Input Matrix



The SCART input matrix is an input for the digital matrix (after the ADC) which select which source will be sent to the DSP.

Figure 24: SCART1/2/3 Output Matrix



The SCART output matrix selects the sound to output, which can be directly a SCART input or the output of the DSP. A mute function is provided to switch off the outputs.

A soft-mute function is provided to avoid all spurious sounds when switching from one position to another position.

The SCART 2 and 3 output matrices have the same functions as the SCART 1 output matrix.

The particularity of the matrix is to accept input signal of $2 V_{RMS}$ and to have the capability to output such level. In this case, the power supply must be 8 V.

The Mono audio input is able to accept signals with a $0.5 V_{RMS}$ amplitude.

6 I²S Interface (In / Out)

The STV82x7 offers three input/output choices: one I²S input, three I²S inputs or one I²S output.

6.1 I²S Inputs

The STV82x7 can interface with a digital sound decoder. In this case, the digital data can be input at a speed of 0.384 Mbytes/s (3.072 MHz for a 48 kHz sampling frequency with 32 bits of data). In compliance with Dolby® specifications, only the sampling frequency is subject to restrictions. All other requirements are extracted from other various specifications.

Table 5: I²S Characteristics

| | |
|---------------------------------|--|
| Sampling Frequency (kHz) | 8, 11.025, 12,16, 22.05, 24, 32, 44.1 and 48 |
| Data Size | 16, 18*, 20*, 24*, 32 |
| PCMCLK | $512 \times f_s^{1,2}$ |

1. means that the number is the number of effective bits but the transmission is with 32 bits.
2. $512 \times f_s$ is used by the DACs if $512 \times f_s$ is present.

The PCMCLK (possible clock for upsampling) is provided by the master which is the digital sound decoder. A sample rate conversion (SRC) will be necessary in the second case (STV82x7 slave) in order to have a fixed frequency output from this block (either 32 kHz, 44.1 kHz or 48 kHz).

Note: The SRC function is only available in single I²S input mode.

The I²S interface is used in two ways depending on the package:

1. The interface with one I²S (I²S_DATA0) connection (only stereo or stereo-coded Dolby® Pro Logic®);
2. One interface with three I²S connections connected to the DSP to allow the processing of a multi-channel signal (maximum of 6 channels).

Figure 25: I²S Block Diagram

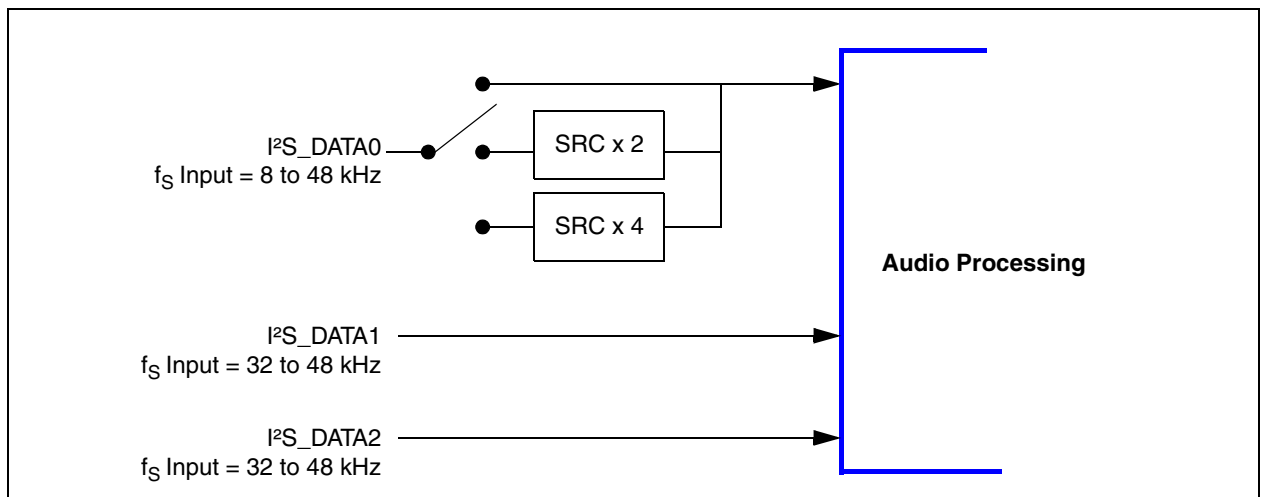


Table 6: I²S Frequency Configuration

| I ² S (Max. Number of Channels) | f _S Input (kHz) | f _S Output (kHz) after SRC | SRC Use |
|---|----------------------------|--|---------|
| 1 (I ² S_DATA0) | 8 | 32.0 | x 4 |
| 1 (I ² S_DATA0) | 16 | 32.0 | x 2 |
| 3 | 32 | 32.0 | No |
| 1 (I ² S_DATA0) | 11.025 | 44.1 | x 4 |
| 1 (I ² S_DATA0) | 22.05 | 44.1 | x 2 |
| 3 | 44.1 | 44.1 | No |
| 1 (I ² S_DATA0) | 12 | 48.0 | x 4 |
| 1 (I ² S_DATA0) | 24 | 48.0 | x 2 |
| 3 | 48 | 48.0 | No |

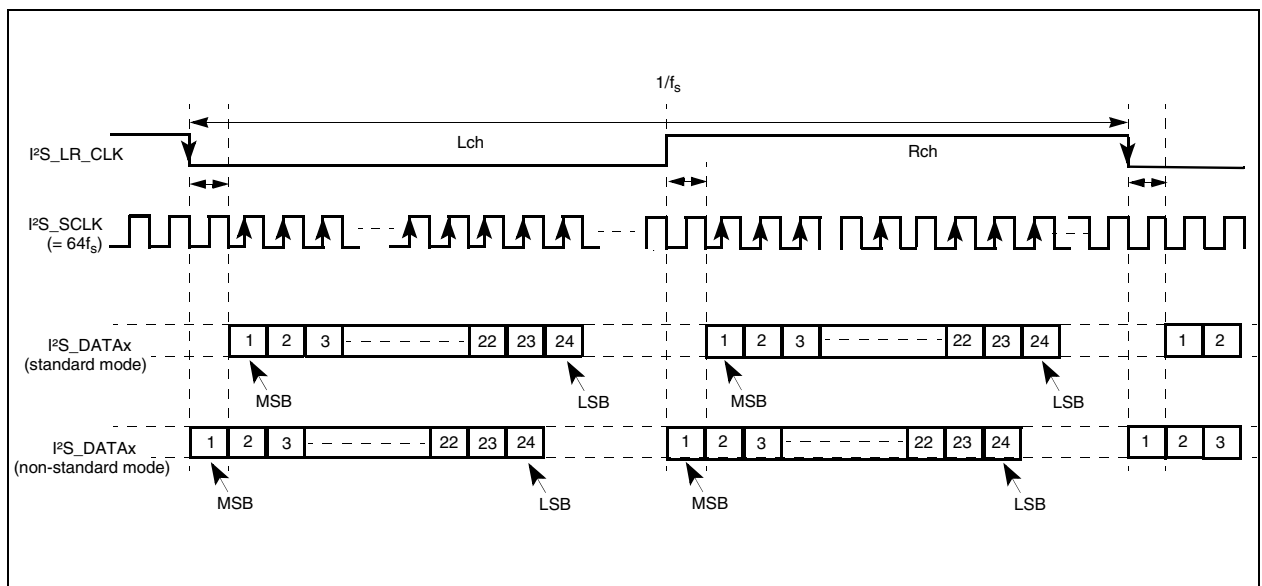
Both standard and non-standard modes are available, see [Figure 26](#).

6.2 I²S Output

A digital stereo output (I²S compatible) is also available for routing the demodulated signal or a converted input audio signal to an external device. In this case the I²S_DATA0 signal and all clock signals are set as outputs by setting bit D6 in register RESET to 1. The STV82x7 I²S drives the serial bus (SCLK, LR_CLK, I²S_DATA0) in master mode in 64.f_s format with a sampling frequency (f_s) of 32 kHz. The I²S_PCM_CLK signal can be used as a master clock in 512.f_s format if required for the slave interface. Both standard and non-standard modes are available, see [Figure 26](#).

Note: The Input and Output modes for I²S are exclusive.

Figure 26: I²S Data Format: Lch = LOW, Rch = HIGH (I²S Input or Output mode)



7 S/PDIF Input/Output

An S/PDIF output is available for connection with an external decoder/amplifier. An internal multiplexer allows selection of either the internal signal or the external signal connected on the SPDIF input (for example, the signal provided by the external MPEG audio / Dolby Digital decoder). The outputted internal signal can be selected from:

- L/R
- C/Sub
- HP or Surround
- SCART.

A mute facility is also provided on the SPDIF output.

8 Power Supply Management

A mixed supply voltage environment requires the following voltages:

- 3.3V capable inputs/outputs for digital pins;
- 1.8V digital core;
- 8V capable inputs/outputs for analog audio interfaces (capability to output 2 V_{RMS} for SCART requirements);
- 3.3V for stereo ADC and DAC (analog part);
- 1.8V for stereo ADC and DAC (digital part);
- 1.8V for IF ADC and AGC.

These voltages will be delivered by the application with an accuracy of $\pm 5\%$. For more information, refer to [Section 13.3: Power Supply Data](#).

Other specific DC voltages or features are provided:

- Voltage Reference and Biasing Generation (AGC, ADCs, DACs),
- Bandgap reference.

8.1 Standby Mode (Loop-through mode)

The STV82x7 provides a Loop-through mode configuration that bypasses IC functions via a SCART I/O pin (Full Analog Path only). In this case, only a minimum power of 200 mW is required.

In Standby mode, the digital and analog power supplies are switched off, except for pins VCC_H, VCC33_LS, VCC33_SC, and VCC_NISO which are used to maintain the SCART path with the last configuration programmed by analog matrixing (register [SCART1_2_OUTPUT_CTRL](#) and [SCART3_OUTPUT_CTRL](#)). When switching back to normal Full Power mode, all I²C registers are reset except for those used in Standby mode to maintain the original configuration.

In Standby mode, the I²C bus does not operate. However, the bus can still be used by other ICs since the I²C I/O pins (SDA and SCL) of the STV82x7 are forced into a high-impedance configuration.

9 Additional Controls and Flag

This logic contains:

- the headphone detection,
- the IRQ generation, signal to be output to the MCU,
- the I²C bus expander output pin.

9.1 Headphone Detection

For headphone, the $\overline{\text{HP_DET}}$ input can be used to automatically mute the Loudspeakers and Subwoofer outputs when the HP_LS_MUTE bit is set in register [HEADPHONE_CONFIG](#) (active low). When a headphone is detected (the $\overline{\text{HP_DET}}$ pin is set to 0) and the Mute function is enabled. Each change on the $\overline{\text{HP_DET}}$ pin generates an IRQ request to the microprocessor on the IRQ pin.

9.2 IRQ Generation

Four IRQs are generated by the STV82x7. On each IRQ generation, the IRQ pin is set to 1. The pending IRQ status must be read at the I²S address 81h and the acknowledge is done by writing 0 to this register.

The four availables IRQs are:

IRQ0: The identified TV sound standard is displayed in register [AUTOSTD_STATUS](#). Each change in the detected standard is flagged to the host system via hardware pin IRQ. The flag must be reset by re-programming the IRQ bit in register [AUTOSTD_CTRL](#) and then checking the detected standard status by reading registers [AUTOSTD_STATUS](#), [NICAM_STAT](#), and [ZWT_STAT](#).

IRQ1: This IRQ is enabled only in digital input mode. In case of I²S synchronisation loss, this IRQ is set to 1.

IRQ2: This IRQ is set to 1 when the device detects any change on the HP Detection pin (Headphone connection or disconnection).

IRQ3: On the STV82x7, same pins are used for both Headphone and Surround loudspeaker signal output. A change in the Headphone configuration (HP active or not active) will lead to a signal switch on those hardware pins. In order to ensure a smooth audio transition, the output is soft muted before the signal is switched. The IRQ3 is then set to 1 to advise the master processor that the signal has been switched and to request a HP/Srnd Output Un-Mute.

9.3 I²C Bus Expander

Pin BUS_EXP can be used to control external switchable IF SAW filters or audio switches. This pin can be directly programmed by register [RESET](#).

10 STV82x7 Reset

All STV82x7 features are controlled via the I²C bus.

The STV82x7 can be "reset" in 2 ways:

1. By Software via the I²C bus: This clears all synchronous logic, except for the I²C bus registers.
2. By Hardware via the RESET pin: In addition to clearing all synchronous logic, the RESET input (active on the low level) resets all the I²C bus registers to the *default values* listed below.

Table 7: RESET Default Values

| Function | Default mode |
|-------------------------------|----------------------------------|
| Demodulation | |
| Auto-standard | ON |
| Scanned Standards | M/N, B/G, I, L/L' |
| FM Deviation | ± 125 kHz (Max.) |
| Audio Outputs | |
| Automatic Mute Mode | ON |
| Loudspeaker Source | Demodulated Sound |
| Loudspeaker Volume | -40 dB, differential mode, muted |
| Loudspeaker L/R Balance | L/R = 100% |
| Subwoofer | -40 dB / OFF |
| Headphone Source | Demodulated Sound |
| Headphone Automatic Detection | ON |
| Headphone Volume | -40 dB, differential mode, muted |
| Headphone L/R Balance | L/R = 100% |
| SCART-1 out | Demodulated Sound |
| SCART-2 out | SCART1 Source |
| SCART Volume | -5.5 dB, independent mode, muted |
| I ² S out | OFF |
| Audio Processing | |
| Loudspeaker/Headphone SVC | OFF, 0 dB Reference Value |
| Loudspeaker Surround | OFF |
| Loudspeaker 5-Band Equalizer | OFF, 0 dB (Flat Band) |
| Loudspeaker Loudness | OFF |
| Headphone Bass/Treble | OFF, 0 dB (Flat Band) |
| Loudspeaker/Headphone Beeper | -40 dB / OFF |

11 I²C Interface

11.1 I²C Address and Protocol

The STV82x7 I²C interface works in Slave mode and is fully compliant with I²C standards in Fast mode (maximum frequency of 400 kHz). Two pairs of I²C chip addresses are used to connect two STV82x7 chips to the same I²C serial bus. The device address pairs are defined by the polarity of the ADR_SEL pin and are listed in the following table:

Table 8: I²C Read/Write Addresses

| ADR | Write Address (W) | Read Address (R) |
|--------------------------|-------------------|------------------|
| LOW (connected to GND1) | 80h | 81h |
| HIGH (connected to VDD1) | 84h | 85h |

Protocol Description

- Write Protocol

| | | | | | | | | | | | |
|-------|---|---|-------------|---|------|---|------|---|------|---|------|
| Start | W | A | Sub-address | A | Data | A | | A | Data | A | Stop |
|-------|---|---|-------------|---|------|---|------|---|------|---|------|

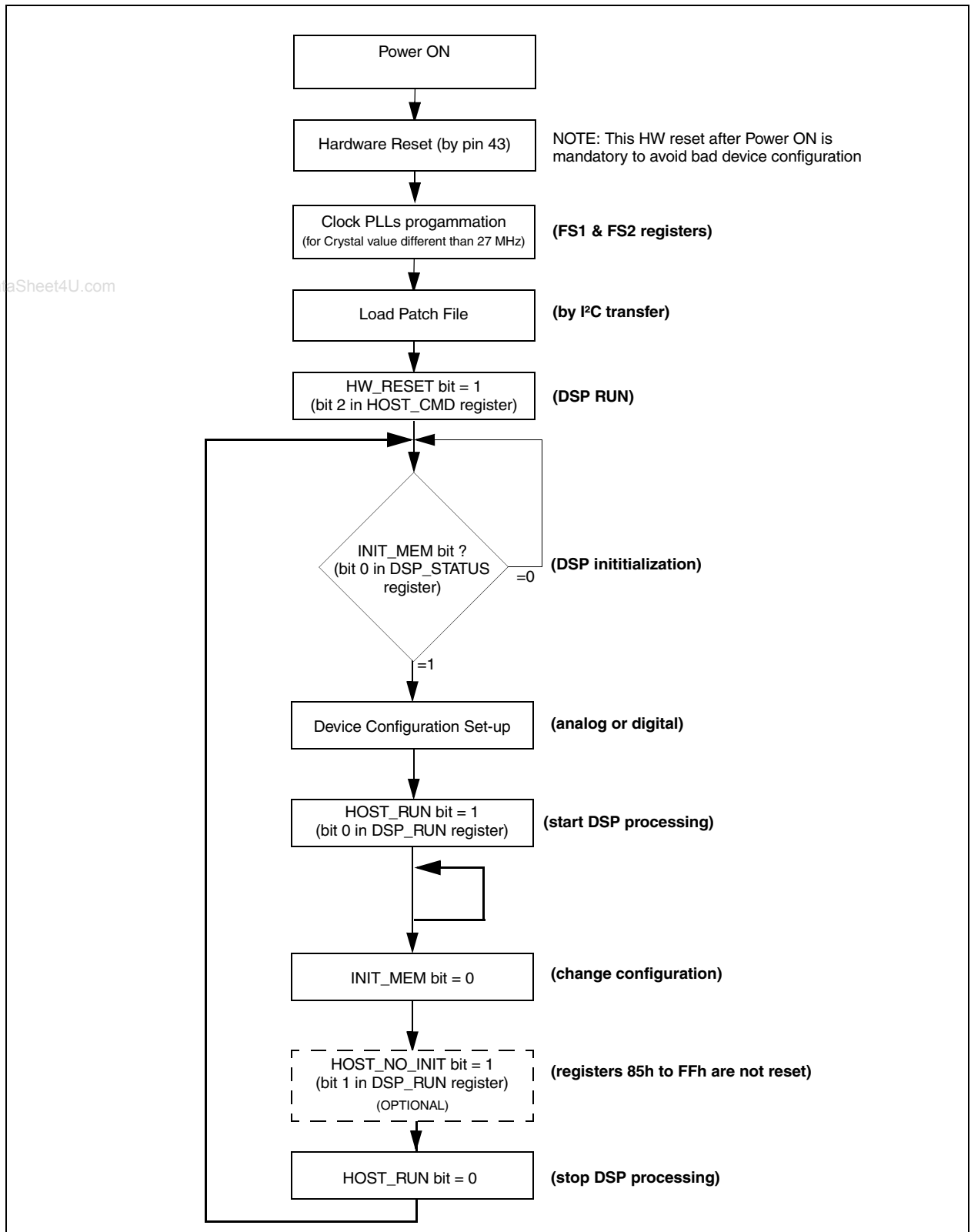
- Read Protocol

| | | | | | | | | | | | | | | |
|-------|---|---|-------------|---|------|-------|---|---|------|---|------|---|------|---|
| Start | W | A | Sub-address | A | Stop | Start | R | A | Data | A | | A | Data | N |
|-------|---|---|-------------|---|------|-------|---|---|------|---|------|---|------|---|

- W = Write address,
- R = Read address,
- A = Acknowledge,
- N = No acknowledge.
- Sub-address is the register address pointer; this value auto-increments for both write and read.

11.2 Start-up and Configuration Change Procedure

Figure 27: Flow chart



12 Register List

Note: The unused bits (defined as 'Reserved') in the I²C registers must be kept to zero.

The system clock registers (from address 08h to 0Bh and from address 5Ah to 5Dh) do not need to be modified if a standard 27 MHz quartz crystal oscillator is used.

The default values of the demodulator registers (from address 0Ch to 55h) are for optimum performances and any change is not recommended, except for:

- **AGC_GAIN** (0Fh) to adjust AGC gain for AM carrier in L/L' standard (AGC used in open loop).
- **CAROFFSET1** (22h) and **CAROFFSET2** (3Ah) to compensate IF carrier frequency with an out-of-standard offset.
- Soundlevel Prescaling **PRESCALE_AM** (94h), **PRESCALE_FM** (95h), **PRESCALE_NICAM** (96h) and **PRESCALE_SCART** (97h) to equalize demodulated or external audio signal before audio processing. Peak detector registers **PEAK_DET_INPUT** (9Dh), **PEAK_DET_L** (9Eh), **PEAK_DET_R** (9Fh), **PEAK_DET_L_R** (A0h) can be used to measure internal sound level.

Sound source selection for each audio output channel Loudspeakers, Headphone and SCART to be done using **AUDIO_MATRIX_INPUT** (A2h).

In Multi-lingual mode, **AUDIO_MATRIX_LANGUAGE** (A4h) selects separately the language for each audio output channel.

Register **AUTOSTD_CTRL** (8Ah) is used to select between L/L' or D/K/K1/K2/K3 standard which can be discriminated automatically. To be used also to change maximum FM deviation (125 kHz, by default) in case of wide overmodulation. **AUTOSTD_STANDARD_DETECT** (8Bh) and **AUTOSTD_STEREO_DETECT** (8Ch) to define the list of mono and stereo standards to be recognized automatically.

Note: () used in reset value column means that the bit or the byte is read-only.
 (S) symbol indicates that the field value is represented in signed binary format.
 (*) The field **AGC_ERR[4:0]** (**AGC_GAIN**) can be written by user if the bit **AGC_CMD** (**AGC_CTRL**) is set to one (by default controlled by Automatic Standard Recognition System). To be used to adjust manually the input gain of analog AGC amplifier for AM carrier (L/L').

12.1 I²C Register Map

By default, all I²C registers controlled by Automatic Standard Recognition System (Autostandard) are forced to Read-only mode for the user. These registers and bits are shaded in [Table 9](#).

Table 9: List of I²C Registers (Sheet 1 of 6)

| Name | Addr. | Reset | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|------------------------------|-------|-------------|------------------|-------------------------|-----------------|--------------|---------|-------------------|--------------|-----------|
| IC General Control | | | | | | | | | | |
| CUT_ID | 00h | (0000 0001) | 0 | 0 | CUT_NUMBER[5:0] | | | | | |
| RESET | 01h | 0000 0000 | BUS_EXP | I ² S_OUTPUT | 0 | EN_STBY | 0 | SOFT_LRST2 | SOFT_LRST1 | SOFT_RST |
| I2S_STAT | 05h | (0000 0000) | 0 | 0 | 0 | 0 | 0 | 0 | LR_OFF | LOCK_FLAG |
| I2S_SYNC_OFFSET | 06h | (0000 0000) | RESERVED | | | | | | | |
| Clocking 1 | | | | | | | | | | |
| SYS_CONFIG | 07h | 0000 0000 | I2S_CH_NB[1:0] | | INPUT_FREQ[3:0] | | | INPUT_CONFIG[1:0] | | |
| FS1_DIV | 08h | 0001 0010 | EN_PROG | 0 | NDIV1[1:0] | | 0 | SDIV1[2:0] | | |
| FS1_MD | 09h | 0001 0001 | 0 | 0 | 0 | MD1[4:0] | | | | |
| FS1_PE_H | 0Ah | 0011 0110 | PE_H1[7:0] | | | | | | | |
| FS1_PE_L | 0Bh | 0000 0000 | PE_L1[7:0] | | | | | | | |
| Demodulator | | | | | | | | | | |
| DEMOD_CTRL | 0Ch | 0000 0110 | 0 | 0 | FAR_MODE | GAP_MODE | AM_SEL | DEMOD_MODE[2:0] | | |
| DEMOD_STAT | 0Dh | (0000 0000) | 0 | 0 | 0 | QPSK_LK | FM2_CAR | FM2_SQ | FM1_CAR | FM1_SQ |
| AGC_CTRL | 0Eh | 0001 0001 | AGC_CMD | 0 | 0 | AGC_REF[2:0] | | | AGC_CST[1:0] | |
| AGC_GAIN | 0Fh | (0000 0000) | 0 | AGC_ERR[4:0] | | | | | SIG_OVER | SIG_UNDER |
| DC_ERR_IF | 10h | (0000 0000) | DC_ERR[7:0] | | | | | | | |
| Demodulator Channel 1 | | | | | | | | | | |
| CARFQ1H | 12h | 0011 1110 | CARFQ1[23:16] | | | | | | | |
| CARFQ1M | 13h | 1000 0000 | CARFQ1[15:8] | | | | | | | |
| CARFQ1L | 14h | 0000 0000 | CARFQ1[7:0] | | | | | | | |
| FIR1C0 | 15h | 0000 0000 | FIR1C0[7:0] (S) | | | | | | | |
| FIR1C1 | 16h | 1111 1110 | FIR1C1[7:0] (S) | | | | | | | |
| FIR1C2 | 17h | 1111 1100 | FIR1C2[7:0] (S) | | | | | | | |
| FIR1C3 | 18h | 1111 1101 | FIR1C3[7:0] (S) | | | | | | | |
| FIR1C4 | 19h | 0000 0010 | FIR1C4[7:0] (S) | | | | | | | |
| FIR1C5 | 1Ah | 0000 1101 | FIR1C5[7:0] (S) | | | | | | | |
| FIR1C6 | 1Bh | 0001 1000 | FIR1C6[7:0]6 (S) | | | | | | | |
| FIR1C7 | 1Ch | 0001 1111 | FIR1C7[7:0] (S) | | | | | | | |
| ACOEFF1 | 1Dh | 0010 0011 | ACOEFF1[7:0] | | | | | | | |
| BCOEFF1 | 1Eh | 0001 0010 | BCOEFF1[7:0] | | | | | | | |
| CRF1 | 1Fh | (0000 0000) | CRF1[7:0] (S) | | | | | | | |
| CETH1 | 20h | 0010 0000 | CETH1[7:0] | | | | | | | |
| SQTH1 | 21h | 0011 1100 | SQTH1[7:0] | | | | | | | |

Table 9: List of I²C Registers (Sheet 2 of 6)

| Name | Addr. | Reset | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|------------|-------|-----------|---------------------|-------|-------|-------|-------|-------|-------|-------|
| CAROFFSET1 | 22h | 0000 0000 | CAROFFSET1[7:0] (S) | | | | | | | |

Demodulator Channel 2

| | | | | | | | | | | |
|------------|-----|-------------|---------------------|------------|-------------|--------|-----------|---------------|--|--|
| IAGCR | 25h | 1000 1000 | IAGC_REF[7:0] | | | | | | | |
| IAGCC | 26h | 0000 0011 | IAGC_OFF | FAR_FLT_EN | MONO_FLT_EN | BG_SEL | MONO_PROG | IAGC_CST[2:0] | | |
| IAGCS | 27h | (0000 0000) | IAGC_CTRL[7:0] | | | | | | | |
| CARFQ2H | 28h | 0100 0100 | CARFQ2[23:16] | | | | | | | |
| CARFQ2M | 29h | 0100 0000 | CARFQ2[15:8] | | | | | | | |
| CARFQ2L | 2Ah | 0000 0000 | CARFQ2[7:0] | | | | | | | |
| FIR2C0 | 2Bh | 0000 0000 | FIR2C0[7:0] (S) | | | | | | | |
| FIR2C1 | 2Ch | 0000 0000 | FIR2C1[7:0] (S) | | | | | | | |
| FIR2C2 | 2Dh | 0000 0000 | FIR2C2[7:0] (S) | | | | | | | |
| FIR2C3 | 2Eh | 0000 0000 | FIR2C3[7:0] (S) | | | | | | | |
| FIR2C4 | 2Fh | 1111 1111 | FIR2C4[7:0] (S) | | | | | | | |
| FIR2C5 | 30h | 0000 0100 | FIR2C5[7:0] (S) | | | | | | | |
| FIR2C6 | 31h | 0001 0100 | FIR2C6[7:0] (S) | | | | | | | |
| FIR2C7 | 32h | 0010 0101 | FIR2C7[7:0] (S) | | | | | | | |
| ACOEFF2 | 33h | 1001 0000 | ACOEFF2[7:0] | | | | | | | |
| BCOEFF2 | 34h | 1010 1100 | BCOEFF2[7:0] | | | | | | | |
| SCOEFF | 35h | 0001 1100 | SCOEFF[7:0] | | | | | | | |
| SRF | 36h | (0000 0000) | SRF[7:0] (S) | | | | | | | |
| CRF2 | 37h | (0000 0000) | CRF2[7:0] (S) | | | | | | | |
| CETH2 | 38h | 0010 0000 | CETH2[7:0] | | | | | | | |
| SQTH2 | 39h | 0011 1100 | SQTH2[7:0] | | | | | | | |
| CAROFFSET2 | 3Ah | 0000 0000 | CAROFFSET2[7:0] (S) | | | | | | | |

NICAM

| | | | | | | | | | | |
|------------|-----|-------------|------------|--------|-----|----------|---|---------|----------|-----|
| NICAM_CTRL | 3Dh | 0000 0000 | 0 | 0 | 0 | 0 | 0 | DIF_POL | ECT | MAE |
| NICAM_BER | 3Eh | (0000 0000) | ERROR[7:0] | | | | | | | |
| NICAM_STAT | 3Fh | (0000 0000) | NIC_DET | F_MUTE | LOA | CBI[3:0] | | | NIC_MUTE | |

Stereo FM

| | | | | | | | | | | |
|----------|-----|-------------|---------------|----------|-------------|---|-------------|---------------|-------|-------|
| ZWT_CTRL | 40h | 0011 0001 | LRST_TONE_OFF | STD_MODE | THRESH[3:0] | | | TSCTRL[1:0] | | |
| ZWT_TIME | 41h | 0000 0100 | 0 | 0 | 0 | 0 | 0 | ZWT_TIME[2:0] | | |
| ZWT_STAT | 42h | (0000 0000) | 0 | 0 | 0 | 0 | ZW_STAT_RDY | ZW_DET | ZW_ST | ZW_DM |

Analog Control

| | | | | | | | | | | |
|----------------------|-----|-----------|---------------------|---------------------|---|---|--------------|---------------------|--|--|
| ADC_CTRL | 56h | 0000 1000 | I2S_DATA0_CTRL[1:0] | | 0 | 0 | ADC_POWER_UP | ADC_INPUT_SEL[2:0] | | |
| SCART1_2_OUTPUT_CTRL | 57h | 1010 1000 | SC2_MUTE | SC2_OUTPUT_SEL[2:0] | | | SC1_MUTE | SC1_OUTPUT_SEL[2:0] | | |
| SCART3_OUTPUT_CTRL | 58h | 0000 1011 | 0 | 0 | 0 | 0 | SC3_MUTE | SC3_OUTPUT_SEL[2:0] | | |

Clocking 2

Table 9: List of I²C Registers (Sheet 3 of 6)

| Name | Addr. | Reset | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|----------|-------|-----------|------------|------------|-------|----------|-------|------------|-------|-------|
| FS2_DIV | 5Ah | 0001 0001 | 0 | NDIV2[1:0] | | | 0 | SDIV2[2:0] | | |
| FS2_MD | 5Bh | 0001 0001 | 0 | 0 | 0 | MD2[4:0] | | | | |
| FS2_PE_H | 5Ch | 0101 1100 | PE_H2[7:0] | | | | | | | |
| FS2_PE_L | 5Dh | 0010 1001 | PE_L2[7:0] | | | | | | | |

DSP Control

| | | | | | | | | | | | |
|---------------|-----|-------------|-------------------|------------------|-------|-------------|--------------------------------------|-----------------------|-------------------------|-------------------|----------|
| HOST_CMD | 80h | 0000 0000 | IT_IN_DSP | 0 | 0 | 0 | 0 | HW_RESET | | | |
| IRQ_STATUS | 81h | 0000 0000 | | | | | IRQ3 (HP/Srmd unmute ready) | IRQ2 (HP detected) | IRQ1 (I2S sync lost) | IRQ0 (autostd) | |
| SOFT_VERSION | 82h | (0000 0002) | SOFT_VERSION[7:0] | | | | | | | | |
| ONCHIP_ALGOS | 83h | (0000 0000) | 0 | PRO_LOGIC_SELECT | NICAM | I2S_INPUT | TRUBASS | TRU SURROUND | PRO_LOGIC | MULTICHANNEL | |
| DSP_STATUS | 84h | 0000 0000 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | INIT_MEM | |
| DSP_RUN | 85h | 0000 0000 | | | | | 0 | 0 | HOST_NO_INIT | HOST_RUN | |
| I2S_IN_CONFIG | 86h | 1000 1110 | LOCK_MODE_EN | 0 | SYNC | LRCLK_START | LRCLK_POLARITY | SCLK_POLARITY | DATA_CFG | I2S_MODE | |
| AV_DELAY | 89h | 0000 0000 | DELAY_TIME[6:0] | | | | | | | | DELAY_ON |

Automatic Standard Recognition System

| | | | | | | | | | | |
|-------------------------|-----|-------------|--------------|--------------|-----------------|---------------|-----------------|-------------------|---------------|--------|
| AUTOSTD_CTRL | 8Ah | 0000 0001 | 0 | 0 | 0 | FORCE_SQUELCH | SINGLE_SHOT | DK_DEV[1:0] | | LDK_SW |
| AUTOSTD_STANDARD_DETECT | 8Bh | 0010 1111 | 0 | NICAM_C4_OFF | NICAM_GAP_MODE | NICAM_MONO_IN | LDK_SCK | I_SCK | BG_SCK | MN_SCK |
| AUTOSTD_STEREO_DETECT | 8Ch | 0001 1111 | LDK_ZWT3 | LDK_ZWT2 | LDK_SWT1 | LDK_NICAM | I_NICAM | BG_ZWT | BG_NICAM | MN_ZWT |
| AUTOSTD_TIMERS | 8Dh | 1010 0100 | FM_TIME[1:0] | | NICAM_TIME[2:0] | | | ZWEITON_TIME[2:0] | | |
| AUTOSTD_STATUS | 8Eh | (0000 0000) | STEREO_ID | STEREO_OK | MONO_OK | AUTOSTD_ON | STEREO_SID[1:0] | | MONO_SID[1:0] | |

Audio Preprocessing & Selection

| | | | | | | | | | | | |
|---------------------|-----|-------------|-----------------------|-------------------------|-------------------------|---------------------|------------------|----------|------------------|--------------|--|
| DC_REMOVAL_INPUT | 90h | 0000 0111 | 0 | 0 | 0 | 0 | 0 | DC_SCART | DC_NICAM | DC_DEMOD | |
| DC_REMOVAL_L | 91h | (0000 0000) | DC_REMOVAL_L[7:0] (S) | | | | | | | | |
| DC_REMOVAL_R | 92h | (0000 0000) | DC_REMOVAL_R[7:0] (S) | | | | | | | | |
| PRESCALE_SELECT | 93h | 0000 0000 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | AM_FM_SELECT | |
| PRESCALE_AM | 94h | 0000 0000 | 0 | PRESCALE_AM[6:0] (S) | | | | | | | |
| PRESCALE_FM | 95h | 0000 1100 | 0 | PRESCALE_FM[6:0] (S) | | | | | | | |
| PRESCALE_NICAM | 96h | 0001 1010 | 0 | PRESCALE_NICAM[6:0] (S) | | | | | | | |
| PRESCALE_SCART | 97h | 0000 0000 | 0 | 0 | PRESCALE_SCART[5:0] (S) | | | | | | |
| PRESCALE_I2S_0 | 98h | 0000 0000 | 0 | 0 | PRESCALE_I2S_0[5:0] (S) | | | | | | |
| PRESCALE_I2S_1 | 99h | 0000 0000 | 0 | 0 | PRESCALE_I2S_1[5:0] (S) | | | | | | |
| PRESCALE_I2S_2 | 9Ah | 0000 0000 | 0 | 0 | PRESCALE_I2S_2[5:0] (S) | | | | | | |
| DEEMPHASIS_DEMATRIX | 9Bh | 0000 0000 | 0 | 0 | NICAM_DEMATRIX | NICAM_DEEMPH_BYPASS | FM_DEMATRIX[1:0] | | FM_DEEMPH_BYPASS | FM_DEEMPH_SW | |

Table 9: List of I²C Registers (Sheet 4 of 6)

| Name | Addr. | Reset | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|----------------|-------|--------------|--------------------|---------------|----------------|-------|-------|---------------------|-------|-------|
| PEAK_DET_INPUT | 9Dh | 0000 0000 | PEAK_LOCATION | 0 | PEAK_L_R_RANGE | | | PEAK_DET_INPUT[1:0] | | |
| PEAK_DET_L | 9Eh | 0(0000 0000) | OVERLOAD_L [7:0] | PEAK_L[6:0] | | | | | | |
| PEAK_DET_R | 9Fh | 0(0000 0000) | OVERLOAD_R [7:0] | PEAK_R[6:0] | | | | | | |
| PEAK_DET_L_R | A0h | 0(0000 0000) | OVERLOAD_L_R [7:0] | PEAK_L_R[6:0] | | | | | | |

Matrixing

| | | | | | | | | | | |
|-----------------------|-----|-----------|-------------|--------------|---------------------|-----------------|-------------------------|--------------------|---------------------|-----------------|
| AUDIO_MATRIX_INPUT | A2h | 0000 0000 | 0 | 0 | 0 | 0 | 0 | SCART_INPUT_SOURCE | HP_INPUT_SOURCE | LS_INPUT_SOURCE |
| AUDIO_MATRIX_CONFIG | A3h | 0000 0000 | 0 | 0 | 0 | SCART_MATRIX | DEMOD_MATRIX[3:0] | | | |
| AUDIO_MATRIX_LANGUAGE | A4h | 0000 0000 | MUTE_STEREO | MUTE_ALL | SCART_LANGUAGE[1:0] | | HP_LANGUAGE[1:0] | | LS_LANGUAGE[1:0] | |
| DOWNMIX_IN_MODE | A6h | 0000 0010 | 0 | 0 | 0 | 0 | LFE_IN | MIX_IN_MODE[2:0] | | |
| DOWNMIX_OUT_MODE | A7h | 0100 1010 | 0 | HP_MODE[1:0] | | SCART_MODE[1:0] | | MIX_OUT_MODE[2:0] | | |
| DOWNMIX_DUAL_MODE | A8h | 0000 0000 | 0 | DUAL_ON | LS_DUAL_SELECT[1:0] | | SCART_DUAL_SELECT [1:0] | | HP_DUAL_SELECT[1:0] | |
| DOWNMIX_CONFIG | A9h | 0000 0001 | 0 | 0 | SRND_FACTOR[1:0] | | CENTER_FACTOR[1:0] | | LR_UPMIX | NORMALIZE |

Audio Processing

| | | | | | | | | | | |
|----------------------|-----|-----------|---------------------------|-------------------------|-------------------------|-----------------------|-------------------|-------------------|------------------|------------|
| PRO_LOGIC2_CONTROL | AAh | 0011 1010 | PL2_LFE | PL2_OUTPUT_DOWNMIX[2:0] | | | PL2_MODES[2:0] | | | PL2_ACTIVE |
| PCM_SRND_DELAY | ABh | 0000 0000 | 0 | 0 | 0 | SNRND_DELAY[4:0] | | | | |
| PCM_CENTER_DELAY | ACh | 0000 0000 | 0 | 0 | 0 | CENTER_DELAY[3:0] | | | | |
| PRO_LOGIC2_CONFIG | ADh | 0000 0000 | 0 | 0 | 0 | PL2_SRND_FILTER | PL2_RS_POLARITY | PL2_PANORAMA | PL2_AUTO BALANCE | |
| PRO_LOGIC2_DIMENSION | AEh | 0000 0000 | 0 | PL2_C_WIDTH | | | 0 | PL2_DIMENSION | | |
| PRO_LOGIC2_LEVEL | AFh | 0000 0000 | PL2_LEVEL | | | | | | | |
| NOISE_GENERATOR | B0h | 0000 0000 | 10_DB_ATTENUATE | SRIGHT_NOISE | SLEFT_NOISE | SUB_NOISE | CENTER_NOISE | RIGHT_NOISE | LEFT_NOISE | NOISE_ON |
| TRUSRND_CONTROL | B1h | 0000 0000 | 0 | TRUSRND_MONO_SRND | TRUSRND_INPUT_MODE[3:0] | | | | TRUSRND_MODE | TRUSRND_ON |
| TRUSRND_INPUT_GAIN | B6h | 0000 0000 | TRUSRND_INPUT_GAIN[7:0] | | | | | | | |
| TRUSRND_HP_DCL | B7h | 0000 0000 | 0 | 0 | 0 | 0 | 0 | DIALOG_CLARITY_ON | HEADPHONE_ON | 0 |
| TRUSRND_DC_ELEVATION | B8h | 0000 1100 | TRUSRND_DC_ELEVATION[7:0] | | | | | | | |
| TRUBASS_LS_CONTROL | BAh | 0000 0110 | 0 | 0 | 0 | TRUBASS_LS_SIZE[3:0] | | | TRUBASS_LS_ON | |
| TRUBASS_LS_LEVEL | BBh | 0000 1001 | TRUBASS_LS_LEVEL[7:0] | | | | | | | |
| TRUBASS_HP_CONTROL | BCh | 0000 0110 | 0 | 0 | 0 | TRUBASS_HP_SIZE[3:0] | | | TRUBASS_HP_ON | |
| TRUBASS_HP_LEVEL | BDh | 0000 1001 | TRUBASS_HP_LEVEL[7:0] | | | | | | | |
| SVC_LS_CONTROL | BEh | 0000 0010 | 0 | 0 | 0 | 0 | SVC_LS_INPUT[1:0] | | SVC_LS_AMP | SVC_LS_ON |
| SVC_LS_TIME_TH | BFh | 1001 1000 | SVC_LS_TIME[2:0] | | | SVC_LS_THRESHOLD[4:0] | | | | |
| SVC_HP_CONTROL | C0h | 0000 0010 | 0 | 0 | 0 | 0 | 0 | 0 | SVC_LHP_AMP | SVC_HP_ON |

Table 9: List of I²C Registers (Sheet 5 of 6)

| Name | Addr. | Reset | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|----------------------|-------|-----------|--------------------|------------------------|------------------|--------------------------|-------------------------|---------------|--------------------|-----------------|
| SVC_HP_TIME_TH | C1h | 1001 1000 | SVC_HP_TIME[2:0] | | | SVC_HP_THRESHOLD[4:0] | | | | |
| SVC_LS_GAIN | C2h | 0000 0000 | 0 | 0 | 0 | SVC_LS_MAKE_UP_GAIN[4:0] | | | | |
| SVC_HP_GAIN | C3h | 0000 0000 | 0 | 0 | 0 | SVC_HP_MAKE_UP_GAIN[4:0] | | | | |
| STSRND_CONTROL | C4h | 0000 0000 | | | | | | STSRND_STEREO | STSRND_MODE | STSRND_ON |
| STSRND_FREQ | C5h | 0001 0101 | 0 | 0 | STSRND_BASS[1:0] | | STSRND_MEDIUM[1:0] | | STSRND_TREBLE[1:0] | |
| STSRND_LEVEL | C6h | 1000 0000 | STSRND_GAIN[7:0] | | | | | | | |
| OMNISURROUND_CONTROL | C7h | 0000 0000 | | ST_VOICE | | | OMNISURROUND_INPUT_MODE | | | OMNISURROUND_ON |
| ST_DYNAMIC_BASS | C8h | 0000 0000 | BASS_LEVEL | | | | | BASS_FREQ | | DYN_BASS_ON |
| LS_EQ_BT_CTRL | C9h | 0000 0000 | 0 | 0 | 0 | 0 | 0 | 0 | LS_EQ_BT_SW | LS_EQ_ON |
| LS_EQ_BAND1 | CAh | 0000 0000 | EQ_BAND1[7:0] (S) | | | | | | | |
| LS_EQ_BAND2 | CBh | 0000 0000 | EQ_BAND2[7:0] (S) | | | | | | | |
| LS_EQ_BAND3 | CCh | 0000 0000 | EQ_BAND3[7:0] (S) | | | | | | | |
| LS_EQ_BAND4 | CDh | 0000 0000 | EQ_BAND4[7:0] (S) | | | | | | | |
| LS_EQ_BAND5 | CEh | 0000 0000 | EQ_BAND5[7:0] (S) | | | | | | | |
| LS_BASS_GAIN | CFh | 0000 0000 | LS_BASS[7:0] (S) | | | | | | | |
| LS_TREBLE_GAIN | D0h | 0000 0000 | LS_TREBLE[7:0] (S) | | | | | | | |
| HP_BT_CONTROL | D1h | 0000 0000 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | HP_BT_ON |
| HP_BASS_GAIN | D2h | 0000 0000 | HP_BASS[7:0] (S) | | | | | | | |
| HP_TREBLE_GAIN | D3h | 0000 0000 | HP_TREBLE[7:0] (S) | | | | | | | |
| OUTPUT_BASS_MNGT | D4h | 0000 0000 | BASS_MANAGE_ON | 0 | SUB_ACTIVE | GAIN_SWITCH | 0 | OCFG_NUM[2:0] | | |
| LS_LOUDNESS | D5h | 0000 0100 | 0 | LS_LOUD_THRESHOLD[2:0] | | | LS_LOUD_GAIN_HR[2:0] | | | LS_LOUD_ON |
| HP_LOUDNESS | D6h | 0000 0100 | 0 | HP_LOUD_THRESHOLD[2:0] | | | HP_LOUD_GAIN_HR[2:0] | | | HP_LOUD_ON |

Volume

| | | | | | | | | | | |
|-------------------|-----|-----------|------------------------|-----------------------|---|---|-------------------|------------------|------------------------|----------------|
| VOLUME_MODES | D7h | 1100 0111 | ANTCLIP_HP_VOL_CLAMP | ANTICLIP_LS_VOL_CLAMP | 0 | 0 | SCART_VOLUME_MODE | SRND_VOLUME_MODE | HP_VOLUME_MODE | LS_VOLUME_MODE |
| LS_L_VOLUME_MSB | D8h | 1001 1000 | LS_L_VOLUME_MSB[7:0] | | | | | | | |
| LS_L_VOLUME_LSB | D9h | 0000 0000 | 0 | 0 | 0 | 0 | 0 | 0 | LS_L_VOLUME_LSB[1:0] | |
| LS_R_VOLUME_MSB | DAh | 0000 0000 | LS_R_VOLUME_MSB[7:0] | | | | | | | |
| LS_R_VOLUME_LSB | DBh | 0000 0000 | 0 | 0 | 0 | 0 | 0 | 0 | LS_R_VOLUME_LSB[1:0] | |
| LS_C_VOLUME_MSB | DCh | 1001 1000 | LS_C_VOLUME_MSB[7:0] | | | | | | | |
| LS_C_VOLUME_LSB | DDh | 0000 0000 | 0 | 0 | 0 | 0 | 0 | 0 | LS_C_VOLUME_LSB[1:0] | |
| LS_SUB_VOLUME_MSB | DEh | 1001 1000 | LS_SUB_VOLUME_MSB[7:0] | | | | | | | |
| LS_SUB_VOLUME_LSB | DFh | 0000 0000 | 0 | 0 | 0 | 0 | 0 | 0 | LS_SUB_VOLUME_LSB[1:0] | |
| LS_SL_VOLUME_MSB | E0h | 1001 1000 | LS_SL_VOLUME_MSB[7:0] | | | | | | | |
| LS_SL_VOLUME_LSB | E1h | 0000 0000 | 0 | 0 | 0 | 0 | 0 | 0 | LS_SL_VOLUME_LSB[1:0] | |
| LS_SR_VOLUME_MSB | E2h | 0000 0000 | LS_SR_VOLUME_MSB[7:0] | | | | | | | |

Table 9: List of I²C Registers (Sheet 6 of 6)

| Name | Addr. | Reset | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|----------------------|-------|-----------|---------------------------|-------|-------|-------|-------|-------|---------------------------|-------|
| LS_SR_VOLUME_LSB | E3h | 0000 0000 | 0 | 0 | 0 | 0 | 0 | 0 | LS_SR_VOLUME_LSB[1:0] | |
| LS_MASTER_VOLUME_MSB | E4h | 1110 1000 | LS_MASTER_VOLUME_MSB[7:0] | | | | | | | |
| LS_MASTER_VOLUME_LSB | E5h | 0000 0000 | 0 | 0 | 0 | 0 | 0 | 0 | LS_MASTER_VOLUME_LSB[1:0] | |
| HP_L_VOLUME_MSB | E6h | 1001 1000 | HP_L_VOLUME_MSB[7:0] | | | | | | | |
| HP_L_VOLUME_LSB | E7h | 0000 0000 | 0 | 0 | 0 | 0 | 0 | 0 | HP_L_VOLUME_LSB[1:0] | |
| HP_R_VOLUME_MSB | E8h | 0000 0000 | HP_R_VOLUME_MSB[7:0] | | | | | | | |
| HP_R_VOLUME_LSB | E9h | 0000 0000 | 0 | 0 | 0 | 0 | 0 | 0 | HP_R_VOLUME_LSB[1:0] | |
| SCART_L_VOLUME_MSB | EAh | 1101 1101 | SCART_L_VOLUME_MSB[7:0] | | | | | | | |
| SCART_L_VOLUME_LSB | EBh | 0000 0000 | 0 | 0 | 0 | 0 | 0 | 0 | SCART_L_VOLUME_LSB[1:0] | |
| SCART_R_VOLUME_MSB | ECh | 1101 1101 | SCART_R_VOLUME_MSB[7:0] | | | | | | | |
| SCART_R_VOLUME_LSB | EDh | 0000 0000 | 0 | 0 | 0 | 0 | 0 | 0 | SCART_R_VOLUME_LSB[1:0] | |

Beeper

| | | | | | | | | | | |
|-----------------|-----|-----------|------------------|---|---|----------------------|---|--------------|------------------|-----------|
| BEEPER_ON | EEh | 0000 0000 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | BEEPER_ON |
| BEEPER_MODE | EFh | 0000 0011 | 0 | 0 | 0 | BEEPER_DURATION[1:0] | | BEEPER_PULSE | BEEPER_PATH[1:0] | |
| BEEPER_FREQ_VOL | F0h | 0111 0000 | BEEPER_FREQ[2:0] | | | BEEPER_VOLUME[4:0] | | | | |

Mute

| | | | | | | | | | | |
|--------------|-----|-----------|-----------------|---|---|--------------|----------------|------------|----------|-----------|
| MUTE_DIGITAL | F1h | 1001 1111 | AUTOSTD_MUTE_ON | 0 | 0 | SCART_D_MUTE | SRND_HP_D_MUTE | SUB_D_MUTE | C_D_MUTE | LS_D_MUTE |
|--------------|-----|-----------|-----------------|---|---|--------------|----------------|------------|----------|-----------|

S/PDIF

| | | | | | | | | | | |
|-------------------|-----|-----------|---|---|---|---|---|----------------|------------------------|--|
| S/PDIF_OUT_CONFIG | F2h | 0000 0100 | 0 | 0 | 0 | 0 | 0 | SPDIF_OUT_MUTE | S/PDIF_OUT_SELECT[2:0] | |
|-------------------|-----|-----------|---|---|---|---|---|----------------|------------------------|--|

Headphone Configuration

| | | | | | | | | | | |
|------------------|-----|-------------|---|---|---|---|----------|------------|---------------|-------------|
| HEADPHONE_CONFIG | F3h | 0000 001(0) | 0 | 0 | 0 | 0 | HP_FORCE | HP_LS_MUTE | HP_DET_ACTIVE | HP_DETECTED |
|------------------|-----|-------------|---|---|---|---|----------|------------|---------------|-------------|

DAC Control

| | | | | | | | | | | |
|----------------------|-----|-----------|----------------|---|------------|----------------|--------------|---------------|---------------|----------|
| DAC_CONTROL | F4h | 0001 1111 | 0 | 0 | S/PDIF_MUX | DAC_SCART_MUTE | DAC_SHP_MUTE | DAC_CSUB_MUTE | DAC_LSLR_MUTE | POWER_UP |
| SPDIF_CHANNEL_STATUS | F9h | 0000 0000 | CHANNEL_STATUS | | | EMPHASIS | | COPYRIGHT | NON_AUDIO | PRO_CON |

AutoStandard Coefficients Settings

| | | | | | | | | | | |
|-------------------------|-----|-----------|------------------------------|---|---|---|---|---|-------------------------|-------------------------|
| AUTOSTD_COEFF_CTRL | FBh | 0000 0001 | 0 | 0 | 0 | 0 | 0 | 0 | AUTOSTD_COEFF_CTRL[1:0] | |
| AUTOSTD_COEFF_INDEX_MSB | FCh | 0000 0000 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | AUTOSTD_COEFF_INDEX_MSB |
| AUTOSTD_COEFF_INDEX_LSB | FDh | 0000 0000 | AUTOSTD_COEFF_INDEX_LSB[7:0] | | | | | | | |
| AUTOSTD_COEFF_VALUE | FEh | 0000 0000 | AUTOSTD_COEFF_VALUE[7:0] | | | | | | | |

12.2 STV82x7 General Control Registers

CUT_ID

Version Identification

Address: 00h

Type: R

| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|-------|-------|-----------------|-------|-------|-------|-------|-------|
| 0 | 0 | CUT_NUMBER[5:0] | | | | | |

| Bit Name | Reset | Function |
|-----------------|--------|-----------------------------|
| Bits[7:6] | 00 | Reserved |
| CUT_NUMBER[5:0] | 000001 | Dice Version Identification |

RESET

Software Reset Register

Address: 01h

Type: R/W

| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---------|-------------------------|-------|---------|-------|------------|------------|----------|
| BUS_EXP | I ² S_OUTPUT | 0 | EN_STBY | 0 | SOFT_LRST2 | SOFT_LRST1 | SOFT_RST |

Description

The built-in Automatic Standard Recognition System (Autostandard) can be disabled. In this case, the Software Reset function (bits SOFT_LRST1 and SOFT_LRST2) can be used to implement the Automatic Standard Recognition by I²C Software. This is not required if the built-in Automatic Standard Recognition System function is used (default).

| Bit Name | Reset | Function |
|-------------------------|-------|--|
| BUS_EXP | 0 | Static control by I2C of hardware pin BUS_EXP |
| I ² S_OUTPUT | 0 | 0 = I ² S Input (I ² S output will be provided on I2S_DATA0 pin) 1 = I ² S Output (512 x fs will be provided on I2S_PCM_CLK pin) |
| Bit[5] | 0 | Reserved. |
| EN_STBY | 0 | Standby mode enabling 0: Normal mode 1: To lock the digital signals before to settle the device in standby mode |
| Bit 3 | 0 | Reserved. |
| SOFT_LRST2 | 0 | Softreset (active high) of Channel 2 detectors only. |
| SOFT_LRST1 | 0 | Softreset (active high) of Channel 1 detectors only. |
| SOFT_RST | 0 | General softreset (active high) to reset all hardware registers except for I ² C data. |

I2S_CTRL**I²S Synchronization Control Register**

Address: 04h

Type: R/W

| | | | | | | | |
|-------|-------|-------|-------|-------|-------|--------|-----------|
| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
| 0 | 0 | 0 | 0 | 0 | 0 | LR_OFF | LOCK_FLAG |

| Bit Name | Reset | Function |
|-----------|-------|--|
| Bits[7:2] | 0 | Reserved. |
| LR_OFF | 0 | LR Signal Detection 0: LR signal detected and correct 1: Missing LR pulses detected |
| LOCK_FLAG | 0 | Lock Flag allowing unmute of Audio Output |

I2S_STAT**I²S Synchronization Status Register**

Address: 05h

Type: R/W

| | | | | | | | |
|-------|-------|-------|-------|-------|-------|--------|-----------|
| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
| 0 | 0 | 0 | 0 | 0 | 0 | LR_OFF | LOCK_FLAG |

| Bit Name | Reset | Function |
|-----------|-------|--|
| Bits[7:2] | 0 | Reserved. |
| LR_OFF | 0 | LR Signal Detection 0: LR signal detected and correct 1: Missing LR pulses detected |
| LOCK_FLAG | 0 | Lock Flag allowing unmute of Audio Output |

I2S_SYNC_OFFSET**I²S Synchronization Offset Frequency Register**

Address: 06h

Type: R/W

12.3 Clocking 1

A low-jitter PLL Clock is integrated and can be fully reprogrammed using the registers described below. By default, the programming is defined for a 27-MHz quartz crystal frequency, which is the frequency recommended for reducing potential RF interference in the application. However, if

necessary, the PLL Clock can be re-programmed for other quartz crystal frequencies within a range from 23 to 30 MHz. Other quartz crystal frequencies can be programmed on your demand.

Note: A Crystal Frequency change is compatible with other default I²C programming including the built-in Automatic Standard Recognition System.

SYS_CONFIG**System Configuration Control Register**

Address: 07h

Type: R/W

| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|----------------|-----------------|-------|-------|-------------------|-------|-------|-------|
| I2S_CH_NB[1:0] | INPUT_FREQ[3:0] | | | INPUT_CONFIG[1:0] | | | |

www.DataSheet4U.com

| Bit Name | Reset | Function |
|-------------------|-------|--|
| I2S_CH_NB[1:0] | 00 | Number of I2S channels input 00: N/A 01: 2 channels 10: 4 channels 11: 6 channels |
| INPUT_FREQ[3:0] | 0000 | I2S Input frequency 0000 : 32 kHz 0001: 44.1 kHz 0010: 48 kHz 0011: 8 kHz (I2S input, 2 channels only) 0100 : 11.025 kHz (I2S input, 2 channels only) 0101 : 12 kHz (I2S input, 2 channels only) 0110 : 16 kHz (I2S input, 2 channels only) 0111 : 22.05 kHz (I2S input, 2 channels only) 1000 : 24 kHz (I2S input, 2 channels only) |
| INPUT_CONFIG[1:0] | 0 | Input stream to process 0 : SIF & SCART input (32 kHz) 1 : SCART input only (48 kHz) 2 : I2S input only |

FS1_DIV**FS1 I/O Divider Programming Register**

Address: 08h

Type: R/W

| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---------|-------|------------|-------|-------|------------|-------|-------|
| EN_PROG | 0 | NDIV1[1:0] | | 0 | SDIV1[2:0] | | |

| Bit Name | Reset | Function |
|----------|-------|---|
| EN_PROG | 0 | FS1 programming enable 0: FS1 I2C registers programming ignored by system - FS1 pre-programmed automatically by SYS-CONFIG register (normal use with standard quartz of 27 MHz) 1: FS1 I2C registers programming used by system - FS1 pre-programming by SYS-CONFIG deactivated (to be used in case of no standard quartz, different from 27 MHz) |

| Bit Name | Reset | Function |
|------------|-------|------------------------------------|
| Bit 6 | 0 | Reserved. |
| NDIV1[1:0] | 01 | FS1 Input clock divider selection |
| Bit 3 | 0 | Reserved. |
| SDIV1[2:0] | 010 | FS1 Output clock divider selection |

FS1_MD**FS1 Coarse Selection Register**

Address: 09h

Type: R/W

www.DataSheet4U.com

| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|-------|-------|-------|----------|-------|-------|-------|-------|
| 0 | 0 | 0 | MD1[4:0] | | | | |

| Bit Name | Reset | Function |
|-----------|-------|----------------------|
| Bits[7:5] | 000 | Reserved. |
| MD1[4:0] | 10001 | FS1 Coarse Selection |

FS1_PE_H**FS1 Fine Selection Register (MSBs)**

Address: 0Ah

Type: R/W

| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|------------|-------|-------|-------|-------|-------|-------|-------|
| PE_H1[7:0] | | | | | | | |

| Bit Name | Reset | Function |
|------------|--------------|---------------------------|
| PE_H1[7:0] | 0011 0110 | FS1 Fine Selection (MSBs) |

FS1_PE_L**FS1 Fine Selection Register (LSBs)**

Address: 0Bh

Type: R/W

| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|------------|-------|-------|-------|-------|-------|-------|-------|
| PE_L1[7:0] | | | | | | | |

| Bit Name | Reset | Function |
|------------|--------------|---------------------------|
| PE_L1[7:0] | 0000 0000 | FS1 Fine Selection (LSBs) |

12.4 Demodulator

DEMOD_CTRL

Demodulator Control Register

Address: 0Ch

Type: R/W

| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|-------|-------|----------|----------|--------|-----------------|-------|-------|
| 0 | 0 | FAR_MODE | GAP_MODE | AM_SEL | DEMOD_MODE[2:0] | | |

| Bit Name | Reset | Function | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|-----------------|---------------|---|--|---------------|--------------------|------|--------|-----------|------|------|---------|------|--------|-----------------------|------|------|-----------------------|------|--------|---------|------|------|-----------|------|--------|---------------|------|------|---------------|
| bit [7:6] | 000 | Reserved | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| FAR_MODE | 0 | 1: Farrow and Mono filter for NICAM active | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| GAP_MODE | 0 | Defines the clock gapping mode of the demodulator 0: (default), the FS1 freq is controlled by stl-error (clock-pll mode) to align the instantaneous value of the internal clock with respect to the received NICAM clock 1: the FS1 freq is fixed and the mean value of the internal clock is aligned by variable gapping (src-error) with respect to the received NICAM clock | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| AM_SEL | 0 | Demodulator Configuration Select 0: FM configuration of demodulator (Default) 1: AM configuration of demodulator | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| DEMOD_MODE[2:0] | 110 | Demodulator Mode Select <table border="0"> <thead> <tr> <th></th> <th><u>CH1 FM</u></th> <th><u>CH2 FM/QPSK</u></th> </tr> </thead> <tbody> <tr> <td>000:</td> <td>Normal</td> <td>FM Normal</td> </tr> <tr> <td>001:</td> <td>Wide</td> <td>FM Wide</td> </tr> <tr> <td>010:</td> <td>Normal</td> <td>QPSK System B/G/L/D/K</td> </tr> <tr> <td>011:</td> <td>Wide</td> <td>QPSK System B/G/L/D/K</td> </tr> <tr> <td>100:</td> <td>Normal</td> <td>FM Wide</td> </tr> <tr> <td>101:</td> <td>Wide</td> <td>FM Normal</td> </tr> <tr> <td>110:</td> <td>Normal</td> <td>QPSK System I</td> </tr> <tr> <td>111:</td> <td>Wide</td> <td>QPSK System I</td> </tr> </tbody> </table> | | <u>CH1 FM</u> | <u>CH2 FM/QPSK</u> | 000: | Normal | FM Normal | 001: | Wide | FM Wide | 010: | Normal | QPSK System B/G/L/D/K | 011: | Wide | QPSK System B/G/L/D/K | 100: | Normal | FM Wide | 101: | Wide | FM Normal | 110: | Normal | QPSK System I | 111: | Wide | QPSK System I |
| | <u>CH1 FM</u> | <u>CH2 FM/QPSK</u> | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 000: | Normal | FM Normal | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 001: | Wide | FM Wide | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 010: | Normal | QPSK System B/G/L/D/K | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 011: | Wide | QPSK System B/G/L/D/K | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 100: | Normal | FM Wide | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 101: | Wide | FM Normal | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 110: | Normal | QPSK System I | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 111: | Wide | QPSK System I | | | | | | | | | | | | | | | | | | | | | | | | | | | |

DEMOD_STAT

Demodulator Detection Status Register

Address: 0Dh

Type: R

| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|-------|-------|-------|---------|---------|--------|---------|--------|
| 0 | 0 | 0 | QPSK_LK | FM2_CAR | FM2_SQ | FM1_CAR | FM1_SQ |

| Bit Name | Reset | Function |
|-----------|-------|---|
| Bit [7:5] | 000 | Reserved. |
| QPSK_LK | 0 | QPSK Lock Detection Flag 0: Not detected 1: Detected |
| FM2_CAR | 0 | Channel 2 FM/AM Carrier Detection Flag 0: Not detected 1: Detected |
| FM2_SQ | 0 | Channel 2 FM Squelch Detection Flag 0: Not detected 1: Detected |
| FM1_CAR | 0 | Channel 1 FM/AM Carrier Detection Flag 0: Not detected 1: Detected |
| FM1_SQ | 0 | Channel 1 FM Squelch Detection Flag 0: Not detected 1: Detected |

Note: These registers allow direct access to the demodulator signal detectors.

AGC_CTRL**IF AGC Control Register**

Address: 0Eh

Type: R/W

| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---------|-------|-------|--------------|-------|--------------|-------|-------|
| AGC_CMD | 0 | 0 | AGC_REF[2:0] | | AGC_CST[1:0] | | |

| Bit Name | Reset | Function | | | | | | | | | | | | | | | | | | | | |
|-----------------------|-----------------------|--|----------------------------|--|-----------------------|--|------|-----------------------|------|-----------------|------|------|------|-------|------|------|------|--------|------|-------|------|----------------------------|
| AGC_CMD | 0 | Automatic Gain Control Command Mode Normally set to 0 enabling automatic mode. For L/L standards, the AGC should be switched off due to the presence of the AM sound carrier. In this case, a fixed gain value should be set using the AGCS register. 0: Automatic mode. AGC controlled by the Autostandard function. (Default) 1: Manual/Forced mode | | | | | | | | | | | | | | | | | | | | |
| Bits[6:5] | 00 | Reserved. | | | | | | | | | | | | | | | | | | | | |
| AGC_REF[2:0] | 100 | This bitfield is used to defines the clipping level which adjusts the allowable proportion of samples at the input of the ADC which will be clipped. The AGC tries to maximize the use of the full scale range of the ADC. The default setting gives a ratio of 1/256. <table border="0"> <thead> <tr> <th colspan="2"><u>Clipping Ratio</u></th> <th colspan="2"><u>Clipping Ratio</u></th> </tr> </thead> <tbody> <tr> <td>000:</td> <td>1/16 (Single carrier)</td> <td>100:</td> <td>1/256 (Default)</td> </tr> <tr> <td>001:</td> <td>1/32</td> <td>101:</td> <td>1/512</td> </tr> <tr> <td>010:</td> <td>1/64</td> <td>110:</td> <td>1/1024</td> </tr> <tr> <td>011:</td> <td>1/128</td> <td>111:</td> <td>1/2048 (Multiple carriers)</td> </tr> </tbody> </table> | <u>Clipping Ratio</u> | | <u>Clipping Ratio</u> | | 000: | 1/16 (Single carrier) | 100: | 1/256 (Default) | 001: | 1/32 | 101: | 1/512 | 010: | 1/64 | 110: | 1/1024 | 011: | 1/128 | 111: | 1/2048 (Multiple carriers) |
| <u>Clipping Ratio</u> | | <u>Clipping Ratio</u> | | | | | | | | | | | | | | | | | | | | |
| 000: | 1/16 (Single carrier) | 100: | 1/256 (Default) | | | | | | | | | | | | | | | | | | | |
| 001: | 1/32 | 101: | 1/512 | | | | | | | | | | | | | | | | | | | |
| 010: | 1/64 | 110: | 1/1024 | | | | | | | | | | | | | | | | | | | |
| 011: | 1/128 | 111: | 1/2048 (Multiple carriers) | | | | | | | | | | | | | | | | | | | |

| Bit Name | Reset | Function | | | | | | | | |
|--------------|-------|---|----|------|----|------|----|------|----|-------|
| AGC_CST[1:0] | 01 | <p>AGC Time Constant</p> <p>This is the time constant between each step of 1.5 dB by the AGC.</p> <p style="text-align: center;"><u>Step Duration (ms)</u></p> <table> <tr> <td>00</td> <td>1.33</td> </tr> <tr> <td>01</td> <td>2.66</td> </tr> <tr> <td>10</td> <td>5.33</td> </tr> <tr> <td>11</td> <td>10.66</td> </tr> </table> | 00 | 1.33 | 01 | 2.66 | 10 | 5.33 | 11 | 10.66 |
| 00 | 1.33 | | | | | | | | | |
| 01 | 2.66 | | | | | | | | | |
| 10 | 5.33 | | | | | | | | | |
| 11 | 10.66 | | | | | | | | | |

AGC_GAIN**IF AGC Control and Status Register**

Address: 0Fh

Type: R/W

| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|-------|--------------|-------|-------|-------|-------|----------|-----------|
| 0 | AGC_ERR[4:0] | | | | | SIG_OVER | SIG_UNDER |

| Bit Name | Reset | Function |
|--------------|-------|---|
| Bit 7 | 0 | Reserved. |
| AGC_ERR[4:0] | 00000 | <p>Amplifier Gain Control</p> <p>This is the Gain Control value of AGC. There are 20 steps of +1.5 dB (see Note below).</p> <p>00000: Gain-min 10100: Gain-min + 30db 11111: Gain-min + 30db</p> |
| SIG_OVER | 0 | <p>AGC Input Signal Upper Threshold</p> <p>0: Normal signal 1: Signal too large and AGC is overloaded</p> |
| SIG_UNDER | 0 | <p>AGC Input Signal Lower Threshold</p> <p>0: Normal signal 1: Signal too small and AGC is underloaded</p> <p>When the AGC is in Automatic mode (AGC_CMD = 0), bits SIG_OVER and SIG_UNDER indicate if the input signal is too small/large and the AGC is under/overloaded. This is useful when setting the STV82x7 SIF input level.</p> |

Note: When **AGC_CMD = 0**, **AGC_ERR[4:0]** can be read -- indicating the input level. It can also be written to -- presetting the AGC level which will then adjust itself to the final value.

When **AGC_CMD = 1**, the AGC is off and writing to **AGC_ERR[4:0]** directly controls the AGC amplifier gain. Reading AGC_ERR just confirms the fixed value.

DC_ERR_IF

DC Offset Status for IF ADC

Address: 10h

Type: R

Bit 7 Bit 6 Bit 5 Bit 4 Bit 3 Bit 2 Bit 1 Bit 0

DC_ERR[7:0]

| Bit Name | Reset | Function |
|-------------|----------|----------------------------------|
| DC_ERR[7:0] | 00000000 | DC offset error of IF ADC output |

12.5 Demodulator Channel 1

CARFQ1H, CARFQ1M, CARFQ1L Channel 1 Carrier DCO Frequency

Address: 12h to 14h

Type: R/W

Bit 7 Bit 6 Bit 5 Bit 4 Bit 3 Bit 2 Bit 1 Bit 0

CARFQ1[23:16], CARFQ1[15:8], CARFQ1[7:0]

| Bit Name | Reset | Function |
|---------------|----------|--|
| CARFQ1[23:16] | 00111110 | Channel 1 DCO Carrier Frequency (8 MSBs) |
| CARFQ1[15:8] | 10000000 | Channel 1 DCO Carrier Frequency |
| CARFQ1[7:0] | 00000000 | Channel 1 DCO Carrier Frequency (8 LSBs), see Table 10 . |

Table 10: Mono Carrier Frequencies by System

| System | Mono Carrier Freq. (MHz) | CARFQ1[23:0] (dec) | CARFQ1[23:0] |
|-----------|--------------------------|--------------------|--------------|
| M/N | 4.5 | 3072000 | 2EE000h |
| B/G | 5.5 | 3754667 | 394AABh |
| I | 6.0 | 4096000 | 3E8000h |
| L | 6.5 | 4453717 | 43F555h |
| D/K/K1/K2 | 6.5 | 4437333 | 43B555h |

Note: Carrier Freq: $CARFQ1(dec) \cdot f_S / 2^{24}$ with $f_S = 24.576$ MHz (crystal oscillator frequency independent)

FIR1C[0:7]**Channel 1 FIR Coefficients**

Address: 15h to 1Ch

Type: R/W

Bit 7 Bit 6 Bit 5 Bit 4 Bit 3 Bit 2 Bit 1 Bit 0

FIR1C0[7:0] to FIR1C7[7:0]

Table 11: Channel 1 FIR Coefficients

| Bitfield | Description | | | | | |
|-------------|---------------|-----------|------------|------------|------------|-----|
| | (reset state) | | | | | |
| | FM 27 kHz | FM 50 kHz | FM 200 kHz | FM 350 kHz | FM 500 kHz | AM |
| FIR1C0[7:0] | FFh | 00h | 00h | 02h | 01h | 00h |
| FIR1C1[7:0] | FEh | FEh | 01h | 01h | 00h | FEh |
| FIR1C2[7:0] | FEh | FCh | 01h | FCh | 04h | FDh |
| FIR1C3[7:0] | 00h | FDh | FCh | 03h | FAh | FEh |
| FIR1C4[7:0] | 06h | 02h | 08h | 04h | 05h | 04h |
| FIR1C5[7:0] | 0Eh | 0Dh | F6h | F2h | 00h | 0Dh |
| FIR1C6[7:0] | 16h | 18h | F8h | 06h | F2h | 16h |
| FIR1C7[7:0] | 1Bh | 1Fh | 4Ah | 43h | 4Dh | 1Dh |

ACOEFF1**Channel 1 Baseband PLL Loop Filter Proportional Coefficient**

Address: 1Dh

Type: R/W

Bit 7 Bit 6 Bit 5 Bit 4 Bit 3 Bit 2 Bit 1 Bit 0

ACOEFF1[7:0]

| Bit Name | Reset | Function |
|--------------|----------|---|
| ACOEFF1[7:0] | 00100011 | Used to program the Proportional Coefficient of the baseband PLL loop filter (Channel 1) Defines the damping factor of the loop. For values, refer to Table 12 . |

BCOEFF1**Channel 1 Baseband PLL Loop Filter Integral Coefficient & DCO Gain**

Address: 1Eh

Type: R/W

Bit 7 Bit 6 Bit 5 Bit 4 Bit 3 Bit 2 Bit 1 Bit 0

BCOEFF1[7:0]

| Bit Name | Reset | Function |
|--------------|----------|---|
| BCOEFF1[7:0] | 00010010 | Used to program the Integral Coefficient of the baseband PLL loop filter and DCO gain Defines the bandwidth of the loop. For values, refer to Table 12 . |

Table 12: Baseband PLL Loop Filter Adjustment (FM Mode)

| FM Mode | Small | Standard | Medium | Wide* | A2 Standard |
|------------------|-------|----------|--------|-------|-------------|
| ACOEFF | 10h | 22h | 2Ch | 2Ch | 10h |
| BCOEFF | 1Ah | 12h | 0Ah | 0Ah | 11h |
| FM_DEV max (kHz) | 62.5 | 125 | 250 | 500 | 125 |
| DCO Range (kHz) | 96 | 192 | 384 | 768 | 192 |

(*) Refer to [DEMOD_CTRL](#) (DEMOD_MODE[2:0])**CRF1****Channel 1 Baseband PLL Demodulator Offset**

Address: 1Fh

Type: R

Bit 7 Bit 6 Bit 5 Bit 4 Bit 3 Bit 2 Bit 1 Bit 0

CRF1[7:0]

| Bit Name | Reset | Function |
|-----------|------------|---|
| CRF1[7:0] | (00000000) | Channel 1 Carrier Recovery Frequency Displays the instantaneous frequency offset of the Channel 1 Baseband PLL Demodulator. |

CETH1**Channel 1 FM/AM Carrier Level Threshold**

Address: 20h

Type: R/W

Bit 7 Bit 6 Bit 5 Bit 4 Bit 3 Bit 2 Bit 1 Bit 0

CETH1[7:0]

| Bit Name | Reset | Function | | | | | | | | | | | | | | | | | | | | |
|------------|----------------|--|---------------------------------------|----------------|------|----------------|-----|----|-----|-------------------------|-----|-----|-----|-----|-----|-----|-----|---------------------------------------|-----|---------------|--|--|
| CETH1[7:0] | 00100000 | <p>This register is used to compare the carrier level in the channel and the threshold value. This level is measured after the channel filter and is relative to the full scale reference level (0 dB). This is used as part of the validation of an FM signal, if the carrier level is below the threshold, the signal is considered to be non-valid.</p> <table border="1"> <thead> <tr> <th>CETH</th> <th>Threshold (dB)</th> <th>CETH</th> <th>Threshold (dB)</th> </tr> </thead> <tbody> <tr> <td>FFh</td> <td>-6</td> <td>10h</td> <td>-32 (Recommended Value)</td> </tr> <tr> <td>80h</td> <td>-12</td> <td>08h</td> <td>-38</td> </tr> <tr> <td>40h</td> <td>-18</td> <td>00h</td> <td>OFF (all carrier levels are accepted)</td> </tr> <tr> <td>20h</td> <td>-24 (Default)</td> <td></td> <td></td> </tr> </tbody> </table> | CETH | Threshold (dB) | CETH | Threshold (dB) | FFh | -6 | 10h | -32 (Recommended Value) | 80h | -12 | 08h | -38 | 40h | -18 | 00h | OFF (all carrier levels are accepted) | 20h | -24 (Default) | | |
| CETH | Threshold (dB) | CETH | Threshold (dB) | | | | | | | | | | | | | | | | | | | |
| FFh | -6 | 10h | -32 (Recommended Value) | | | | | | | | | | | | | | | | | | | |
| 80h | -12 | 08h | -38 | | | | | | | | | | | | | | | | | | | |
| 40h | -18 | 00h | OFF (all carrier levels are accepted) | | | | | | | | | | | | | | | | | | | |
| 20h | -24 (Default) | | | | | | | | | | | | | | | | | | | | | |

SQTH1**Channel 1 FM Squelch Threshold Register**

Address: 21h

Type: R/W

Bit 7 Bit 6 Bit 5 Bit 4 Bit 3 Bit 2 Bit 1 Bit 0

SQTH1[7:0]

| Bit Name | Reset | Function | | | | | | | | | | | | |
|------------|--------------|---|------|----------|-----|---|-----|----|-----|--------------|-----|----|-----|----|
| SQTH1[7:0] | 00111100 | <p>The squelch detector measures the level of high frequency noise (> 40 kHz) and compares it to the threshold level (SQTH). If the level is below this value, the S/N of the FM signal is considered to be acceptable. Values are given for FM with standard deviation.</p> <table border="1"> <thead> <tr> <th>SQTH</th> <th>S/N (dB)</th> </tr> </thead> <tbody> <tr> <td>FAh</td> <td>0</td> </tr> <tr> <td>77h</td> <td>10</td> </tr> <tr> <td>3Ch</td> <td>15 (Default)</td> </tr> <tr> <td>23h</td> <td>20</td> </tr> <tr> <td>19h</td> <td>25</td> </tr> </tbody> </table> | SQTH | S/N (dB) | FAh | 0 | 77h | 10 | 3Ch | 15 (Default) | 23h | 20 | 19h | 25 |
| SQTH | S/N (dB) | | | | | | | | | | | | | |
| FAh | 0 | | | | | | | | | | | | | |
| 77h | 10 | | | | | | | | | | | | | |
| 3Ch | 15 (Default) | | | | | | | | | | | | | |
| 23h | 20 | | | | | | | | | | | | | |
| 19h | 25 | | | | | | | | | | | | | |

CAROFFSET1**Channel 1 DCO Carrier Offset Compensation**

Address: 22h

Type: R/W

Bit 7 Bit 6 Bit 5 Bit 4 Bit 3 Bit 2 Bit 1 Bit 0

CAROFFSET1[7:0] (S)

| Bit Name | Reset | Function |
|-----------------|----------|--|
| CAROFFSET1[7:0] | 00000000 | <p>This value is used to correct the carrier frequency offset of the incoming IF signal. Automatic frequency control in FM mode can be implemented by registers DC_REMOVAL_L and DC_REMOVAL_R.</p> <p>A DCO frequency offset (in two's complement format) is added to the pre-programming value by AUTOTSD in the CARFQ1 registers (corresponding to the standard IF carrier frequency). The programmable carrier offset ranges from -192 kHz to +190.5 kHz with a resolution of 1.5 kHz.</p> <p>For standard FM deviation, the value displays by DC_REMOVAL_L and DC_REMOVAL_R can be directly loaded in CAROFFSET1 to exactly compensate the carrier offset on Channel 1</p> |

12.6 Demodulator Channel 2

IAGCR

Channel 2 Internal AGC Reference for QPSK

Address: 25h

Type: R/W

| | | | | | | | |
|---------------|-------|-------|-------|-------|-------|-------|-------|
| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
| IAGC_REF[7:0] | | | | | | | |

| Bit Name | Reset | Function |
|---------------|----------|--|
| IAGC_REF[7:0] | 10001000 | Sets the mean value of the internal AGC, used for QPSK demodulation. The default setting corresponds to half full scale amplitude at the baseband PLL input. |

IAGCC

Channel 2 Internal AGC Time Constant for QPSK

Address: 26h

Type: R/W

| | | | | | | | |
|----------|------------|-------------|--------|-----------|---------------|-------|-------|
| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
| IAGC_OFF | FAR_FLT_EN | MONO_FLT_EN | BG_SEL | MONO_PROG | IAGC_CST[2:0] | | |

| Bit Name | Reset | Function | | | | | | | | | | | | | | | | | | | | | | | | |
|---------------|-------|--|-----|-----|-----|-----|-----|----|-----|-----|----|-----|----|----|-----|----|---|-----|----|---|-----|----|---|-----|-----|------|
| IAGC_OFF | 0 | AGC Disable 0: Internal AGC is active 1: Internal AGC is disabled | | | | | | | | | | | | | | | | | | | | | | | | |
| FAR_FLT_EN | 0 | 1: Enable Farrow filter for NICAM | | | | | | | | | | | | | | | | | | | | | | | | |
| MONO_FLT_EN | 0 | 1: Enable Mono filter for NICAM | | | | | | | | | | | | | | | | | | | | | | | | |
| BG_SEL | 0 | 1: BG NICAM Mono filter selected | | | | | | | | | | | | | | | | | | | | | | | | |
| MONO_PROG | 0 | 1: Enable programming of Mono filter | | | | | | | | | | | | | | | | | | | | | | | | |
| IAGC_CST[2:0] | 011 | <p>Internal AGC Programmable Step Constant.</p> <p>These bits control the time per step (values given for QPSK mode). The default value defines the optimum trade-off between fast settling time (for the fastest NICAM identification) and the noise immunity (minimum BER degradation)</p> <p style="text-align: center;"><u>Step time (us) Time Response (ms)</u></p> <table border="1" style="margin-left: 20px;"> <tr><td>000</td><td>703</td><td>128</td></tr> <tr><td>001</td><td>352</td><td>64</td></tr> <tr><td>010</td><td>176</td><td>32</td></tr> <tr><td>011</td><td>88</td><td>16</td></tr> <tr><td>100</td><td>44</td><td>8</td></tr> <tr><td>101</td><td>22</td><td>4</td></tr> <tr><td>110</td><td>11</td><td>2</td></tr> <tr><td>111</td><td>5.5</td><td>0.82</td></tr> </table> | 000 | 703 | 128 | 001 | 352 | 64 | 010 | 176 | 32 | 011 | 88 | 16 | 100 | 44 | 8 | 101 | 22 | 4 | 110 | 11 | 2 | 111 | 5.5 | 0.82 |
| 000 | 703 | 128 | | | | | | | | | | | | | | | | | | | | | | | | |
| 001 | 352 | 64 | | | | | | | | | | | | | | | | | | | | | | | | |
| 010 | 176 | 32 | | | | | | | | | | | | | | | | | | | | | | | | |
| 011 | 88 | 16 | | | | | | | | | | | | | | | | | | | | | | | | |
| 100 | 44 | 8 | | | | | | | | | | | | | | | | | | | | | | | | |
| 101 | 22 | 4 | | | | | | | | | | | | | | | | | | | | | | | | |
| 110 | 11 | 2 | | | | | | | | | | | | | | | | | | | | | | | | |
| 111 | 5.5 | 0.82 | | | | | | | | | | | | | | | | | | | | | | | | |

IAGCS

Channel 2 Internal AGC Status for QPSK

Address: 27h

Type: R

Bit 7 Bit 6 Bit 5 Bit 4 Bit 3 Bit 2 Bit 1 Bit 0

IAGC_CTRL[7:0]

| Bit Name | Reset | Function |
|----------------|----------|--|
| IAGC_CTRL[7:0] | 00000000 | Indicates the value of the internal AGC gain control |

www.DataSheet4U.com CARFQ2H, CARFQ2M, CARFQ2L Channel 2 Carrier DCO Frequency

Address: 28H to 2Ah

Type: R/W

Bit 7 Bit 6 Bit 5 Bit 4 Bit 3 Bit 2 Bit 1 Bit 0

CARFQ2[23:16], CARFQ2[15.8], CARFQ2[7:0]

| Bit Name | Reset | Function |
|---------------|----------|---|
| CARFQ2[23:16] | 01000100 | Channel 2 DCO Carrier Frequency (8 MSBs) |
| CARFQ2[15.8] | 01000000 | Channel 2 DCO Carrier Frequency |
| CARFQ2[7:0] | 00000000 | Channel 2 DCO Carrier Frequency (8 LSBs) See Table 13 . |

Table 13: Stereo Carrier Frequencies by System

| System | Stereo Carrier Freq. (MHz) | CARFQ2[23:0] (Dec) | CARFQ2[23:0] |
|-----------|----------------------------|--------------------|--------------|
| M/N A2+ | 4.724212 | 3225062 | 3135E6h |
| B/G NICAM | 5.85 | 3993600 | 3CF000h |
| BG A2 | 5.7421875 | 3920000 | 3BD080h |
| I NICAM | 6.552 | 4472832 | 444000h |
| L NICAM | 5.85 | 3993600 | 3CF000h |
| DK NICAM | 5.85 | 3993600 | 3CF000h |
| DK1 A2* | 6.258125 | 4272000 | 412F80h |
| DK2 A2* | 6.7421875 | 4602667 | 463B2Bh |
| DK3 A2* | 5.7421875 | 3920000 | 3BD080h |

FIR2C[0:7]**Channel 2 FIR Coefficients**

Address: 2Bh to 32h

Type: R/W

Bit 7 Bit 6 Bit 5 Bit 4 Bit 3 Bit 2 Bit 1 Bit 0

FIR2C0[7:0] to FIR2C7[7:0]

Table 14: Channel 2 FIR Coefficients

| Bitfield | Description | | | |
|-------------|-------------|-----------|----------|---------------------------|
| | FM 27 kHz | FM 50 kHz | QPSK 40% | (reset state) QPSK100% |
| FIR2C0[7:0] | FFh | 00h | 00h | 00h |
| FIR2C1[7:0] | FEh | FEh | 00h | 00h |
| FIR2C2[7:0] | FEh | FCh | FFh | 00h |
| FIR2C3[7:0] | 00h | FDh | 03h | 00h |
| FIR2C4[7:0] | 06h | 02h | 00h | FFh |
| FIR2C5[7:0] | 0Eh | 0Dh | F4h | 04h |
| FIR2C6[7:0] | 16h | 18h | 0Ah | 14h |
| FIR2C7[7:0] | 1Bh | 1Fh | 3Dh | 25h |

ACOEFF2**Channel 2 Baseband PLL Loop Filter Proportional Coefficient**

Address: 33h

Type: R/W

Bit 7 Bit 6 Bit 5 Bit 4 Bit 3 Bit 2 Bit 1 Bit 0

ACOEFF2[7:0]

| Bit Name | Reset | Function |
|--------------|----------|---|
| ACOEFF2[7:0] | 10010000 | This value defines the loop clamping factor used to program the Proportional Coefficient of the baseband PLL loop filter (Channel 2). See Table 15 and Table 16 . |

BCOEFF2**Channel 2 Baseband PLL Loop Filter Integral Coefficient & DCO Gain**

Address: 34h

Type: R/W

Bit 7 Bit 6 Bit 5 Bit 4 Bit 3 Bit 2 Bit 1 Bit 0

BCOEFF2[7:0]

| Bit Name | Reset | Function |
|--------------|----------|--|
| BCOEFF2[7:0] | 10101100 | This value defines the loop bandwidth used to program the Integral Coefficient of the Baseband PLL loop filter and DCO gain. See Table 15 and Table 16 . |

Table 15: Baseband PLL Loop Filter Adjustments (FM Mode)

| FM mode | Small | Standard | Mid | Wide | A2 standard |
|------------------|-------|----------|-----|------|-------------|
| ACOEFF | 10h | 22h | 2Ch | 2Ch | 10h |
| BCOEFF | 1Ah | 12h | 0Ah | 0Ah | 11h |
| FM_DEV max (kHz) | 62.5 | 125 | 250 | 500 | 125 |
| DCO Range (kHz) | 96 | 192 | 384 | 768 | 192 |

Table 16: Baseband PLL Loop Filter Adjustments (QPSK Mode)

| QPSK mode | Small | Medium | Large | Extra-large |
|-------------------|---------|--------|--------|-------------|
| ACOEFF | 90h | 90h | 90h | 90h |
| BCOEFF | ACh | A3h | 9Ah | 91h |
| DCO_DEV max (kHz) | 2.84375 | 5.6875 | 11.375 | 22.75 |

SCOEFF**Channel 2 Symbol Tracking Loop Coefficients**

Address: 35h

Type: R/W

Bit 7 Bit 6 Bit 5 Bit 4 Bit 3 Bit 2 Bit 1 Bit 0

SCOEFF[7:0]

| Bit Name | Reset | Function |
|-------------|----------|--|
| SCOEFF[7:0] | 00011100 | This value is used to program the proportional and integral coefficients of the QPSK Symbol tracking loop. See Table 17 and Table 18 . |

Table 17: QPSK System - BG/L/DK Standards (40% Roll-off)

| | Extra-Small | Small | Medium | Large | Extra-Large | Open Loop |
|--------|-------------|-------|--------|-------|-------------|-----------|
| SCOEFF | 1Eh | 25h | 24h | 26h | 2Ah | 80h |

Table 18: QPSK System - I Standard (100% Roll-off)

| | Extra-Small | Small | Medium | Large | Extra-Large |
|--------|-------------|-------|--------|-------|-------------|
| SCOEFF | 16h | 1Dh | 1Ch | 23h | 22h |

SRF

Channel 2 Symbol Tracking Loop Frequency

Address: 36h

Type: R/W

Bit 7 Bit 6 Bit 5 Bit 4 Bit 3 Bit 2 Bit 1 Bit 0

SRF[7:0]

| Bit Name | Reset | Function |
|----------|----------|---|
| SRF[7:0] | 00000000 | Displays in two's complement format the frequency deviation between the incoming NICAM bitstream and the quartz clocks. The maximum error is ± 250 ppm. |

www.DataSheet4U.com

CRF2

Channel 2 Baseband PLL Demodulator Offset

Address: 37h

Type: R

Bit 7 Bit 6 Bit 5 Bit 4 Bit 3 Bit 2 Bit 1 Bit 0

CRF2[7:0]

| Bit Name | Reset | Function |
|-----------|----------|---|
| CRF2[7:0] | 00000000 | Channel 2 Carrier Recovery Frequency. Displays the instantaneous frequency offset of the Channel 2 Baseband PLL |

CETH2

Channel 2 FM Carrier Level Threshold

Address: 38h

Type: R/W

Bit 7 Bit 6 Bit 5 Bit 4 Bit 3 Bit 2 Bit 1 Bit 0

CETH2[7:0]

| Bit Name | Reset | Function | | | | | | | | | | | | | | | | | | | | |
|-------------|-----------------------|--|---------------------------------------|-----------------------|-------------|-----------------------|-----|----|-----|-----|-----|-----|-----|-----|-----|-----|-----|---------------------------------------|-----|---------------|--|--|
| CETH2[7:0] | 00100000 | This register is used to compare the carrier level in the channel and the threshold value. This level is measured after the channel filter and is relative to the full scale reference level (0 dB). This is used as part of the validation of an FM signal, if the carrier level is below the threshold, the signal is considered to be non-valid. <table border="0"> <thead> <tr> <th><u>CETH</u></th> <th><u>Threshold (dB)</u></th> <th><u>CETH</u></th> <th><u>Threshold (dB)</u></th> </tr> </thead> <tbody> <tr> <td>FFh</td> <td>-6</td> <td>10h</td> <td>-32</td> </tr> <tr> <td>80h</td> <td>-12</td> <td>08h</td> <td>-38</td> </tr> <tr> <td>40h</td> <td>-18</td> <td>00h</td> <td>OFF (All carrier levels are accepted)</td> </tr> <tr> <td>20h</td> <td>-24 (Default)</td> <td></td> <td></td> </tr> </tbody> </table> | <u>CETH</u> | <u>Threshold (dB)</u> | <u>CETH</u> | <u>Threshold (dB)</u> | FFh | -6 | 10h | -32 | 80h | -12 | 08h | -38 | 40h | -18 | 00h | OFF (All carrier levels are accepted) | 20h | -24 (Default) | | |
| <u>CETH</u> | <u>Threshold (dB)</u> | <u>CETH</u> | <u>Threshold (dB)</u> | | | | | | | | | | | | | | | | | | | |
| FFh | -6 | 10h | -32 | | | | | | | | | | | | | | | | | | | |
| 80h | -12 | 08h | -38 | | | | | | | | | | | | | | | | | | | |
| 40h | -18 | 00h | OFF (All carrier levels are accepted) | | | | | | | | | | | | | | | | | | | |
| 20h | -24 (Default) | | | | | | | | | | | | | | | | | | | | | |

SQTH2**Channel 2 FM Squelch Threshold**

Address: 39h

Type: R/W

Bit 7 Bit 6 Bit 5 Bit 4 Bit 3 Bit 2 Bit 1 Bit 0

SQTH2[7:0]

| Bit Name | Reset | Function | | | | | | | | | | | | |
|------------|--------------|---|------|----------|-----|---|-----|----|-----|--------------|-----|----|-----|----|
| SQTH2[7:0] | 00111100 | <p>The squelch detector measures the level of high frequency noise (> 40 kHz) and compares it to the threshold level (SQTH). If the level is below this value, the S/N of the FM signal is considered to be acceptable. Values are given for FM with standard deviation.</p> <table border="1"> <thead> <tr> <th>SQTH</th> <th>S/N (dB)</th> </tr> </thead> <tbody> <tr> <td>FAh</td> <td>0</td> </tr> <tr> <td>77h</td> <td>10</td> </tr> <tr> <td>3Ch</td> <td>15 (Default)</td> </tr> <tr> <td>23h</td> <td>20</td> </tr> <tr> <td>19h</td> <td>25</td> </tr> </tbody> </table> | SQTH | S/N (dB) | FAh | 0 | 77h | 10 | 3Ch | 15 (Default) | 23h | 20 | 19h | 25 |
| SQTH | S/N (dB) | | | | | | | | | | | | | |
| FAh | 0 | | | | | | | | | | | | | |
| 77h | 10 | | | | | | | | | | | | | |
| 3Ch | 15 (Default) | | | | | | | | | | | | | |
| 23h | 20 | | | | | | | | | | | | | |
| 19h | 25 | | | | | | | | | | | | | |

CAROFFSET2**Channel 2 DCO Carrier Offset Compensation**

Address: 3Ah

Type: R/W

Bit 7 Bit 6 Bit 5 Bit 4 Bit 3 Bit 2 Bit 1 Bit 0

CAROFFSET2[7:0] (S)

| Bit Name | Reset | Function |
|-----------------|----------|---|
| CAROFFSET2[7:0] | 00000000 | <p>This value is used to correct the carrier frequency offset of the incoming IF signal. Automatic frequency control in FM mode can be implemented by registers DC_REMOVAL_L and DC_REMOVAL_R.</p> <p>A DCO frequency offset (in two's complement format) is added to the pre-programming value by AUTOTSD in the CARFQ2 registers (corresponding to the standard IF carrier frequency). The programmable carrier offset ranges from -192 kHz to +190.5 kHz with a resolution of 1.5 kHz.</p> <p>For standard FM deviation, the value displayed by register DC_REMOVAL_R can be directly loaded in register CAROFFSET2 to exactly compensate the carrier offset on Channel 2.</p> |

12.7 NICAM Registers**NICAM_CTRL****NICAM Decoder Control Register**

Address: 3Dh

Type: R/W

Bit 7 Bit 6 Bit 5 Bit 4 Bit 3 Bit 2 Bit 1 Bit 0

| | | | | | | | |
|---|---|---|---|---|---------|-----|-----|
| 0 | 0 | 0 | 0 | 0 | DIF_POL | ECT | MAE |
|---|---|---|---|---|---------|-----|-----|

| Bit Name | Reset | Function |
|-----------|-------|---|
| Bits[7:3] | 00000 | Reserved. |
| DIF_POL | 0 | 0: No polarity inversion (Default) 1: Polarity inversion of the differential decoding |
| ECT | 0 | Error Counter Timer: Defines the NICAM error measurement period 0: 128 ms (Default) 1: 64 ms |
| MAE | 0 | Max. Allowed Errors. Defines the NICAM error decoding for mute function. 0: 511 Max (Default) 1: 255 Max |

NICAM_BER**NICAM Bit Error Rate Register**

Address: 3Eh

Type: R

Bit 7 Bit 6 Bit 5 Bit 4 Bit 3 Bit 2 Bit 1 Bit 0

| |
|------------|
| ERROR[7:0] |
|------------|

| Bit Name | Reset | Function |
|------------|----------|----------------------------------|
| ERROR[7:0] | 00000000 | NICAM Error Counter Value |

NICAM_STAT**NICAM Detection Status Register**

Address: 3Fh

Type: R

Bit 7 Bit 6 Bit 5 Bit 4 Bit 3 Bit 2 Bit 1 Bit 0

| | | | | |
|---------|--------|-----|----------|----------|
| NIC_DET | F_MUTE | LOA | CBI[3:0] | NIC_MUTE |
|---------|--------|-----|----------|----------|

| Bit Name | Reset | Function |
|----------|-------|---|
| NIC_DET | 0 | NICAM Signal Detect 0: NICAM signal no detected 1: NICAM signal detected |
| F_MUTE | 0 | Frame Mute 0: No mute 1: Mute due to Superframe Alignment Loss |
| LOA | 0 | Loss of Frame Alignment Word (FAW) 0: No Alignment Lost 1: Frame Alignment Word Lost |
| CBI[3:0] | 0000 | Indicates the received NICAM control bits |
| NIC_MUTE | 0 | Indicates the NICAM decoder mute |

12.8 Stereo Mode

ZWT_CTRL

Zweiton Detector Control Register

Address: 40h

Type: R/W

| | | | | | | | |
|---------------|----------|-------------|-------|-------|-------------|-------|-------|
| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
| LRST_TONE_OFF | STD_MODE | THRESH[3:0] | | | TSCTRL[1:0] | | |

| Bit Name | Reset | Function | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|---------------|----------------------------|--|----------------------------|----------------------------|----------------|----------------------------|-------------------|----|------|----|------|------------------|--------------|-------|------|------|------------------|------|------|-------|------|------------------|------|------|----------------|-----|------------------|-------|------|-------|------|------|------|------|------|-------|------|-------|
| LRST_TONE_OFF | 0 | Control of the reset of the tone detector 0: Periodical reset of tone detection enabled 1: Periodical reset of tone detection disabled | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| STD_MODE_C | 0 | 0: German standard (Default) 1: Korean standard | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| THRESH[3:0] | 1100 | Defines the threshold of the detector for pilot and tone frequencies. <table border="1" style="margin-left: 40px;"> <thead> <tr> <th></th> <th>Level (% of the mid scale)</th> <th></th> <th>Level (% of the mid scale)</th> </tr> </thead> <tbody> <tr> <td>0000</td> <td>0</td> <td>1000</td> <td>50</td> </tr> <tr> <td>0001</td> <td>6.25</td> <td>1001</td> <td>56.25</td> </tr> <tr> <td>0010</td> <td>12.5</td> <td>1010</td> <td>62.5</td> </tr> <tr> <td>0011</td> <td>18.75</td> <td>1011</td> <td>68.75</td> </tr> <tr> <td>0100</td> <td>25</td> <td>1100 (Default)</td> <td>75</td> </tr> <tr> <td>0101</td> <td>31.25</td> <td>1101</td> <td>81.25</td> </tr> <tr> <td>0110</td> <td>37.5</td> <td>1110</td> <td>87.5</td> </tr> <tr> <td>0111</td> <td>43.75</td> <td>1111</td> <td>93.75</td> </tr> </tbody> </table> | | Level (% of the mid scale) | | Level (% of the mid scale) | 0000 | 0 | 1000 | 50 | 0001 | 6.25 | 1001 | 56.25 | 0010 | 12.5 | 1010 | 62.5 | 0011 | 18.75 | 1011 | 68.75 | 0100 | 25 | 1100 (Default) | 75 | 0101 | 31.25 | 1101 | 81.25 | 0110 | 37.5 | 1110 | 87.5 | 0111 | 43.75 | 1111 | 93.75 |
| | Level (% of the mid scale) | | Level (% of the mid scale) | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 0000 | 0 | 1000 | 50 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 0001 | 6.25 | 1001 | 56.25 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 0010 | 12.5 | 1010 | 62.5 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 0011 | 18.75 | 1011 | 68.75 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 0100 | 25 | 1100 (Default) | 75 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 0101 | 31.25 | 1101 | 81.25 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 0110 | 37.5 | 1110 | 87.5 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 0111 | 43.75 | 1111 | 93.75 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| TSCTRL[1:0] | 00 | Defines both the detection time and the error probability (reliability of the detection). <table border="1" style="margin-left: 40px;"> <thead> <tr> <th></th> <th>Sample Accumulation</th> <th>Decision Count</th> <th>Time (ms)</th> <th>Error Probability</th> </tr> </thead> <tbody> <tr> <td>00</td> <td>1024</td> <td>2</td> <td>256</td> <td>10⁻⁴</td> </tr> <tr> <td>01 (Default)</td> <td>1024</td> <td>3</td> <td>384</td> <td>10⁻⁶</td> </tr> <tr> <td>10</td> <td>2048</td> <td>2</td> <td>512</td> <td>10⁻⁷</td> </tr> <tr> <td>11</td> <td>2048</td> <td>3</td> <td>768</td> <td>10⁻⁹</td> </tr> </tbody> </table> | | Sample Accumulation | Decision Count | Time (ms) | Error Probability | 00 | 1024 | 2 | 256 | 10 ⁻⁴ | 01 (Default) | 1024 | 3 | 384 | 10 ⁻⁶ | 10 | 2048 | 2 | 512 | 10 ⁻⁷ | 11 | 2048 | 3 | 768 | 10 ⁻⁹ | | | | | | | | | | | |
| | Sample Accumulation | Decision Count | Time (ms) | Error Probability | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 00 | 1024 | 2 | 256 | 10 ⁻⁴ | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 01 (Default) | 1024 | 3 | 384 | 10 ⁻⁶ | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 10 | 2048 | 2 | 512 | 10 ⁻⁷ | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 11 | 2048 | 3 | 768 | 10 ⁻⁹ | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

ZWT_TIME

Zweiton Detector Timing Register

Address: 41h

Type: R/W

| | | | | | | | |
|-------|-------|-------|-------|-------|---------------|-------|-------|
| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
| 0 | 0 | 0 | 0 | 0 | ZWT_TIME[2:0] | | |

| Bit Name | Reset | Function |
|-----------|-------|-----------|
| Bit [7:3] | 00000 | Reserved. |

| Bit Name | Reset | Function |
|---------------|-------|--|
| ZWT_TIME[2:0] | 100 | Defines the period of the reset tone used for tone detection system reset. <u>Duration</u> (ms) |
| | | 000 256 |
| | | 001 512 |
| | | 010 768 |
| | | 011 1024 |
| | | 100 1280 |
| | | 101 1536 |
| | | 110 1792 |
| | | 111 2040 |

ZWT_STAT**Zweiton Status Register**

www.DataSheet4U.com

Address: 42h

Type: R

| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---------------|-------|-------|-------|-------------|--------|-------|-------|
| LRST_TONE_OFF | 0 | 0 | 0 | ZW_STAT_RDY | ZW_DET | ZW_ST | ZW_DM |

| Bit Name | Reset | Function |
|---------------|-------|--|
| LRST_TONE_OFF | 0 | Indicates the status of the control bit programmed in the reg ZWT-CTRL 0: Periodical reset of tone detection enabled 1: Periodical reset of tone detection disabled |
| Bits[6:4] | 000 | Reserved. |
| ZW_STAT_RDY | 0 | Periodic flag indicating when the tone detection flags are updated and ready to be read |
| ZW_DET | 0 | Pilot Detection Flag |
| ZW_ST | 0 | Stereo Tone Detection Flag |
| ZW_DM | 0 | Dual Mono Tone Detection Flag |

12.9 Analog Control**ADC_CTRL****Register Description**

Address: 56h

Type: R/W

| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---------------------|-------|-------|--------------|--------------------|-------|-------|-------|
| I2S_DATA0_CTRL[1:0] | 0 | 0 | ADC_POWER_UP | ADC_INPUT_SEL[2:0] | | | |

| Bit Name | Reset | Function |
|---------------------|-------|--|
| I2S_DATA0_CTRL[1:0] | 00 | 00 = SCART 01 = L, R 10 = HP or Srnd 11 = C/Sub |
| Bits[7:4] | 0000 | Reserved. |
| ADC_POWER_UP | 1 | Control of the power up of the Audio ADC 0: ADC in power down mode 1: Wake up of the ADC |
| ADC_INPUT_SEL [2:0] | 000 | Selection of the ADC input signal 000: SCART 1 (Default) 011: SCART 4 001: SCART 2 100: Mono input 010: SCART 3 Other: reserved |

SCART1_2_OUTPUT_CTRL Register Description

Address: 57h

Type: R/W

| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|----------|---------------------|-------|-------|----------|---------------------|-------|-------|
| SC2_MUTE | SC2_OUTPUT_SEL[2:0] | | | SC1_MUTE | SC1_OUTPUT_SEL[2:0] | | |

| Bit Name | Reset | Function |
|---------------------|-------|---|
| SC2_MUTE | 1 | Mute command for the output SCART 2 0: output not muted 1: output muted |
| SC2_OUTPUT_SEL[2:0] | 010 | Selection of the output SCART 2 configuration: 000: DSP 100: Input SCART 3 001: Mono input 101: Input SCART 4 010: Input SCART 1 (Default) Other: Reserved 011: Input SCART 2 |
| SC1_MUTE | 1 | Mute command for the output scart 1 0: output not muted 1: output muted |
| SC1_OUTPUT_SEL[2:0] | 000 | Selection of the output SCART 1 configuration: 000: DSP (Default) 100: Input SCART 3 001: Mono input 101: Input SCART 4 010: Input SCART 1 Other: Reserved 011: Input SCART 2 |

SCART3_OUTPUT_CTRL

Register Description

Address: 58h

Type: R/W

| | | | | | | | |
|-------|-------|-------|-------|----------|---------------------|-------|-------|
| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
| 0 | 0 | 0 | 0 | SC3_MUTE | SC3_OUTPUT_SEL[2:0] | | |

| Bit Name | Reset | Function |
|---------------------|-------|---|
| Bits[7:4] | 0000 | Reserved. |
| SC3_MUTE | 1 | Mute command for the output SCART 3 0: output not muted 1: output muted |
| SC3_OUTPUT_SEL[2:0] | 011 | Selection of the output SCART 3 configuration: 000: DSP 001: Mono input 010: Input SCART 1 011: Input SCART 2 (Default) 100: Input SCART 3 101: Input SCART 4 Other: Reserved |

12.10 Clocking 2

FS2_DIV

FS2 I/O Divider Programming Register

Address: 5Ah

Type: R/W

| | | | | | | | |
|-------|-------|------------|-------|-------|------------|-------|-------|
| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
| 0 | 0 | NDIV2[1:0] | | | SDIV2[2:0] | | |

| Bit Name | Reset | Function |
|------------|-------|------------------------------------|
| Bit [7:6] | 0 | Reserved. |
| NDIV2[1:0] | 01 | FS2 Input clock divider selection |
| Bit 4 | 0 | Reserved. |
| SDIV2[2:0] | 001 | FS2 Output clock divider selection |

FS2_MD

FS2 Coarse Selection Register

Address: 5Bh

Type: R/W

| | | | | | | | |
|-------|-------|-------|----------|-------|-------|-------|-------|
| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
| 0 | 0 | 0 | MD2[4:0] | | | | |

| Bit Name | Reset | Function |
|-----------|-------|----------------------|
| Bits[7:5] | 000 | Reserved. |
| MD2[4:0] | 10001 | FS2 Coarse Selection |

FS2_PE_H**FS2 Fine Selection Register (MSBs)**

Address: 5Ch

Type: R/W

Bit 7 Bit 6 Bit 5 Bit 4 Bit 3 Bit 2 Bit 1 Bit 0

PE_H2[7:0]

www.DataSheet4U.com

| Bit Name | Reset | Function |
|------------|--------------|---------------------------|
| PE_H2[7:0] | 0101 1100 | FS2 Fine Selection (MSBs) |

FS2_PE_L**FS2 Fine Selection Register (LSBs)**

Address: 5Dh

Type: R/W

Bit 7 Bit 6 Bit 5 Bit 4 Bit 3 Bit 2 Bit 1 Bit 0

PE_L2[7:0]

| Bit Name | Reset | Function |
|------------|--------------|---------------------------|
| PE_L2[7:0] | 0010 1001 | FS2 Fine Selection (LSBs) |

12.11 DSP Control**HOST_CMD****DSP Hardware Control Register**

Address: 80h

Type: R/W

Bit 7 Bit 6 Bit 5 Bit 4 Bit 3 Bit 2 Bit 1 Bit 0

| | | | | | | | |
|-----------|---|---|---|---|----------|--|--|
| IT_IN_DSP | 0 | 0 | 0 | 0 | HW_RESET | | |
|-----------|---|---|---|---|----------|--|--|

| Bit Name | Reset | Function |
|-----------|-------|------------------|
| IT_IN_DSP | 0 | Valid I2C table. |
| Bits[6:3] | 0000 | Reserved. |

| Bit Name | Reset | Function |
|-----------|-------|------------------------------|
| HW_RESET | 0 | DSP Hardware reset when set. |
| Bits[1:0] | 00 | Reserved. |

IRQ_STATUS**IRQ Status Register**

Address: 81h

Type: R/W

| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|-------|-------|-------|-------|-------|-------|-------|-------|
| IRQ7 | IRQ6 | IRQ5 | IRQ4 | IRQ3 | IRQ2 | IRQ1 | IRQ0 |

www.DataSheet4U.com

| Bit Name | Reset | Function |
|-----------|-------|-------------------------------|
| Bits[7:4] | 0000 | Reserved. |
| IRQ3 | 0 | Unmute HP/Srnd DAC IRQ |
| IRQ2 | 0 | HP connection/deconnectionIRQ |
| IRQ1 | 0 | I2S lock lostIRQ |
| IRQ0 | 0 | Auto-Standard IRQ |

SOFT_VERSION**Embedded Software Version Register**

Address: 82h

Type: R

| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|-------------------|-------|-------|-------|-------|-------|-------|-------|
| SOFT_VERSION[7:0] | | | | | | | |

| Bit Name | Reset | Function |
|-------------------|--------------|-----------------------------------|
| SOFT_VERSION[7:0] | 0000 0002 | Version of the Embedded software. |

ONCHIP_ALGOS**Register Description**

Address: 83h

Type: R

| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|-------|------------------|-------|-----------|---------|--------------|-----------|--------------|
| 0 | PRO_LOGIC_SELECT | NICAM | I2S_INPUT | TRUBASS | TRU SURROUND | PRO_LOGIC | MULTICHANNEL |

| Bit Name | Reset | Function |
|------------------|-------|---|
| Bit 7 | 0 | Reserved. |
| PRO_LOGIC_SELECT | 0 | 0: Dolby Pro Logic I 1: Dolby Pro Logic II |
| NICAM | 0 | NICAM Demodulator is present when set. |
| I2S_INPUT | 0 | 0: 1 I2S input 1: 3 I2S inputs |
| DIALOG_CLARITY | 0 | SRS Dialog Clarity algorithm is present when set. |
| TRUBASS | 0 | SRS Trubass algorithm is present when set. |
| TRUSURROUND | 0 | SRS Trusurround algorithm is present when set. |
| PRO_LOGIC | 0 | Dolby Pro Logic algorithm is present when set. |
| MULTICHANNEL | 0 | Multichannels output is present when set. |

DSP_STATUS**DSP Status Register**

Address: 84h

Type: R

| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|-------|-------|-------|-------|-------|-------|-------|----------|
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | INIT_MEM |

| Bit Name | Reset | Function |
|-----------|---------|---|
| Bits[7:1] | 0000000 | Reserved. |
| INIT_MEM | 0 | DSP Initialization 0: DSP is not initialized. 1: DSP is initialized. |

DSP_RUN**Register Description**

Address: 85h

Type: R/W

| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|-----------|-------|-------|-------|-------|-------|--------------|----------|
| TEST_MODE | | | | 0 | 0 | HOST_NO_INIT | HOST_RUN |

| Bit Name | Reset | Function |
|----------------------|-------|---|
| TEST_MODE_INPUT[7:6] | 00 | active in TEST_MODE = 1 (bypass processing) 0: I2S_0 copied to SCART and SPDIF outputs 1: I2S_1 copied to SCART and SPDIF outputs 2: I2S_2 copied to SCART and SPDIF outputs |

| Bit Name | Reset | Function |
|----------------|-------|--|
| TEST_MODE[5:4] | 00 | 0: standard configuration 1: bypass processing configuration 2: Clock Loop test |
| Bits[3:2] | 00 | Reserved |
| HOST_NO_INIT | 0 | 0: I2C register table is initialized when we soft reset 1: I2C register table is not initialized when we soft reset |
| HOST_RUN | 0 | 0: soft reset DSP 1: start DSP processing |

I2S_IN_CONFIG**I²S Configuration Register**

Address: 86h

Type: R/W

| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|--------------|-------|-------|-------------|----------------|---------------|----------|----------|
| LOCK_MODE_EN | 0 | SYNC | LRCLK_START | LRCLK_POLARITY | SCLK_POLARITY | DATA_CFG | I2S_MODE |

| Bit Name | Reset | Function |
|----------------|-------|---|
| LOCK_MODE_EN | 1 | 0: Disable Lock Mode for external I2S input 1: Enable Lock Mode for external I2S input |
| Bit 6 | 0 | Reserved. |
| SYNC | 0 | I2S synchronisation: 0: Capture directly 1: Wait for synchro |
| LRCLK_START | 0 | according to LRCLK POLARITY, first data take: 0: Left 1: Right |
| LRCLK_POLARITY | 0 | Polarity of the left data |
| SCLK_POLARITY | 1 | 0: Falling edge 1: Rising edge |
| DATA_CFG | 1 | 0: LSB First 1: MSB First |
| I2S_MODE | 0 | 0: Non standard mode 1: Standard mode (Refer to Figure 26) |

AV_DELAY**Audio/Video Delay Register**

Address: 89h

Type: R/W

| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|------------|-------|-------|-------|-------|-------|-------|----------|
| DELAY_TIME | | | | | | | DELAY_ON |

| Bit Name | Reset | Function |
|------------|----------|--|
| DELAY_TIME | 00000000 | Audio Delay Time 0000000: 0 ms ... 0111100: 60 ms (48kHz) ... 1011010: 90 ms (32kHz) |
| DELAY_ON | 0 | Audio/video delay is enabled when set. |

Note: AV_DELAY acts on both LS and HP paths simultaneously (same delay).

12.12 Automatic Standard Recognition

AUTOSTD_CTRL

Automatic Standard Recognition Control Register

Address: 8Ah

Type: R/W

| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|-------|-------|-------|---------------|-------------|-------------|-------|--------|
| 0 | 0 | 0 | FORCE_SQUELCH | SINGLE_SHOT | DK_DEV[1:0] | | LDK_SW |

| Bit Name | Reset | Function |
|---------------|-------|--|
| Bits[7:5] | 000 | Reserved. |
| FORCE_SQUELCH | 0 | Allow to force squelch detection 0: FM squelch is taken into consideration for MONO detection 1: FM squelch is not taken into consideration for MONO detection |
| SINGLE_SHOT | 0 | Single Shot Mode Selection 0: Single Shot mode is not selected 1: Single Shot mode is selected ¹ |
| DK_DEV[1:0] | 00 | Selects FM deviation configuration to take into account of overmodulation in DK_NICAM standard. 00: FM 50 kHz (Default) 10: FM 350 kHz 01: FM 200 kHz 11: FM 500 kHz |
| LDK_SW | 1 | Makes exclusive the auto search of DK/K1/K2/K3 and L/L' standard 0: DK/K1/K2/K3 standard auto-search / L/L' disabled 1: L/L' standard auto-search / DK/K1/K2/K3 disabled |

1. **Single Shot** mode can be used before disabling the Automatic Standard Recognition (Autostandard) to pre-program demodulator registers in a defined standard and reduce I²C programming in Manual mode

Note: Only standard deviation FM 50K kHz is compatible with other D/K1/K2/K3 standards in Automatic Standard Recognition Search mode.

FM deviation superior to 350 kHz will degrade strongly NICAM reception due to overlapping of FM and QPSK IF spectrum in DK-NICAM standard.

L/L' and DK/K1/K2/K3 standard cannot be discriminated in Automatic Standard Recognition Search mode because the same frequency is used for the mono IF carrier.

AUTOSTD_STANDARD_DETECT Auto Standard Check Standard Register

Address: 8Bh

Type: R/W

| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|-------|------------------|--------------------|-------------------|---------|-------|--------|--------|
| 0 | NICAM_C4_O FF | NICAM_GAP_ MODE | NICAM_MON O_IN | LDK_SCK | I_SCK | BG_SCK | MN_SCK |

| Bit Name | Reset | Function |
|----------------|-------|--|
| NICAM_C4_OFF | 0 | 0: Autostandard will consider the C4 bit for MONO backup 1: Autostandard will ignore the C4 bit for MONO backup |
| NICAM_GAP_MODE | 1 | 0: NICAM, fast search 1: NICAM, slow search (no perturbations on LEFT channel in search mode) |
| NICAM_MONO_IN | 0 | 0: the MONO backup for NICAM comes from internal demodulator 1: the MONO backup for NICAM comes from MONO input |
| LDK_SCK | 1 | L/L' or D/K Mono Standard Enable 0: Disabled 1: Enabled |
| I_SCK | 1 | I Mono Standard Enable 0: Disabled 1: Enabled |
| BG_SCK | 1 | B/G Mono Standard Enable 0: Disabled 1: Enabled |
| MN_SCK | 1 | M/N Mono Standard Enable 0: Disabled 1: Enabled |

Note: Autostandard is off when all mono standards are disabled (LDK_SCK = 0, I_SCK = 0, BG_SCK = 0 and MN_SCK = 0).

AUTOSTD_STEREO_DETECT Auto Standard Check Stereo Register

Address: 8Ch

Type: R/W

| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|----------|----------|----------|---------|-------|--------|--------|--------|
| LDK_ZWT3 | LDK_ZWT2 | LDK_ZWT1 | LDK_NIC | I_NIC | BG_ZWT | BG_NIC | MN_ZWT |

| Bit Name | Reset | Function |
|----------|-------|---|
| LDK_ZWT3 | 0 | D/K3 Zweiton (A2*) Stereo Standard Enable 0: Disabled 1: Enabled |
| LDK_ZWT2 | 0 | D/K2 Zweiton (A2*) Stereo Standard Enable 0: Disabled 1: Enabled |
| LDK_ZWT1 | 0 | D/K1 Zweiton (A2*) Stereo Standard Enable 0: Disabled 1: Enabled |
| LDK_NIC | 1 | D/K NICAM Stereo Standard Enable 0: Disabled 1: Enabled |
| I_NIC | 1 | I NICAM Stereo Standard Enable 0: Disabled 1: Enabled |
| BG_ZWT | 1 | B/G Zweiton (A2) Standard Enable 0: Disabled 1: Enabled |
| BG_NIC | 1 | B/G NICAM Standard Enable 0: Disabled 1: Enabled |
| MN_ZWT | 1 | M/N Zweiton (A2+) Standard Enable 0: Disabled 1: Enabled |

Note: Stereo standard covers all transmission modes (stereo or multi-language) of the NICAM or Zweiton (A2, A2* or A2+) system.

AUTOSTD_TIMERS**Detection Time Out Register**

Address: 8Dh

Type: R/W

| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|--------------|-------|-----------------|-------|-------|-------------------|-------|-------|
| FM_TIME[1:0] | | NICAM_TIME[2:0] | | | ZWEITON_TIME[2:0] | | |

| Bit Name | Reset | Function |
|-----------------|-------|---|
| FM_TIME[1:0] | 10 | FM/AM Detection Time-out 00 : 16 ms 10: 48 ms (Default) 01: 32 ms 11: 64 ms |
| NICAM_TIME[2:0] | 100 | NICAM Detection Time-out 000: 96 ms 100: 224 ms (Default) 001: 128 ms 101: 256 ms 010: 160 ms 110: 288 ms 011: 192 ms 111: 320 ms |

| Bit Name | Reset | Function |
|-------------------|-------|--|
| ZWEITON_TIME[2:0] | 100 | Zweiton Detection Time-out 000: forbids 100: 1280 ms (Default) 001: 512 ms 101: 1536 ms 010: 768 ms 110: 1792 ms 011: 1024 ms 111: 2040 ms |

Note: The time-out default value is optimum and does not normally need to be changed.

AUTOSTD_STATUS**Detection Standard Status Register**

Address: 8Eh

Type: R

| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|-----------|-----------|---------|------------|-----------------|-------|---------------|-------|
| STEREO_ID | STEREO_OK | MONO_OK | AUTOSTD_ON | STEREO_SID[1:0] | | MONO_SID[1:0] | |

| Bit Name | Reset | Function |
|-----------------|-------|--|
| STEREO_ID | 0 | Stereo Mode Detection flag activated when a stereo standard coming from the demodulator selected on Loudspeakers output. Stereo transmission modes are: - Zweiton Stereo Carrier AND Stereo Modulation (indifferently German or Korean standard) - NICAM stereo with backup (CBI = 1000) - NICAM stereo with no backup (CBI = 0000) |
| AUTOSTD_ON | 0 | Automatic Standard Recognition System Status 0: Automatic Standard Recognition System is OFF 1: Automatic Standard Recognition System is ON |
| STEREO_SID[1:0] | 00 | Identification of the detected TV sound standard. See Table 19 . |
| MONO_SID[1:0] | 00 | |
| STEREO_OK | 0 | STEREO STANDARD DETECTED |
| MONO_OK | 0 | MONO STANDARD DETECTED |

Table 19: TV Sound Standards

| System | Mono Sound (MHz) | MONO_SID [1:0] | LDK_SW | DK_DEV [1:0] | Stereo Sound (MHz) | STEREO_SID [1:0] |
|--------|------------------|----------------|--------|--------------|---------------------|------------------|
| M/N | 4.5 (FM 27k) | 00 | X | XX | 4.724 (Zweiton A2+) | 00 |
| B/G | 5.5 (FM 50k) | 01 | X | XX | 5.85 (NICAM 40%) | 00 |
| | | | X | XX | 5.742 (Zweiton A2) | 01 |
| I | 6.0 (FM 50k) | 10 | X | XX | 6.552 (NICAM 100%) | 00 |

Table 19: TV Sound Standards

| System | Mono Sound (MHz) | MONO_SID [1:0] | LDK_SW | DK_DEV [1:0] | Stereo Sound (MHz) | STEREO_SID [1:0] | |
|----------------|------------------|----------------|--------|--------------|--------------------|---------------------|----|
| L | 6.5 (AM) | 11 | 1 | XX | 5.85 (NICAM 40%) | 00 | |
| D/K | 6.5 (FM 50k) | | 0 | | 00 | 5.85 (NICAM 40%) | 00 |
| | 6.5 (FM 200k) | | | | 01 | | |
| | 6.5 (FM 350k) | | | | 10 | | |
| | 6.5 (FM 500k) | | | | 11 | | |
| D/K1/K2/ K3 | 6.5 (FM 50k) | | | 0 | XX | 5.85 (NICAM 40%) | 00 |
| | | | | 0 | XX | 6.258 (Zweiton A2*) | 01 |
| | | | | 0 | XX | 6.742 (Zweiton A2*) | 10 |
| | | | | 0 | XX | 5.742 (Zweiton A2*) | 11 |

Note: X means don't care.

12.13 Audio Preprocessing and Selection Registers

DC_REMOVAL_INPUT

DC Removal Register

Address: 90h

Type: R/W

| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|-------|-------|-------|-------|-------|----------|----------|----------|
| 0 | 0 | 0 | 0 | 0 | DC_SCART | DC_NICAM | DC_DEMOD |

| Bit Name | Reset | Function |
|-----------|-------|--|
| Bits[7:3] | 00000 | Reserved. |
| DC_SCART | 1 | 0: SCART input, DC removal inactive 1: SCART input, DC removal active |
| DC_NICAM | 1 | 0: NICAM input, DC removal inactive 1: NICAM input, DC removal active |
| DC_DEMOD | 1 | 0: FM input, DC removal inactive 1: FM input, DC removal active |

DC_REMOVAL_L

FM DC Offset Left Registerl

Address: 91h

Type: R

Bit 7 Bit 6 Bit 5 Bit 4 Bit 3 Bit 2 Bit 1 Bit 0

DC_REMOVAL_L[7:0]

| Bit Name | Reset | Function |
|-------------------|-----------|---|
| DC_REMOVAL_L[7:0] | 0000 0000 | Displays (in two's complement format) the FM (or AM) DC offset level after demodulation on channel 1 (and removed automatically). In FM mode, the DC offset value gives a direct value of the carrier frequency offset which is used to compensate the DCO with the CAROFFSET1 value in the event of an out-of-standard offset. The range and the resolution depend upon the FM bandwidth programmed defined in register BCOEFF1. See Table 20 . |

DC_REMOVAL_R

FM DC Offset Right Register

Address: 92h

Type: R

Bit 7 Bit 6 Bit 5 Bit 4 Bit 3 Bit 2 Bit 1 Bit 0

DC_REMOVAL_R[7:0]

| Bit Name | Reset | Function |
|-------------------|-----------|---|
| DC_REMOVAL_R[7:0] | 0000 0000 | Displays (in two's complement format) the FM (or AM) DC offset level after demodulation on channel 2 (and removed automatically). In FM mode, the DC offset value gives a direct value of the carrier frequency offset which is used to compensate the DCO with the CAROFFSET2 value in the event of an out-of-standard offset. The range and the resolution depend upon the FM bandwidth programmed defined in register BCOEFF2. See Table 20 . |

Table 20: DC_REMOVAL_L/R Range and Resolution

| FM mode | Range (kHz) | Resolution (kHz) |
|------------------------|-------------|------------------|
| Small | ± 96 | 0.750 |
| Standard & A2 Standard | ± 192 | 1.5 |
| Medium | ± 384 | 3 |
| Large | ± 768 | 6 |

PRESCALE_SELECT**AM/FM Prescaling Select Register**

Address: 93h

Type: R/W

| | | | | | | | |
|-------|-------|-------|-------|-------|-------|-------|--------------|
| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | AM_FM_SELECT |

| Bit Name | Reset | Function |
|--------------|---------|--|
| Bits[7:1] | 0000000 | Reserved. |
| AM_FM_SELECT | 0 | 0: FM prescale is applied to demodulator channels 1: AM prescale is applied to demodulator channels |

PRESCALE_AM**AM Prescaling Register**

Address: 94h

Type: R/W

| | | | | | | | |
|-------|-------------|-------|-------|-------|-------|-------|-------|
| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
| 0 | PRESCALE_AM | | | | | | |

| Bit Name | Reset | Function | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|------------------|---------------|--|---------------|---------------|--|---------------|---------|-----|---------|-----|---------|-------|---------|-------|---------|-----|---------|-----|---------|-------|---------|-------|---------|-----|---------|-----|--|------|--|--|
| Bit 7 | 0 | Reserved. | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| PRESCALE_AM[6:0] | 0000000 | -12 to + 24 dB AM prescaling to normalize the AM demodulated signal level before audio processing. Auto level control can be implemented by I2C software using the Peak Level Detector. (Default value = 0 dB) | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | <table border="0"> <thead> <tr> <th></th> <th><u>G (dB)</u></th> <th></th> <th><u>G (dB)</u></th> </tr> </thead> <tbody> <tr> <td>0110000</td> <td>+24</td> <td>1101100</td> <td>-10</td> </tr> <tr> <td>0101111</td> <td>+23.5</td> <td>1101011</td> <td>-10.5</td> </tr> <tr> <td>0101110</td> <td>+23</td> <td>1101010</td> <td>-11</td> </tr> <tr> <td>0101101</td> <td>+22.5</td> <td>1101001</td> <td>-11.5</td> </tr> <tr> <td>0101100</td> <td>+22</td> <td>1101000</td> <td>-12</td> </tr> <tr> <td></td> <td>etc.</td> <td></td> <td></td> </tr> </tbody> </table> | | <u>G (dB)</u> | | <u>G (dB)</u> | 0110000 | +24 | 1101100 | -10 | 0101111 | +23.5 | 1101011 | -10.5 | 0101110 | +23 | 1101010 | -11 | 0101101 | +22.5 | 1101001 | -11.5 | 0101100 | +22 | 1101000 | -12 | | etc. | | |
| | <u>G (dB)</u> | | <u>G (dB)</u> | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 0110000 | +24 | 1101100 | -10 | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 0101111 | +23.5 | 1101011 | -10.5 | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 0101110 | +23 | 1101010 | -11 | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 0101101 | +22.5 | 1101001 | -11.5 | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 0101100 | +22 | 1101000 | -12 | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | etc. | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

PRESCALE_FM**FM Prescaling Register**

Address: 95h

Type: R/W

| | | | | | | | |
|-------|-------------|-------|-------|-------|-------|-------|-------|
| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
| 0 | PRESCALE_FM | | | | | | |

| Bit Name | Reset | Function | | | | | | | | | | | | | | |
|------------------|---------------|--|---------------|---------------|-------------|-------------|---------------|---------------|-------------|-------------|---------------|---------------|-------------|-------------|------|--|
| Bit 7 | 0 | Reserved. | | | | | | | | | | | | | | |
| PRESCALE_FM[6:0] | 0001100 | -12 to + 24 dB FM prescaling to normalize the FM demodulated signal level before audio processing. Auto level control can be implemented by I2C software using the Peak Level Detector. (Default value = +6 dB) | | | | | | | | | | | | | | |
| | | <table style="width: 100%; border: none;"> <thead> <tr> <th style="text-align: left;"><u>G (dB)</u></th> <th style="text-align: left;"><u>G (dB)</u></th> </tr> </thead> <tbody> <tr> <td>0110000 +24</td> <td>1101100 -10</td> </tr> <tr> <td>0101111 +23.5</td> <td>1101011 -10.5</td> </tr> <tr> <td>0101110 +23</td> <td>1101010 -11</td> </tr> <tr> <td>0101101 +22.5</td> <td>1101001 -11.5</td> </tr> <tr> <td>0101100 +22</td> <td>1101000 -12</td> </tr> <tr> <td>etc.</td> <td></td> </tr> </tbody> </table> | <u>G (dB)</u> | <u>G (dB)</u> | 0110000 +24 | 1101100 -10 | 0101111 +23.5 | 1101011 -10.5 | 0101110 +23 | 1101010 -11 | 0101101 +22.5 | 1101001 -11.5 | 0101100 +22 | 1101000 -12 | etc. | |
| <u>G (dB)</u> | <u>G (dB)</u> | | | | | | | | | | | | | | | |
| 0110000 +24 | 1101100 -10 | | | | | | | | | | | | | | | |
| 0101111 +23.5 | 1101011 -10.5 | | | | | | | | | | | | | | | |
| 0101110 +23 | 1101010 -11 | | | | | | | | | | | | | | | |
| 0101101 +22.5 | 1101001 -11.5 | | | | | | | | | | | | | | | |
| 0101100 +22 | 1101000 -12 | | | | | | | | | | | | | | | |
| etc. | | | | | | | | | | | | | | | | |

www.DataSheet4U.com

PRESCALE_NICAM**NICAM Prescaling Register**

Address: 96h

Type: R/W

| | | | | | | | |
|-------|----------------|-------|-------|-------|-------|-------|-------|
| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
| 0 | PRESCALE_NICAM | | | | | | |

| Bit Name | Reset | Function | | | | | | | | | | | | | | |
|---------------------|---------------|---|---------------|---------------|-------------|------------|---------------|--------------|-------------|------------|---------------|--------------|-------------|------------|------|--|
| Bit 7 | 0 | Reserved. | | | | | | | | | | | | | | |
| PRESCALE_NICAM[6:0] | 011010 | -6 to + 24 dB NICAM prescaling to normalize the NICAM demodulated signal level before audio processing. Auto level control can be implemented by I2C software using the Peak Level Detector. (Default value = +13 dB) | | | | | | | | | | | | | | |
| | | <table style="width: 100%; border: none;"> <thead> <tr> <th style="text-align: left;"><u>G (dB)</u></th> <th style="text-align: left;"><u>G (dB)</u></th> </tr> </thead> <tbody> <tr> <td>0110000 +24</td> <td>1111000 -4</td> </tr> <tr> <td>0101111 +23.5</td> <td>1110111 -4.5</td> </tr> <tr> <td>0101110 +23</td> <td>1110110 -5</td> </tr> <tr> <td>0101101 +22.5</td> <td>1110101 -5.5</td> </tr> <tr> <td>0101100 +22</td> <td>1110100 -6</td> </tr> <tr> <td>etc.</td> <td></td> </tr> </tbody> </table> | <u>G (dB)</u> | <u>G (dB)</u> | 0110000 +24 | 1111000 -4 | 0101111 +23.5 | 1110111 -4.5 | 0101110 +23 | 1110110 -5 | 0101101 +22.5 | 1110101 -5.5 | 0101100 +22 | 1110100 -6 | etc. | |
| <u>G (dB)</u> | <u>G (dB)</u> | | | | | | | | | | | | | | | |
| 0110000 +24 | 1111000 -4 | | | | | | | | | | | | | | | |
| 0101111 +23.5 | 1110111 -4.5 | | | | | | | | | | | | | | | |
| 0101110 +23 | 1110110 -5 | | | | | | | | | | | | | | | |
| 0101101 +22.5 | 1110101 -5.5 | | | | | | | | | | | | | | | |
| 0101100 +22 | 1110100 -6 | | | | | | | | | | | | | | | |
| etc. | | | | | | | | | | | | | | | | |

PRESCALE_SCART**SCART Prescaling Register**

Address: 97h

Type: R/W

| | | | | | | | |
|-------|-------|----------------|-------|-------|-------|-------|-------|
| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
| 0 | 0 | PRESCALE_SCART | | | | | |

| Bit Name | Reset | Function |
|-----------|-------|-----------|
| Bit [7:6] | 00 | Reserved. |

| Bit Name | Reset | Function | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|---------------------|---------------|---|---------------|---------------|--|---------------|--------|-----|--------|-----|--------|-------|--------|-------|--------|-----|--------|-----|--------|-------|--------|-------|--------|-----|--------|-----|--|------|--|--|
| PRESCALE_SCART[5:0] | 0000000 | -12 to + 12 dB SCART prescaling to normalize the SCART signal level before audio processing. Auto level control can be implemented by I2C software using the Peak Level Detector. (Default value = 0 dB) | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | <table> <thead> <tr> <th></th> <th><u>G (dB)</u></th> <th></th> <th><u>G (dB)</u></th> </tr> </thead> <tbody> <tr> <td>011000</td> <td>+12</td> <td>101100</td> <td>-10</td> </tr> <tr> <td>010111</td> <td>+11.5</td> <td>101011</td> <td>-10.5</td> </tr> <tr> <td>010110</td> <td>+11</td> <td>101010</td> <td>-11</td> </tr> <tr> <td>010101</td> <td>+10.5</td> <td>101001</td> <td>-11.5</td> </tr> <tr> <td>010100</td> <td>+10</td> <td>101000</td> <td>-12</td> </tr> <tr> <td></td> <td>etc.</td> <td></td> <td></td> </tr> </tbody> </table> | | <u>G (dB)</u> | | <u>G (dB)</u> | 011000 | +12 | 101100 | -10 | 010111 | +11.5 | 101011 | -10.5 | 010110 | +11 | 101010 | -11 | 010101 | +10.5 | 101001 | -11.5 | 010100 | +10 | 101000 | -12 | | etc. | | |
| | <u>G (dB)</u> | | <u>G (dB)</u> | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 011000 | +12 | 101100 | -10 | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 010111 | +11.5 | 101011 | -10.5 | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 010110 | +11 | 101010 | -11 | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 010101 | +10.5 | 101001 | -11.5 | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 010100 | +10 | 101000 | -12 | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | etc. | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

PRESCALE_I2S_0**I2S_0 Prescaling Register**

www.DataSheet4U.com
Address: 98h

Type: R/W

| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|-------|-------|---------------------|-------|-------|-------|-------|-------|
| 0 | 0 | PRESCALE_I2S_0[5:0] | | | | | |

| Bit Name | Reset | Function | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|---------------------|---------------|---|---------------|---------------|--|---------------|--------|-----|--------|-----|--------|-------|--------|-------|--------|-----|--------|-----|--------|-------|--------|-------|--------|-----|--------|-----|--|------|--|--|
| Bits [7:6] | 00 | Reserved. | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| PRESCALE_I2S_0[5:0] | 000000 | -12 to + 12 dB I2S_0 prescaling to normalize the I2S_0 signal level before audio processing. Auto level control can be implemented by I2C software using the Peak Level Detector. (Default value = 0 dB) | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | <table> <thead> <tr> <th></th> <th><u>G (dB)</u></th> <th></th> <th><u>G (dB)</u></th> </tr> </thead> <tbody> <tr> <td>011000</td> <td>+12</td> <td>101100</td> <td>-10</td> </tr> <tr> <td>010111</td> <td>+11.5</td> <td>101011</td> <td>-10.5</td> </tr> <tr> <td>010110</td> <td>+11</td> <td>101010</td> <td>-11</td> </tr> <tr> <td>010101</td> <td>+10.5</td> <td>101001</td> <td>-11.5</td> </tr> <tr> <td>010100</td> <td>+10</td> <td>101000</td> <td>-12</td> </tr> <tr> <td></td> <td>etc.</td> <td></td> <td></td> </tr> </tbody> </table> | | <u>G (dB)</u> | | <u>G (dB)</u> | 011000 | +12 | 101100 | -10 | 010111 | +11.5 | 101011 | -10.5 | 010110 | +11 | 101010 | -11 | 010101 | +10.5 | 101001 | -11.5 | 010100 | +10 | 101000 | -12 | | etc. | | |
| | <u>G (dB)</u> | | <u>G (dB)</u> | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 011000 | +12 | 101100 | -10 | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 010111 | +11.5 | 101011 | -10.5 | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 010110 | +11 | 101010 | -11 | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 010101 | +10.5 | 101001 | -11.5 | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 010100 | +10 | 101000 | -12 | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | etc. | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

PRESCALE_I2S_1**I2S_1 Prescaling Register**

Address: 99h

Type: R/W

| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|-------|-------|---------------------|-------|-------|-------|-------|-------|
| 0 | 0 | PRESCALE_I2S_1[5:0] | | | | | |

| Bit Name | Reset | Function |
|------------|-------|-----------|
| Bits [7:6] | 00 | Reserved. |

| Bit Name | Reset | Function | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|---------------------|---------------|--|---------------|---------------|--|---------------|--------|-----|--------|-----|--------|-------|--------|-------|--------|-----|--------|-----|--------|-------|--------|-------|--------|-----|--------|-----|--|------|--|--|
| PRESCALE_I2S_1[5:0] | 000000 | -12 to + 12 dB I2S_1 prescaling to normalize the I2S_1 signal level before audio processing. Auto level control can be implemented by I2C software using the Peak Level Detector. (Default value = 0 dB) | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | <table border="0"> <thead> <tr> <th></th> <th><u>G (dB)</u></th> <th></th> <th><u>G (dB)</u></th> </tr> </thead> <tbody> <tr> <td>011000</td> <td>+12</td> <td>101100</td> <td>-10</td> </tr> <tr> <td>010111</td> <td>+11.5</td> <td>101011</td> <td>-10.5</td> </tr> <tr> <td>010110</td> <td>+11</td> <td>101010</td> <td>-11</td> </tr> <tr> <td>010101</td> <td>+10.5</td> <td>101001</td> <td>-11.5</td> </tr> <tr> <td>010100</td> <td>+10</td> <td>101000</td> <td>-12</td> </tr> <tr> <td></td> <td>etc.</td> <td></td> <td></td> </tr> </tbody> </table> | | <u>G (dB)</u> | | <u>G (dB)</u> | 011000 | +12 | 101100 | -10 | 010111 | +11.5 | 101011 | -10.5 | 010110 | +11 | 101010 | -11 | 010101 | +10.5 | 101001 | -11.5 | 010100 | +10 | 101000 | -12 | | etc. | | |
| | <u>G (dB)</u> | | <u>G (dB)</u> | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 011000 | +12 | 101100 | -10 | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 010111 | +11.5 | 101011 | -10.5 | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 010110 | +11 | 101010 | -11 | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 010101 | +10.5 | 101001 | -11.5 | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 010100 | +10 | 101000 | -12 | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | etc. | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

PRESCALE_I2S_2

I2S_2 Prescaling Register

www.DataSheet4U.com

Address: 9Ah

Type: R/W

| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|-------|-------|---------------------|-------|-------|-------|-------|-------|
| 0 | 0 | PRESCALE_I2S_2[5:0] | | | | | |

| Bit Name | Reset | Function | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|---------------------|---------------|--|---------------|---------------|--|---------------|--------|-----|--------|-----|--------|-------|--------|-------|--------|-----|--------|-----|--------|-------|--------|-------|--------|-----|--------|-----|--|------|--|--|
| Bits [7:6] | 00 | Reserved. | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| PRESCALE_I2S_2[5:0] | 000000 | -12 to + 12 dB I2S_2 prescaling to normalize the I2S_2 signal level before audio processing. Auto level control can be implemented by I2C software using the Peak Level Detector. (Default value = 0 dB) | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | <table border="0"> <thead> <tr> <th></th> <th><u>G (dB)</u></th> <th></th> <th><u>G (dB)</u></th> </tr> </thead> <tbody> <tr> <td>011000</td> <td>+12</td> <td>101100</td> <td>-10</td> </tr> <tr> <td>010111</td> <td>+11.5</td> <td>101011</td> <td>-10.5</td> </tr> <tr> <td>010110</td> <td>+11</td> <td>101010</td> <td>-11</td> </tr> <tr> <td>010101</td> <td>+10.5</td> <td>101001</td> <td>-11.5</td> </tr> <tr> <td>010100</td> <td>+10</td> <td>101000</td> <td>-12</td> </tr> <tr> <td></td> <td>etc.</td> <td></td> <td></td> </tr> </tbody> </table> | | <u>G (dB)</u> | | <u>G (dB)</u> | 011000 | +12 | 101100 | -10 | 010111 | +11.5 | 101011 | -10.5 | 010110 | +11 | 101010 | -11 | 010101 | +10.5 | 101001 | -11.5 | 010100 | +10 | 101000 | -12 | | etc. | | |
| | <u>G (dB)</u> | | <u>G (dB)</u> | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 011000 | +12 | 101100 | -10 | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 010111 | +11.5 | 101011 | -10.5 | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 010110 | +11 | 101010 | -11 | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 010101 | +10.5 | 101001 | -11.5 | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 010100 | +10 | 101000 | -12 | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | etc. | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

DEEMPHASIS_DEMATRIX

Deemphasis-Dematrix Register

Address: 9Bh

Type: R/W

| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|-------|-------|----------------|----------------------|-------------|-------|------------------|--------------|
| 0 | 0 | NICAM_DEMATRIX | NICAM_DEEMPH_BY_PASS | FM_DEMATRIX | | FM_DEEMPH_BYPASS | FM_DEEMPH_SW |

| Bit Name | Reset | Function |
|------------|-------|-----------|
| Bits [7:6] | 00 | Reserved. |

| Bit Name | Reset | Function |
|---------------------|-------|--|
| NICAM_DEMATRIX | 0 | Dematrixing for NICAM demodulator input: 00: L=ch0, R=ch1 01: L=ch1, R=ch0 |
| NICAM_DEEMPH_BYPASS | 0 | 0: NICAM deemphasis is not bypassed. 1: NICAM deemphasis is bypassed. |
| FM_DEMATRIX[3:2] | 00 | Dematrixing for FM demodulator input: 00: L=ch0, R=ch1 01: L=ch0+ch1, R=ch0-ch1 10: L=2ch0-ch1, R=ch1 11: L=(ch0+ch1)/2, R=(ch0-ch1)/2 |
| FM_DEEMPH_BYPASS | 0 | 0: FM deemphasis is not bypassed. 1: FM deemphasis is bypassed. |
| FM_DEEMPH_SW | 0 | 0: 50 μ s FM deemphasis. 1: 75 μ s FM deemphasis. |

PEAK_DET_INPUT**Peak Detector Input source Register**

Address: 9Dh

Type: R

| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---------------|-------|----------------|-------|-------|---------------------|-------|-------|
| PEAK_LOCATION | 0 | PEAK_L_R_RANGE | | | PEAK_DET_INPUT[1:0] | | |

| Bit Name | Reset | Function |
|---------------------|-------|---|
| PEAK_LOCATION | 0 | Peak detector location : 0: Peak detector placed between FM/NICAM Dematrix and Audio Matrix or between I ² S Prescale and DownMix 1: Peak detector placed before DC removal (For input saturation detection) |
| Bit 6 | 0 | Reserved. |
| PEAK_L_R_RANGE | 0000 | Peak L-R range. 0000 : 0 dBFS to -42 dBFS 0001 : -6 dBFS to -48 dBFS 0010 : -12 dBFS to -54 dBFS 0011 : -18 dBFS to -60 dBFS ... |
| PEAK_DET_INPUT[1:0] | 00 | Peak Level Detector Source Selection 00: AM/FM or I ² S 0 10: SCART or I ² S 2 01: NICAM or I ² S 1 |

PEAK_DET_L**Peak Level Detector Status Register (L channel)**

Address: 9Eh

Type: R

| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|------------|-------------|-------|-------|-------|-------|-------|-------|
| OVERLOAD_L | PEAK_L[6:0] | | | | | | |

| Bit Name | Reset | Function |
|---------------|----------|---|
| OVERLOAD_L[7] | 0 | Memorise overload on the peak detection. This field can be reset. |
| PEAK_L[6:0] | 00000000 | Displays the Absolute Peak Level of the audio source selected. The measured value is updated continuously every 64 ms. The range varies linearly from the full scale (0 dB) down to 1/256 of the full scale (-48 dB). In AM/FM Mono mode, only the PEAK_L[7:0] value must be taken into account. In FM Mono mode, the audio peak level range depends upon the programmed FM bandwidth. The unique difference is that the measurement is done after Sound pre-processing (DC offset removal, Prescaling, De-emphasis and Dematrixing). In FM Stereo mode, the maximum value may be used to check if the incoming signal level is correctly adjusted by the prescaling factor or if there are no FM overmodulation problems (clipping). Programmable values are listed in Table 20 . |

www.DataSheet4U.com

PEAK_DET_R**Peak Level Detector Status Register (R channel)**

Address: 9Fh

Type: R

| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|------------|-------------|-------|-------|-------|-------|-------|-------|
| OVERLOAD_R | PEAK_R[6:0] | | | | | | |

| Bit Name | Reset | Function |
|---------------|----------|--|
| OVERLOAD_R[7] | 0 | Memorise overload on the peak detection. This field can be reset. |
| PEAK_R[7:0] | 00000000 | Displays the Absolute Peak Level of the audio source selected. The measured value is updated continuously every 64 ms. The range varies linearly from the full scale (0 dB) down to 1/256 of the full scale (-48 dB). For more information, refer to register PEAK_DET_L . |

PEAK_DET_L_R**Peak Level Detector Status Register (L - R)**

Address: A0h

Type: R

| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|--------------|---------------|-------|-------|-------|-------|-------|-------|
| OVERLOAD_L_R | PEAK_L_R[6:0] | | | | | | |

| Bit Name | Reset | Function |
|-----------------|----------|--|
| OVERLOAD_L_R[7] | 0 | Memorise overload on the peak detection. This field can be reset. |
| PEAK_L_R[7:0] | 00000000 | Displays the Difference between L and R (L - R) channels for the audio source selected. For more information, refer to register PEAK_DET_L . |

12.14 Matrixing

AUDIO_MATRIX_INPUT

Audio Matrix Input Selection Register

Address: A2h

Type: R/W

| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|-------|-------|-------|-------|-------|--------------------|-----------------|-----------------|
| 0 | 0 | 0 | 0 | 0 | SCART_INPUT_SOURCE | HP_INPUT_SOURCE | LS_INPUT_SOURCE |

| Bit Name | Reset | Function |
|--------------------|-------|---|
| Bits [7:3] | 00000 | Reserved. |
| SCART_INPUT_SOURCE | 0 | Select input source for SCART output: 0: Demod 1: SCART input |
| HP_INPUT_SOURCE | 0 | Select input source for HP output: 0: Demod 1: SCART input |
| LS_INPUT_SOURCE | 0 | Select input source for LS output: 0: Demod 1: SCART input |

AUDIO_MATRIX_CONFIG

Register Description

Address: A3h

Type: R/W

| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|-------|-------|-------|--------------|-------------------|-------|-------|-------|
| 0 | 0 | 0 | SCART_MATRIX | DEMOM_MATRIX[3:0] | | | |

| Bit Name | Reset | Function |
|--------------------|-------|--|
| Bits [7:5] | 000 | Reserved. |
| SCART_MATRIX | 0 | Indicates the SCART input signal matrixing (see Table 22) |
| DEMOM_MATRIX [3:0] | 0000 | Indicates the demod input signal matrixing (see Table 21) |

Table 21: Demod Matrix

| Input Mode | Language -> | Stereo | | Mono A | | Mono B | | Mono C | | Backup mode |
|------------------------|-------------|----------|--------|-------------------|---|-------------------|---|-------------------|---|------------------------|
| | | demod_mx | L | R | L | R | L | R | L | |
| Mono AM/FM with backup | 0000 | FM | | FM | | FM | | FM | | |
| Mono AM/FM no backup | 0001 | - | | - | | - | | FM | | |
| Zwt St | 0100 | FM_L | FM_R | (FM_L + FM_R)/2 | | (FM_L + FM_R)/2 | | (FM_L + FM_R)/2 | | |
| Zwt Dual | 0101 | FM_M1 | FM_M2 | FM_M1 | | FM_M2 | | (FM_M1 + FM_M2)/2 | | |
| NICAM Mn, backup | 1000 | NIC_M1 | | NIC_M1 | | NIC_M1 | | FM | | Mono AM/FM with backup |
| NICAM Dual backup | 1001 | NIC_M1 | NIC_M2 | NIC_M1 | | NIC_M2 | | FM | | Mono AM/FM with backup |
| NICAM St, backup | 1010 | NIC_L | NIC_R | (NIC_L + NIC_R)/2 | | (NIC_L + NIC_R)/2 | | FM | | Mono AM/FM with backup |
| NICAM Mn, no backup | 1100 | NIC_M1 | | NIC_M1 | | NIC_M1 | | FM | | Mono AM/FM no backup |
| NICAM Dual, no backup | 1101 | NIC_M1 | NIC_M2 | NIC_M1 | | NIC_M2 | | FM | | Mono AM/FM no backup |
| NICAM St, no backup | 1110 | NIC_L | NIC_R | (NIC_L + NIC_R)/2 | | (NIC_L + NIC_R)/2 | | FM | | Mono AM/FM no backup |

Note: Switching between Stereo and Forced Mono modes can be done using (FM_L + FM_R)/2 or (NIC_L + NIC_R)/2 configurations.

Table 22: SCART Matrix

| SCART_MX | Stereo | | Mono A | | Mono B | | Mono C | |
|----------|---------|---------|---------|-------|---------|-------|-----------------------|-------|
| | Left | Right | Left | Right | Left | Right | Left | Right |
| 0 | SCART_L | SCART_R | SCART_L | | SCART_R | | (SCART_L + SCART_R)/2 | |
| 1 | SCART_R | SCART_L | SCART_R | | SCART_L | | (SCART_L + SCART_R)/2 | |

AUDIO_MATRIX_LANGUAGE Register Description

Address: A4h

Type: R/W

| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|-------------|----------|---------------------|-------|------------------|-------|------------------|-------|
| MUTE_STEREO | MUTE_ALL | SCART_LANGUAGE[1:0] | | HP_LANGUAGE[1:0] | | LS_LANGUAGE[1:0] | |

| Bit Name | Reset | Function |
|---------------------|-------|---|
| MUTE_STEREO | 0 | Mute outputs with stereo signal input |
| MUTE_ALL | 0 | Mute all outputs |
| SCART_LANGUAGE[1:0] | 00 | Select language for SCART output |
| HP_LANGUAGE[1:0] | 00 | Select language for HPoutput |
| LS_LANGUAGE[1:0] | 00 | Select language for LS output 00: stereo 01: mono A 10: mono B 11: mono C |

www.DataSheet4U.com

DOWNMIX_IN_MODE**Register Description**

Address: A6h

Type: R/W

| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|-------|-------|-------|-------|--------|------------------|-------|-------|
| 0 | 0 | 0 | 0 | LFE_IN | MIX_IN_MODE[2:0] | | |

| Bit Name | Reset | Function |
|------------------|-------|--|
| Bits[7:4] | 0000 | Reserved |
| LFE_IN | 0 | 0: LFE signal is not inputed throught Downmix Block 1: LFE signal is inputed throught Downmix Block |
| MIX_IN_MODE[2:0] | 010 | see Table 23 |

Table 23: DownMix IN modes

| Parameter Coding (Decimal Format) | Parameter Field Label | Function |
|-----------------------------------|-----------------------|--------------------------|
| 0 | MODE11 | Mode not used in STV82x7 |
| 1 | MODE10 | 1/0 (C) |
| 2 | MODE20 | 2/0 (L,R) |
| 3 | MODE30 | 3/0 (L,R,C) |
| 4 | MODE21 | 2/1 (L,R,S) |
| 5 | MODE31 | 3/1 (L,R,C,S) |
| 6 | MODE22 | 2/2 (L,R,Ls,Rs) |
| 7 | MODE32 | 3/2 (L,R,C,Ls,Rs) |

DOWNMIX_OUT_MODE

Register Description

Address:A7h

Type: R/W

| | | | | | | | |
|-------|--------------|-------|-----------------|-------|------------------|-------|-------|
| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
| 0 | HP_MODE[1:0] | | SCART_MODE[1:0] | | LS_OUT_MODE[2:0] | | |

| Bit Name | Reset | Function |
|-------------------|-------|------------------------------|
| Bit 7 | 0 | Reserved. |
| HP_MODE[1:0] | 10 | see Table 24 |
| SCART_MODE[1:0] | 01 | see Table 24 |
| LS_OUT_MODE [2:0] | 010 | see Table 25 |

Table 24: DownMix SCART/HP modes

| Parameter Coding (Decimal Format) | Parameter Field Label | Function |
|-----------------------------------|-----------------------|---|
| 0 | MIX_VCR_OFF | Switch off the VCR table setup |
| 1 | MIX_VCR_PROLOGIC | VCR table setup for Tape outputs (for later decoding by a Dolby Prologic decoder - Lt,Rt) |
| 2 | MIX_VCR_STEREO | VCR table setup for Stereo and headphone listening (Lo,Ro) |
| 3 | MIX_COSTOM | reserved |

Table 25: DownMix LS OUT modes

| Parameter Coding (Decimal Format) | Parameter Field Label | Function |
|-----------------------------------|-----------------------|----------------------------|
| 0 | MODE20t | 2/0 Dolby Surround (Lt,Rt) |
| 1 | MODE10 | 1/0 (C) |
| 2 | MODE20 | 2/0 (L,R) |
| 3 | MODE30 | 3/0 (L,R,C) |
| 4 | MODE21 | 2/1 (L,R,S) |
| 5 | MODE31 | 3/1 (L,R,C,S) |
| 6 | MODE22 | 2/2 (L,R,LS,RS) |
| 7 | MODE32 | 3/2 (L,R,C,LS,RS) |

DOWNMIX_DUAL_MODE Register Description

Address: A8h

Type: R/W

| | | | | | | | |
|-------|---------|---------------------|-------|------------------------|-------|---------------------|-------|
| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
| 0 | DUAL_ON | LS_DUAL_SELECT[1:0] | | SCART_DUAL_SELECT[1:0] | | HP_DUAL_SELECT[1:0] | |

| Bit Name | Reset | Function |
|------------------------|-------|--|
| Bit 7 | 0 | Reserved. |
| DUAL_ON | 0 | 0: dual mode disable 1: dual mode enable |
| LS_DUAL_SELECT[1:0] | 00 | Dual Mono Mode on LS output 00: LS dual stereo 01: LS dual left mono 10: LS dual right mono 11: LS dual mixed |
| SCART_DUAL_SELECT[1:0] | 00 | Dual Mono Mode on SCART output 00: SCART dual stereo 01: SCART dual left mono 10: SCART dual right mono 11: SCART dual mixed |
| HP_DUAL_SELECT[1:0] | 00 | Dual Mono Mode on HP output 00: HP dual stereo 01: HP dual left mono 10: HP dual right mono 11: HP dual mixed |

DOWNMIX_CONFIG Register Description

Address: A9h

Type: R/W

| | | | | | | | |
|-------|-------|------------------|-------|--------------------|-------|----------|-----------|
| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
| 0 | 0 | SRND_FACTOR[1:0] | | CENTER_FACTOR[1:0] | | LR_UPMIX | NORMALIZE |

| Bit Name | Reset | Function |
|---------------------|-------|--|
| Bits[7:6] | 00 | |
| SRND_FACTOR [1:0] | 00 | 00: -3dB 01: -4.5dB 10: -6dB 11: -6dB |
| CENTER_FACTOR [1:0] | 00 | 00: -3dB 01: -4.5dB 10: -6dB 11: -4.5dB |

| Bit Name | Reset | Function |
|-----------|-------|---|
| LR_UPMIX | 0 | 0: disable upmixing 1: enable upmixing (DTS specified) |
| NORMALIZE | 1 | 0: disable normalization 1: enable normalization |

12.15 Audio Processing

PRO_LOGIC2_CONTROL Register Description

Address: AAh

Type: R/W

| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---------|-------------------------|-------|-------|-------|----------------|-------|------------|
| PL2_LFE | PL2_OUTPUT_DOWNMIX[2:0] | | | | PL2_MODES[2:0] | | PL2_ACTIVE |

| Bit Name | Reset | Function |
|-------------------------|-------|---|
| PL2_LFE | 0 | 0: Reset the LFE channel 1: Bypass the LFE channel |
| PL2_OUTPUT_DOWNMIX[2:0] | 000 | 000: not applicable 001: not applicable 010: not applicable 011: 3/0 output mode (L,R,C) 100: 2/1 output mode (L,R,Ls - phantom) 101: 3/1 output mode (L,R,C,Ls) 110: 2/2 output mode (L,R,Ls,Rs - phantom) 111: 3/2 output mode (L,R,C,Ls,Rs) |
| PL2_MODES[2:0] | 000 | 000: Pro Logic 1 Emulation (forced if DPL version) 001: Virtual (DPL2 version only) 010: Music (DPL2 version only) 011: Movie (standard) (DPL2 version only) 100: Matrix (DPL2 version only) 101: Custom (DPL2 version only) 110: not applicable (DPL2 version only) 111: not applicable (DPL2 version only) |
| PL2_ACTIVE | 0 | 0: Dolby Prologic 2 is not active 1: Dolby Prologic 2 is active |

Table 26: Prologic II Decode Mode Configuration

| PL2 Mode | Decode Mode | Dimension | Center Width | Auto-Balance | Panorama | Surround Coherence | SUR Filtering |
|----------|---------------------|-----------|--------------|--------------|----------|--------------------|---------------|
| 0 | Pro Logic Emulation | 3 | 0 | 1 | 0 | 0 | 2 |
| 1 | Virtual | 3 | 0 | 1 | 0 | 1 | 0 |
| 2 | Music | x | x | 0 | x | 1 | 1 |

Table 26: Prologic II Decode Mode Configuration (Continued)

| PL2 Mode | Decode Mode | Dimension | Center Width | Auto-Balance | Panorama | Surround Coherence | SUR Filtering |
|----------|----------------|-----------|--------------|--------------|----------|--------------------|---------------|
| 3 | Movie/Standard | 3 | 0 | 1 | 0 | 0 | 0 |
| 4 | Matrix | 3 | 0 | 0 | 0 | 1 | 1 |
| 5 | Custom | x | x | x | x | x | x |

Note: (x = user defined parameter)

www.DataSheet4U.com

PCM_SRND_DELAY**Register Description**

Address: ABh

Type: R/W

| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|-------|-------|-------|-----------------|-------|-------|-------|-------|
| 0 | 0 | 0 | SNRD_DELAY[4:0] | | | | |

| Bit Name | Reset | Function |
|-----------------|-------|--|
| Bits[7:5] | 000 | Reserved. |
| SNRD_DELAY[4:0] | 00000 | Surround Channel Delay range: 0 to 30 (in ms) |

PCM_CENTER_DELAY**Register Description**

Address: ACh

Type: R/W

| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|-------|-------|-------|-------|-------------------|-------|-------|-------|
| 0 | 0 | 0 | 0 | CENTER_DELAY[3:0] | | | |

| Bit Name | Reset | Function |
|-------------------|-------|--|
| Bits[7:4] | 0000 | Reserved. |
| CENTER_DELAY[3:0] | 0000 | Center Channel Delay range: 0 to 10 (in ms) |

PRO_LOGIC2_CONFIG

Register Description

Address: ADh

Type: R/W

| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---------|-------|-------|----------------------|-------|-----------------|--------------|-----------------|
| PL2_LFE | 0 | 0 | PL2_SRND_FILTER[1:0] | | PL2_RS_POLARITY | PL2_PANORAMA | PL2_AUTOBALANCE |

| Bit Name | Reset | Function |
|---------------------|-------|---|
| Bits[7:6] | 00 | Reserved. |
| PL2_SRND_FILTR[1:0] | 00 | 00: 0: Off 01: 1: Shelf Filter (for music and matrix modes) 10: 2: 7kHz LP 11: 3: not applicable |
| PL2_RS_POLARITY | 0 | 0: Rs polarity normal 1: Rs polarity inverted |
| PL2_PANORAMA | 0 | 0: Panorama Off 1: Panorama On |
| PL2_AUTOBALANCE | 0 | 0: Autobalance Off 1: Autobalance On |

See [Table 26: Prologic II Decode Mode Configuration](#) for programming of these bits depending on the decode mode.

PRO_LOGIC2_DIMENSION

Register Description

Address: AEh

Type: R/W

| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|-------|-------------|-------|-------|-------|---------------|-------|-------|
| 0 | PL2_C_WIDTH | | | 0 | PL2_DIMENSION | | |

| Bit Name | Reset | Function |
|------------------|-------|---|
| Bit 7 | 0 | Reserved. |
| PL2_C_WIDTH[2:0] | 000 | 000: 0, no spread = OFF 001: 20 010: 28 011: 36 100: 54 101: 62 110: 69 111: 90, phantom |
| Bit 3 | 0 | Reserved. |

| Bit Name | Reset | Function |
|--------------------|-------|--|
| PL2_DIMENSION[2:0] | 000 | 000: -3, most surround 001: -2 010: -1 011: 0, neutral = OFF 100: 1 101: 2 110:3, most center 111: not applicable |

See [Table 26: Prologic II Decode Mode Configuration](#) for programming of these bits depending on the decode mode.

PRO_LOGIC2_LEVEL Register Description

Address: AFh

Type: R/W

| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|-----------|-------|-------|-------|-------|-------|-------|-------|
| PL2_LEVEL | | | | | | | |

| Bit Name | Reset | Function |
|----------------|----------|--|
| PL2_LEVEL[7:0] | 00000000 | Input Gain attenuation: 0000 0000: 0dB 0000 0001: -0.5dB ... 1111 1111: -127.5dB |

NOISE_GENERATOR Register Description

Address: B0h

Type: R/W

| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|-----------------|--------------|-------------|-----------|--------------|-------------|------------|----------|
| 10_DB_ATTENUATE | SRIGHT_NOISE | SLEFT_NOISE | SUB_NOISE | CENTER_NOISE | RIGHT_NOISE | LEFT_NOISE | NOISE_ON |

| Bit Name | Reset | Function |
|-----------------|-------|--|
| 10_DB_ATTENUATE | 0 | 0: noise is outputted with full range 1: noise is outputted with a 10dB attenuation |
| SRIGHT_NOISE | 0 | 1: Generates noise on LS right surround output |
| SLEFT_NOISE | 0 | 1: Generates noise on LS left surround output |
| SUB_NOISE | 0 | 1: Generates noise on LS subwoofer output |
| CENTER_NOISE | 0 | 1: Generates noise on LS center output |
| RIGHT_NOISE | 0 | 1: Generates noise on LS right output |

| Bit Name | Reset | Function |
|------------|-------|---|
| LEFT_NOISE | 0 | 1: Generates noise on LS left output |
| NOISE_ON | 0 | 0: Noise Generation not active 1: Noise Generation is active |

TRUSRND_CONTROL**Register Description**

Address: B1h

Type: R/W

| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|-------|-------------------|-------------------------|-------|-------|-------|--------------|------------|
| 0 | TRUSRND_MONO_SRND | TRUSRND_INPUT_MODE[3:0] | | | | TRUSRND_MODE | TRUSRND_ON |

| Bit Name | Reset | Function |
|-------------------------|-------|---|
| Bit 7 | 0 | Reserved. |
| TRUSRND_MONO_SRND | 0 | 0: Left mono Srnd mode 1: Right mono Srnd mode |
| TRUSRND_INPUT_MODE[3:0] | 0000 | 0000: Mono 0001: L/R stereo (SRS mode) 0010: L/R/S (SRS mode, Prologic 1 Process) 0011: L/R/Ls/Rs (SRS mode) 0100: L/R/C (TruSurround mode) 0101: L/R/C/S (TruSurround mode, Prologic 1 Process) 0110: L/R/C/Ls/Rs (TruSurround mode) 0111: Lt/Rt (TruSurround mode) 1000: L/R/C/Ls/Rs (SRS mode, BS Digital Broadcast) 1001: L/R/C/Ls/Rs (TruSurround, Prologic 2 Music mode) |
| TRUSRND_MODE | 0 | 0: TruSurround mode 1: Bypass mode |
| TRUSRND_ON | 0 | 0: TruSurround OFF 1: TruSurround ON |

TRUSRND_INPUT_GAIN**Register Description**

Address: B6h

Type: R/W

| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|-------------------------|-------|-------|-------|-------|-------|-------|-------|
| TRUSRND_INPUT_GAIN[7:0] | | | | | | | |

| Bit Name | Reset | Function |
|-------------------------|--------------|--|
| TRUSRND_INPUT_GAIN[7:0] | 0000 0000 | Input Gain attenuation: 0000 0000: 0dB 0000 0001: -0.5dB ... 1111 1111: -127.5dB |

TRUSRND_HP_DCL**Register Description**

Address: B7h

Type: R/W

| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|-------|-------|-------|-------|-------|-------------------|--------------|-------|
| 0 | 0 | 0 | 0 | 0 | DIALOG_CLARITY_ON | HEADPHONE_ON | 0 |

| Bit Name | Reset | Function |
|-------------------|-------|--|
| Bits[7:2] | 00000 | Reserved. |
| DIALOG_CLARITY_ON | 0 | 0: Dialog Clarity OFF 1: Dialog Clarity ON |
| HEADPHONE_ON | 0 | Activate HP mode in TruSurround XT: 0: HP mode OFF 1: HP mode ON |
| Bit [0] | 0 | Reserved. |

TRUSRND_DC_ELEVATION**Register Description**

Address: B8h

Type: R/W

| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---------------------------|-------|-------|-------|-------|-------|-------|-------|
| TRUSRND_DC_ELEVATION[7:0] | | | | | | | |

| Bit Name | Reset | Function |
|---------------------------|--------------|--|
| TRUSRND_DC_ELEVATION[7:0] | 0000 1100 | Dialog Clarity Elevation: 0000 0000: 0dB 0000 0001: -0.5dB ... 1111 1111: -127.5dB |

TRUBASS_LS_CONTROL Register Description

Address: BAh

Type: R/W

| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|-------|-------|-------|-------|----------------------|-------|-------|---------------|
| 0 | 0 | 0 | 0 | TRUBASS_LS_SIZE[2:0] | | | TRUBASS_LS_ON |

| Bit Name | Reset | Function |
|----------------------|-------|--|
| Bits[7:3] | 00000 | Reserved. |
| TRUBASS_LS_SIZE[2:0] | 011 | 000: LF response at 40Hz 001: LF response at 60Hz 010: LF response at 100Hz 011: LF response at 150Hz 100: LF response at 200Hz 101: LF response at 250Hz 110: LF response at 300Hz 111: LF response at 400Hz |
| TRUBASS_LS_ON | 0 | 0: LS TruBass OFF 1: LS TruBass ON |

TRUBASS_LS_LEVEL Register Description

Address: BBh

Type: R/W

| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|-----------------------|-------|-------|-------|-------|-------|-------|-------|
| TRUBASS_LS_LEVEL[7:0] | | | | | | | |

| Bit Name | Reset | Function |
|-----------------------|--------------|--|
| TRUBASS_LS_LEVEL[7:0] | 0000 1001 | Define the amount of SRS TruBass effect for LS outputs: 0000 0000: 0dB 0000 0001: -0.5dB ... 1111 1111: -127.5dB |

TRUBASS_HP_CONTROL Register Description

Address: BCh

Type: R/W

| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|-------|-------|-------|-------|----------------------|-------|-------|---------------|
| 0 | 0 | 0 | 0 | TRUBASS_HP_SIZE[2:0] | | | TRUBASS_HP_ON |

| Bit Name | Reset | Function |
|----------------------|-------|--|
| Bits[7:3] | 00000 | Reserved. |
| TRUBASS_HP_SIZE[2:0] | 011 | 000: LF response at 40Hz 001: LF response at 60Hz 010: LF response at 100Hz 011: LF response at 150Hz 100: LF response at 200Hz 101: LF response at 250Hz 110: LF response at 300Hz 111: LF response at 400Hz |
| TRUBASS_HP_ON | 0 | 0: HP TruBass OFF 1: HP TruBass ON |

TRUBASS_HP_LEVEL Register Description

Address: BDh

Type: R/W

| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|-----------------------|-------|-------|-------|-------|-------|-------|-------|
| TRUBASS_HP_LEVEL[7:0] | | | | | | | |

| Bit Name | Reset | Function |
|-----------------------|--------------|--|
| TRUBASS_HP_LEVEL[7:0] | 0000 1001 | Define the amount of SRS TruBass effect for HP outputs: 0000 0000: 0dB 0000 0001: -0.5dB ... 1111 1111: -127.5dB |

SVC_LS_CONTROL Register Description

Address: BEh

Type: R/W

| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|-------|-------|-------|-------|-------------------|-------|------------|-----------|
| 0 | 0 | 0 | 0 | SVC_LS_INPUT[1:0] | | SVC_LS_AMP | SVC_LS_ON |

| Bit Name | Reset | Function |
|-------------------|-------|--|
| Bits[7:4] | 0000 | Reserved. |
| SVC_LS_INPUT[1:0] | 00 | Select input for peak detection in multichannel mode: 00: Left/Right 01: Center 10: Left/Right/Center |
| SVC_LS_AMP | 1 | 0: 0dB amplification in auto-mode 1: +6dB amplification in auto-mode |
| SVC_LS_ON | 0 | 0: Manual mode(simple prescaler) 1: Automatic mode |

SVC_LS_TIME_TH

Register Description

Address: BFh

Type: R/W

| | | | | | | | |
|------------------|-------|-------|-----------------------|-------|-------|-------|-------|
| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
| SVC_LS_TIME[2:0] | | | SVC_LS_THRESHOLD[4:0] | | | | |

| Bit Name | Reset | Function |
|-----------------------|-------|---|
| SVC_LS_TIME[2:0] | 100 | Time constant for the amplification (6dB gain step) in automatic mode: 000: 30ms 001: 200ms 010: 500ms 011: 1s 100: 16s 101: 32s 110: 64s 111: 128s |
| SVC_LS_THRESHOLD[4:0] | 11000 | see Table 27 and Table 28 . |

Table 27: Gain (threshold field) values in Manual mode

| Manual Mode | Gain (dB) |
|-------------|-----------|
| 00101 | +15.5 |
| 00100 | +12 |
| 00011 | +9.5 |
| 00010 | +6 |
| 00001 | +3.5 |
| 00000 | 0 |
| 11111 | -2.5 |
| 11110 | -6 |
| 11101 | -8.5 |
| 11100 | -12 |
| 11011 | -14.5 |
| 11010 | -18 |
| 11001 | -20.5 |
| 11000 | -24 |
| 10111 | -26.5 |
| 10110 | -30 |

Table 28: Threshold values in Automatic mode

| Automatic Mode | Threshold (dB) |
|----------------|----------------|
| 11111 | -2.5 |
| 11110 | -6 |
| 11101 | -8.5 |
| 11100 | -12 |
| 11011 | -14.5 |
| 11010 | -18 |
| 11001 | -20.5 |
| 11000 | -24 |
| 10111 | -26.5 |
| 10110 | -30 |

SVC_HP_CONTROL**Register Description**

Address: C0h

Type: R/W

| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|-------|-------|-------|-------|-------|-------|-------------|-----------|
| 0 | 0 | 0 | 0 | 0 | 0 | SVC_LHP_AMP | SVC_HP_ON |

| Bit Name | Reset | Function |
|-------------|--------|---|
| Bits[7:2] | 000000 | Reserved. |
| SVC_LHP_AMP | 1 | 0: 0dB amplification in auto-mode 1: +6dB amplification in auto-mode |
| SVC_HP_ON | 0 | 0: Manual mode (simple prescaler) 1: Automatic mode |

SVC_HP_TIME_TH**Register Description**

Address: C1h

Type: R/W

| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|------------------|-------|-------|-------|-----------------------|-------|-------|-------|
| SVC_HP_TIME[2:0] | | | | SVC_HP_THRESHOLD[4:0] | | | |

| Bit Name | Reset | Function |
|-----------------------|-------|---|
| SVC_HP_TIME[2:0] | 100 | Time constant for the amplification (6dB gain step) in automatic mode: 000: 30ms 001: 200ms 010: 500ms 011: 1s 100: 16s 101: 32s 110: 64s 111: 128s |
| SVC_HP_THRESHOLD[4:0] | 11000 | see Table 27 and Table 28 |

SVC_LS_GAIN**Register Description**

Address: C2h

Type: R/W

| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|-------|------------------|-------|-------|-------|-------|-------|-------|
| 0 | SVC_LS_GAIN[6:0] | | | | | | |

| Bit Name | Reset | Function |
|------------------|---------|---|
| Bit 7 | 0 | Reserved. |
| SVC_LS_GAIN[6:0] | 0000000 | Set "make-up" gain applied at SVC LS output: 0000000: +0dB 0000001: +0.5dB ... 0101110: +23dB 0101111: +23.5dB 0110000: +24dB |

SVC_HP_GAIN**Register Description**

Address: C3h

Type: R/W

| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|-------|------------------|-------|-------|-------|-------|-------|-------|
| 0 | SVC_HP_GAIN[6:0] | | | | | | |

| Bit Name | Reset | Function |
|----------|-------|-----------|
| Bit 7 | 0 | Reserved. |

| Bit Name | Reset | Function |
|------------------|---------|---|
| SVC_HP_GAIN[6:0] | 0000000 | Set "make-up" gain applied at SVC HP output: 0000000: +0dB 0000001: +0.5dB ... 0101110: +23dB 0101111: +23.5dB 0110000: +24dB |

STSRND_CONTROL**ST WideSurround Control Register**

Address: C4h

Type: R/W

www.DataSheet4U.com

| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|-------|-------|-------|-------|-------|---------------|-------------|-----------|
| 0 | 0 | 0 | 0 | 0 | STSRND_STEREO | STSRND_MODE | STSRND_ON |

| Bit Name | Reset | Function |
|---------------|-------|---|
| Bits[7:3] | 00000 | Reserved. |
| STSRND_STEREO | 0 | ST WideSurround Mode 0: ST WideSurround Sound in Mono mode (Default) 1: ST WideSurround Sound in Stereo mode |
| STSRND_MODE | 0 | ST WideSurround Sound Stereo Mode 0: Movie Mode 1: Music Mode |
| STSRND_ON | 0 | ST WideSurround Sound Enable 0: ST WideSurround Sound is disabled 1: ST WideSurround Sound is enabled |

STSRND_FREQ**ST WideSurround Sound Frequency**

Address: C5h

Type: R/W

| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|-------|-------|------------------|-------|--------------------|-------|--------------------|-------|
| 0 | 0 | STSRND_BASS[1:0] | | STSRND_MEDIUM[1:0] | | STSRND_TREBLE[1:0] | |

| Bit Name | Reset | Function |
|--------------------|-------|---|
| Bits[7:6] | 00 | Reserved. |
| STSRND_BASS[1:0] | 01 | Defines the bass frequency effect for ST WideSurround Sound. Programmable values are listed in Table 29 . |
| STSRND_MEDIUM[1:0] | 01 | Defines the medium frequency effect for ST WideSurround Sound in Movie or Mono mode (no effect in Music mode). Programmable values are listed in Table 29 . |

| Bit Name | Reset | Function |
|--------------------|-------|---|
| STSRND_TREBLE[1:0] | 01 | Defines the treble frequency effect for ST WideSurround Sound in Movie or Mono mode (no effect in Music mode). Programmable values are listed in Table 29 . |

Table 29: Phase Shifter Center Frequencies

| | Phase Shifter Center Frequency | | |
|--------------|--------------------------------|------------------|------------------|
| | BASS_FREQ[1:0] | MEDIUM_FREQ[1:0] | TREBLE_FREQ[1:0] |
| 00 | 40 Hz | 202 Hz | 2 kHz |
| 01 (Default) | 90 Hz | 416 Hz | 4 kHz |
| 10 | 120 Hz | 500 Hz | 5 kHz |
| 11 | 160 Hz | 588 Hz | 6 kHz |

STSRND_LEVEL

ST WideSurround Gain Register

Address: C6h

Type: R/W

| | | | | | | | |
|------------------|-------|-------|-------|-------|-------|-------|-------|
| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
| STSRND_GAIN[7:0] | | | | | | | |

| Bit Name | Reset | Function | | | | | | | | | | | | | | | | | | | | | | | | |
|---------------------|-----------|---|-----------|-----------|--|-----------|---------------------|------|-----------|------|-----------|-------|-----------|------|-----------|-------|-----------|------|-----------|-------|-----------|------|-------|--|-----------|----|
| STSRND_GAIN[7:0] | 10000000 | Defines the ST WideSurround Sound component gain in linear scale. <table border="1" style="margin-left: 20px;"> <thead> <tr> <th></th> <th>Level (%)</th> <th></th> <th>Level (%)</th> </tr> </thead> <tbody> <tr> <td>1000 0000 (Default)</td> <td>100%</td> <td>0000 0100</td> <td>3.1%</td> </tr> <tr> <td>0111 1111</td> <td>99.2%</td> <td>0000 0011</td> <td>2.3%</td> </tr> <tr> <td>0111 1110</td> <td>98.4%</td> <td>0000 0010</td> <td>1.6%</td> </tr> <tr> <td>0111 1101</td> <td>97.6%</td> <td>0000 0001</td> <td>0.8%</td> </tr> <tr> <td>.....</td> <td></td> <td>0000 0000</td> <td>0%</td> </tr> </tbody> </table> | | Level (%) | | Level (%) | 1000 0000 (Default) | 100% | 0000 0100 | 3.1% | 0111 1111 | 99.2% | 0000 0011 | 2.3% | 0111 1110 | 98.4% | 0000 0010 | 1.6% | 0111 1101 | 97.6% | 0000 0001 | 0.8% | | | 0000 0000 | 0% |
| | Level (%) | | Level (%) | | | | | | | | | | | | | | | | | | | | | | | |
| 1000 0000 (Default) | 100% | 0000 0100 | 3.1% | | | | | | | | | | | | | | | | | | | | | | | |
| 0111 1111 | 99.2% | 0000 0011 | 2.3% | | | | | | | | | | | | | | | | | | | | | | | |
| 0111 1110 | 98.4% | 0000 0010 | 1.6% | | | | | | | | | | | | | | | | | | | | | | | |
| 0111 1101 | 97.6% | 0000 0001 | 0.8% | | | | | | | | | | | | | | | | | | | | | | | |
| | | 0000 0000 | 0% | | | | | | | | | | | | | | | | | | | | | | | |

OMNISURROUND_CONTROL Register Description

Address: C7h

Type: R/W

| | | | | | | | |
|-------|---------------|--------------|----------------------------|-------|-------|-------|-------|
| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
| LFE | ST_VOICE[1:0] | FRONT_BYPASS | OMNI_SURND_INPUT_MODE[3:0] | | | | |

| Bit Name | Reset | Function |
|----------|-------|--|
| LFE | 0 | 0: Do not use LFE channel 1: Generate LFE channel |

| Bit Name | Reset | Function |
|------------------------------|-------|---|
| ST_VOICE[1:0] | 00 | 00: OFF 01: Low 10: Mid 11: High |
| FRONT_BYPASS | 0 | Forced to 0 |
| OMNISRND_ INPUT_MODE[3:0] | 0000 | 000: Mono 001: L/R stereo 010: L/R/S 011: L/R/Ls/Rs 100: L/R/C 101: L/R/C/S 110: L/R/C/Ls/Rs 111: Lt/Rt (Passive matrix) |
| OMNISURND_ON | 0 | 0: OmniSurround OFF 1: OmniSurround ON |

ST_DYNAMIC_BASS**Register Description**

Address: C8h

Type: R/W

| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|-----------------|-------|-------|-------|-------|----------------|-------|-------------|
| BASS_LEVEL[4:0] | | | | | BASS_FREQ[1:0] | | DYN_BASS_ON |

| Bit Name | Reset | Function |
|-----------------|-------|---|
| BASS_LEVEL[4:0] | 00000 | Set ST Dynamic Bass effect level: 00000: +0d B 00001: +0.5 dB ... 11101: +14.5 dB 11110: +15 dB 11111: +15.5 dB |
| BASS_FREQ[1:0] | 00 | 00: 100 Hz Cut-Off frequency 01: 150 Hz Cut-Off frequency 10: 200 Hz Cut-Off frequency 11: Reserved |
| DYN_BASS_ON | 0 | 0: ST Dynamic Bass OFF 1: ST Dynamic Bass ON |

12.16 5-Band Equalizer / Bass-Treble for Loudspeakers

LS_EQ_BT_CTRL

Loudspeakers Equalizer Control Register

Address: C9h

Type: R/W

| | | | | | | | |
|-------|-------|-------|-------|-------|-------|-------------|----------|
| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
| 0 | 0 | 0 | 0 | 0 | 0 | LS_EQ_BT_SW | LS_EQ_ON |

| Bit Name | Reset | Function |
|-------------|--------|--|
| Bits[7:2] | 000000 | Reserved. |
| LS_EQ_BT_SW | 0 | 5-Band Equalizer or Bass-Treble selection 0: 5-Band Equalizer is selected for Loudspeakers. 1: Bass-Treble is selected for Loudspeakers. |
| LS_EQ_ON | 1 | 5-Band Equalizer/Bass-Treble for loudspeakers Enable 0: 5-Band Equalizer/Bass-Treble is disabled 1: 5-Band Equalizer/Bass-Treble is enabled (Default) |

EQ_BANDX_GAIN

Loudspeakers Equalizer Gain Register for BandX

Address: CAh to CEh

Type: R/W

| | | | | | | | |
|----------|-------|-------|-------|-------|-------|-------|-------|
| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
| EQ_BANDX | | | | | | | |

| Bit Name | Reset | Function |
|---------------|--------------|--|
| EQ_BANDX[7:0] | 0000 0000 | BandX gain adjustment within a range from -12 dB to +12 dB in steps of 0.25 dB. Band1: 100 Hz, Band2: 330 Hz, Band3: 1 KHz, Band4: 3.3 KHz, Band5: 10 KHz, see Table 30 . |

Table 30: Loudspeakers Equalizer/Bass-Treble Gain Values (and Headphone Bass-Treble Gain Values)

| Value | Gain G (dB) |
|--------------------|-------------|
| 00110000 | +12 |
| 00101111 | +11.75 |
| 00101110 | +11.50 |
| | |
| 00000000 (Default) | 0 |
| | |
| 10101110 | -11.50 |

Table 30: Loudspeakers Equalizer/Bass-Treble Gain Values (and Headphone Bass-Treble Gain Values)

| Value | Gain G (dB) |
|----------|-------------|
| 10101111 | -11.75 |
| 10110000 | -12 |

LS_BASS_GAIN**Loudspeakers Bass Gain Register**

Address: CFh

Type: R/W

Bit 7 Bit 6 Bit 5 Bit 4 Bit 3 Bit 2 Bit 1 Bit 0

| |
|--------------|
| LS_BASS[7:0] |
|--------------|

| Bit Name | Reset | Function |
|--------------|--------------|--|
| LS_BASS[7:0] | 0000 0000 | Bass gain adjustment within a range from -12 dB to +12 dB in steps of 0.25 dB. |

LS_TREBLE_GAIN**Loudspeakers Treble Gain Register**

Address: D0h

Type: R/W

Bit 7 Bit 6 Bit 5 Bit 4 Bit 3 Bit 2 Bit 1 Bit 0

| |
|-----------|
| LS_TREBLE |
|-----------|

| Bit Name | Reset | Function |
|----------------|--------------|--|
| LS_TREBLE[7:0] | 0000 0000 | Treble gain adjustment within a range from -12 dB to +12 dB in steps of 0.25 dB. |

12.17 Headphone Bass-Treble**HP_BT_CONTROL****Headphone Bass-Treble Control Register**

Address: D1h

Type: R/W

Bit 7 Bit 6 Bit 5 Bit 4 Bit 3 Bit 2 Bit 1 Bit 0

| | | | | | | | | |
|---|---|---|---|---|---|---|---|----------|
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | HP_BT_ON |
|---|---|---|---|---|---|---|---|----------|

| Bit Name | Reset | Function |
|------------|---------|-----------|
| Bits [7:1] | 0000000 | Reserved. |

| Bit Name | Reset | Function |
|----------|-------|--|
| HP_EQ_ON | 1 | Bass-Treble for headphone Enable 0: Bass-Treble is disabled 1: Bass-Treble is enabled (Default) |

HP_BASS_GAIN**Headphone Bass Gain**

Address: D2h

Type: R/W

Bit 7 Bit 6 Bit 5 Bit 4 Bit 3 Bit 2 Bit 1 Bit 0

HP_BASS_GAIN[7:0]

| Bit Name | Reset | Function |
|-------------------|----------|---|
| HP_BASS_GAIN[7:0] | 00000000 | Gain Tuning of Headphone Bass Frequency Gain may be programmed within a range between +12 dB and -12 dB in steps of 0.25 dB. Programmable values are listed in Table 30 . |

HP_TREBLE_GAIN**Headphone Treble Gain**

Address: D3h

Type: R/W

Bit 7 Bit 6 Bit 5 Bit 4 Bit 3 Bit 2 Bit 1 Bit 0

HP_TREBLE_GAIN[4:0]

| Bit Name | Reset | Function |
|---------------------|----------|---|
| HP_TREBLE_GAIN[7:0] | 00000000 | Gain Tuning of Headphone Treble Frequency Gain may be programmed within a range between +12 dB and -12 dB in steps of 0.25 dB. Programmable values are listed in Table 30 . |

OUTPUT_BASS_MNGT**Register Description**

Address: D4h

Type: R/W

Bit 7 Bit 6 Bit 5 Bit 4 Bit 3 Bit 2 Bit 1 Bit 0

| | | | | | | | |
|----------------|---|------------|-------------|---|---------------|--|--|
| BASS_MANAGE_ON | 0 | SUB_ACTIVE | GAIN_SWITCH | 0 | OCFG_NUM[2:0] | | |
|----------------|---|------------|-------------|---|---------------|--|--|

| Bit Name | Reset | Function |
|----------------|-------|--|
| BASS_MANAGE_ON | 1 | 0: BassManagement disables 1: BassManagement enabled |
| Bit 6 | 0 | Reserved. |
| SUB_ACTIVE | 0 | 0: Subwoofer output is disabled (only in config 2,3,4) 1: Subwoofer output is active |
| GAIN_SWITCH | 0 | 0: Level adjustment ON 1: Level adjustment OFF |
| OCFG_NUM | 000 | 000: Bass Management Configuration 0 (refer to Figure 13) 001: Bass Management Configuration 1 (refer to Figure 14) 010: Bass Management Configuration 2 (refer to Figure 15) 011: Bass Management Configuration 3 (refer to Figure 16) 100: Bass Management Configuration 4 (refer to Figure 17) |
| Bit 3 | 0 | Reserved. |

LS_LOUDNESS**Register Description**

Address: D5h

Type: R/W

| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|-------|------------------------|-------|-------|----------------------|-------|-------|------------|
| 0 | LS_LOUD_THRESHOLD[2:0] | | | LS_LOUD_GAIN_HR[2:0] | | | LS_LOUD_ON |

| Bit Name | Reset | Function |
|------------------------|-------|---|
| Bit 7 | 0 | Reserved. |
| LS_LOUD_THRESHOLD[2:0] | 000 | Define the volume threshold level since which loudness effect is applied : 000: 0dB 001: -6dB 010: -12dB 011: -18dB 100: -24dB 101: -32dB 110: -36dB 111: -42dB |
| LS_LOUD_GAIN_HR[2:0] | 010 | Define the amount of Treble added by loudness effect: 000: 0dB 001: 3dB 010: 6dB 011: 9dB 100: 12dB 101: 15dB 110: 18dB |
| LS_LOUD_ON | 0 | 0: Loudness is not active on LS output 1: Loudness is active on LS output |

HP_LOUDNESS

Register Description

Address: D6h

Type: R/W

| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|-------|------------------------|-------|----------------------|-------|-------|------------|-------|
| 0 | HP_LOUD_THRESHOLD[2:0] | | HP_LOUD_GAIN_HR[2:0] | | | HP_LOUD_ON | |

| Bit Name | Reset | Function |
|------------------------|-------|---|
| Bit 7 | 0 | Reserved. |
| HP_LOUD_THRESHOLD[2:0] | 000 | Define the volume threshold level since which loudness effect is applied : 000: 0dB 001: -6dB 010: -12dB 011: -18dB 100: -24dB 101: -32dB 110: -36dB 111: -42dB |
| HP_LOUD_GAIN_HR[2:0] | 010 | Define the amount of Treble added by loudness effect: 000: 0dB 001: 3dB 010: 6dB 011: 9dB 100: 12dB 101: 15dB 110: 18dB |
| HP_LOUD_ON | 0 | 0: Loudness is not active on HP output 1: Loudness is active on HP output |

12.18 Volume

VOLUME_MODES

Set the Volume Modes

Address: D7h

Type: R/W

| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|-----------------------|-----------------------|-------|-------|-------------------|------------------|----------------|----------------|
| ANTICLIP_HP_VOL_CLAMP | ANTICLIP_LS_VOL_CLAMP | 0 | 0 | SCART_VOLUME_MODE | SRND_VOLUME_MODE | HP_VOLUME_MODE | LS_VOLUME_MODE |

| Bit Name | Reset | Function |
|-----------------------|-------|---|
| ANTICLIP_HP_VOL_CLAMP | 1 | The output level is clamped depending on the HP Bass-Treble value to avoid any possible signal clipping on HP output. 0: Volume clamp on HP output is not active 1: Volume clamp on HP output is active |

| Bit Name | Reset | Function |
|-----------------------|-------|---|
| ANTICLIP_LS_VOL_CLAMP | 1 | The output level is clamped depending on the LS Equalizer or LS Bass-Treble value to avoid any possible signal clipping on LS output. 0: Volume clamp on LS output is not active 1: Volume clamp on LS output is active |
| Bits[5:4] | 00 | Reserved. |
| SCART_VOLUME_MODE | 0 | Volume mode for SCART output: 0: Independant 1: Differential |
| SRND_VOLUME_MODE | 1 | Volume mode for Headphone output: 0: Independant 1: Differential |
| HP_VOLUME_MODE | 1 | Volume mode for Surround output: 0: Independant 1: Differential |
| LS_VOLUME_MODE | 1 | Volume mode for LS output: 0: Independant 1: Differential |

LS_L_VOLUME_MSB**Register Description**

Address: D8h

Type: R/W

Bit 7 Bit 6 Bit 5 Bit 4 Bit 3 Bit 2 Bit 1 Bit 0

LS_L_VOLUME_MSB[7:0]

| Bit Name | Reset | Function |
|----------------------|--------------|---|
| LS_L_VOLUME_MSB[7:0] | 1001 1000 | LS 10 bits volume Left channel 8 MSB in independent mode or LS 10 bits volume Left and Right channels 8 MSB in differential mode. See Figure 19: Volume Control on page 36 for range values. |

LS_L_VOLUME_LSB**Register Description**

Address: D9h

Type: R/W

Bit 7 Bit 6 Bit 5 Bit 4 Bit 3 Bit 2 Bit 1 Bit 0

0 0 0 0 0 0 LS_L_VOLUME_LSB[1:0]

| Bit Name | Reset | Function |
|-----------|--------|-----------|
| Bits[7:2] | 000000 | Reserved. |

| Bit Name | Reset | Function |
|----------------------|-------|---|
| LS_L_VOLUME_LSB[1:0] | 00 | LS 10 bits volume Left channel 2 LSB in independent mode or LS 10 bits volume Left and Right channels 2 LSB in differential mode. See Figure 19: Volume Control on page 36 for range values. |

The volume value is defined by the following formula:

$Vol (dB) = \text{Decimal value of } LS_L_VOLUME_MSB \times 0.5 + \text{Decimal value of } LS_L_VOLUME_LSB \times 0.125 - 116 \text{ dB}$
(each step is 0.125 dB).

LS_R_VOLUME_MSB**Register Description**

Address: DAh

Type: R/W

| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|----------------------|-------|-------|-------|-------|-------|-------|-------|
| LS_R_VOLUME_MSB[7:0] | | | | | | | |

| Bit Name | Reset | Function |
|----------------------|--------------|--|
| LS_R_VOLUME_MSB[7:0] | 0000000 0 | LS 10 bits volume Right channel 8 MSB in independent mode or LS 10 bits Left and Right balance 8 MSB in differential mode. See Figure 19: Volume Control on page 36 or Figure 20: Differential Balance on page 37 . |

LS_R_VOLUME_LSB**Register Description**

Address: DBh

Type: R/W

| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|-------|-------|-------|-------|-------|-------|----------------------|-------|
| 0 | 0 | 0 | 0 | 0 | 0 | LS_R_VOLUME_LSB[1:0] | |

| Bit Name | Reset | Function |
|----------------------|--------|--|
| Bits[7:2] | 000000 | Reserved. |
| LS_R_VOLUME_LSB[1:0] | 00 | LS 10 bits volume Right channel 2 LSB in independent mode or LS 10 bits Left and Right balance 2 LSB in differential mode. See Figure 19: Volume Control on page 36 or Figure 20: Differential Balance on page 37 . |

LS_C_VOLUME_MSB**Register Description**

Address: DCh

Type: R/W

| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|----------------------|-------|-------|-------|-------|-------|-------|-------|
| LS_C_VOLUME_MSB[7:0] | | | | | | | |

| Bit Name | Reset | Function |
|----------------------|--------------|--|
| LS_C_VOLUME_MSB[7:0] | 1001 1000 | LS 10 bits volume Center channel 8 MSB See Figure 19: Volume Control on page 36 for range values. |

LS_C_VOLUME_LSB**Register Description**

Address: DDh

Type: R/W

| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|-------|-------|-------|-------|-------|-------|----------------------|-------|
| 0 | 0 | 0 | 0 | 0 | 0 | LS_C_VOLUME_LSB[1:0] | |

www.DataSheet4U.com

| Bit Name | Reset | Function |
|----------------------|--------|--|
| Bits[7:2] | 000000 | Reserved. |
| LS_C_VOLUME_LSB[1:0] | 00 | LS 10 bits volume Center channel 2 LSB See Figure 19: Volume Control on page 36 for range values. |

The volume value is defined by the following formula:

Vol (dB) = Decimal value of LS_C_VOLUME_MSB x 0.5 + Decimal value of LS_C_VOLUME_LSB x 0.125 - 116 dB
(each step is 0.125 dB).

LS_SUB_VOLUME_MSB**Register Description**

Address: DEh

Type: R/W

| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|------------------------|-------|-------|-------|-------|-------|-------|-------|
| LS_SUB_VOLUME_MSB[7:0] | | | | | | | |

| Bit Name | Reset | Function |
|------------------------|--------------|---|
| LS_SUB_VOLUME_MSB[7:0] | 1001 1000 | LS 10 bits volume Subwoofer channel 8 MSB See Figure 19: Volume Control on page 36 for range values. |

LS_SUB_VOLUME_LSB

Register Description

Address: DFh

Type: R/W

| | | | | | | | |
|-------|-------|-------|-------|-------|-------|------------------------|-------|
| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
| 0 | 0 | 0 | 0 | 0 | 0 | LS_SUB_VOLUME_LSB[1:0] | |

| Bit Name | Reset | Function |
|------------------------|--------|---|
| Bits[7:2] | 000000 | Reserved. |
| LS_SUB_VOLUME_LSB[1:0] | 00 | LS 10 bits volume Subwoofer channel 2 LSB See Figure 19: Volume Control on page 36 for range values. |

The volume value is defined by the following formula:

Vol (dB) = Decimal value of LS_SUB_VOLUME_MSB x 0.5 + Decimal value of LS_SUB_VOLUME_LSB x 0.125 - 116 dB (each step is 0.125 dB).

LS_SL_VOLUME_MSB

Register Description

Address: E0h

Type: R/W

| | | | | | | | |
|-----------------------|-------|-------|-------|-------|-------|-------|-------|
| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
| LS_SL_VOLUME_MSB[7:0] | | | | | | | |

| Bit Name | Reset | Function |
|-----------------------|--------------|--|
| LS_SL_VOLUME_MSB[7:0] | 1001 1000 | LS 10 bits volume Left surround channel 8 MSB in independent mode or LS 10 bits Left and Right surround volume 8 MSB in differential mode. See Figure 19: Volume Control on page 36 or Figure 20: Differential Balance on page 37 . |

LS_SL_VOLUME_LSB**Register Description**

Address: E1h

Type: R/W

| | | | | | | | |
|-------|-------|-------|-------|-------|-------|-----------------------|-------|
| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
| 0 | 0 | 0 | 0 | 0 | 0 | LS_SL_VOLUME_LSB[1:0] | |

| Bit Name | Reset | Function |
|-----------------------|--------|--|
| Bits[7:2] | 000000 | Reserved. |
| LS_SL_VOLUME_LSB[1:0] | 00 | LS 10 bits volume Left surround channel 2 LSB in independent mode or LS 10 bits Left and Right surround volume 2 LSB in differential mode. See Figure 19: Volume Control on page 36 or Figure 20: Differential Balance on page 37 . |

The volume value is defined by the following formula:

Vol (dB) = Decimal value of LS_SL_VOLUME_MSB x 0.5 + Decimal value of LS_SL_VOLUME_LSB x 0.125 - 116 dB
(each step is 0.125 dB).

LS_SR_VOLUME_MSB**Register Description**

Address: E2h

Type: R/W

| | | | | | | | |
|-----------------------|-------|-------|-------|-------|-------|-------|-------|
| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
| LS_SR_VOLUME_MSB[7:0] | | | | | | | |

| Bit Name | Reset | Function |
|-----------------------|----------|---|
| LS_SR_VOLUME_MSB[7:0] | 00000000 | LS 10 bits volume Right channel 8 MSB in independent mode or LS 10 bits surround Left and Right balance 8 MSB in differential mode. See Figure 19: Volume Control on page 36 or Figure 20: Differential Balance on page 37 . |

LS_SR_VOLUME_LSB**Register Description**

Address: E3h

Type: R/W

| | | | | | | | |
|-------|-------|-------|-------|-------|-------|-----------------------|-------|
| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
| 0 | 0 | 0 | 0 | 0 | 0 | LS_SR_VOLUME_LSB[1:0] | |

| Bit Name | Reset | Function |
|-----------|--------|-----------|
| Bits[7:2] | 000000 | Reserved. |

| Bit Name | Reset | Function |
|-----------------------|-------|---|
| LS_SR_VOLUME_LSB[1:0] | 00 | LS 10 bits volume Right channel 8 MSB in independent mode or LS 10 bits surround Left and Right balance 2 LSB in differential mode. See Figure 19: Volume Control on page 36 or Figure 20: Differential Balance on page 37 . |

The volume value is defined by the following formula:

$Vol (dB) = \text{Decimal value of LS_SR_VOLUME_MSB} \times 0.5 + \text{Decimal value of LS_SR_VOLUME_LSB} \times 0.125 - 116 \text{ dB}$
(each step is 0.125 dB).

LS_MASTER_VOLUME_MSB Register Description

Address: E4h

Type: R/W

| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---------------------------|-------|-------|-------|-------|-------|-------|-------|
| LS_MASTER_VOLUME_MSB[7:0] | | | | | | | |

| Bit Name | Reset | Function |
|---------------------------|--------------|--|
| LS_MASTER_VOLUME_MSB[7:0] | 1110100 0 | LS 10 bits volume Master channel 8 MSB See Figure 19: Volume Control on page 36 for range values. |

LS_MASTER_VOLUME_LSB Register Description

Address: E5h

Type: R/W

| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|-------|-------|-------|-------|-------|-------|---------------------------|-------|
| 0 | 0 | 0 | 0 | 0 | 0 | LS_MASTER_VOLUME_LSB[1:0] | |

| Bit Name | Reset | Function |
|---------------------------|--------|--|
| Bits[7:2] | 000000 | Reserved. |
| LS_MASTER_VOLUME_LSB[1:0] | 00 | LS 10 bits volume Master channel 2 LSB See Figure 19: Volume Control on page 36 for range values. |

The volume value is defined by the following formula:

$Vol (dB) = \text{Decimal value of LS_MASTER_VOLUME_MSB} \times 0.5 + \text{Decimal value of LS_MASTER_VOLUME_LSB} \times 0.125 - 116 \text{ dB}$
(each step is 0.125 dB).

HP_L_VOLUME_MSB**Register Description**

Address: E6h

Type: R/W

Bit 7 Bit 6 Bit 5 Bit 4 Bit 3 Bit 2 Bit 1 Bit 0

HP_L_VOLUME_MSB[7:0]

| Bit Name | Reset | Function |
|----------------------|--------------|--|
| HP_L_VOLUME_MSB[7:0] | 1001 1000 | HP 10 bits volume Left channel 8 MSB in independent mode or HP 10 bits Left and Right volume 8 MSB in differential mode. See Figure 19: Volume Control on page 36 or Figure 20: Differential Balance on page 37 . |

www.DataSheet4U.com

HP_L_VOLUME_LSB**Register Description**

Address: E7h

Type: R/W

Bit 7 Bit 6 Bit 5 Bit 4 Bit 3 Bit 2 Bit 1 Bit 0

0 0 0 0 0 0 HP_L_VOLUME_LSB[1:0]

| Bit Name | Reset | Function |
|----------------------|--------|--|
| Bits[7:2] | 000000 | Reserved. |
| HP_L_VOLUME_LSB[1:0] | 00 | HP 10 bits volume Left channel 2 LSB in independent mode or HP 10 bits Left and Right volume 2 LSB in differential mode. See Figure 19: Volume Control on page 36 or Figure 20: Differential Balance on page 37 . |

The volume value is defined by the following formula:

$Vol (dB) = \text{Decimal value of HP_L_VOLUME_MSB} \times 0.5 + \text{Decimal value of HP_L_VOLUME_LSB} \times 0.125 - 116 \text{ dB}$
(each step is 0.125 dB).

HP_R_VOLUME_MSB**Register Description**

Address: E8h

Type: R/W

Bit 7 Bit 6 Bit 5 Bit 4 Bit 3 Bit 2 Bit 1 Bit 0

HP_R_VOLUME_MSB[7:0]

| Bit Name | Reset | Function |
|----------------------|--------------|--|
| HP_R_VOLUME_MSB[7:0] | 0000000 0 | HP 10 bits volume Right channel 8 MSB in independent mode or HP 10 bits Left and Right balance 8 MSB in differential mode. See Figure 19: Volume Control on page 36 or Figure 20: Differential Balance on page 37 . |

HP_R_VOLUME_LSB

Register Description

Address: E9h

Type: R/W

| | | | | | | | |
|-------|-------|-------|-------|-------|-------|----------------------|-------|
| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
| 0 | 0 | 0 | 0 | 0 | 0 | HP_R_VOLUME_LSB[1:0] | |

| Bit Name | Reset | Function |
|----------------------|--------|---|
| Bits[7:2] | 000000 | Reserved. |
| HP_R_VOLUME_LSB[1:0] | 00 | HP 10 bits volume Right channel 2 LSB in independent mode or HP 10 bits Left and Right balance 2LSB in differential mode. See Figure 19: Volume Control on page 36 or Figure 20: Differential Balance on page 37 . |

SCART_L_VOLUME_MSB

Register Description

Address: EAh

Type: R/W

| | | | | | | | |
|-------------------------|-------|-------|-------|-------|-------|-------|-------|
| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
| SCART_L_VOLUME_MSB[7:0] | | | | | | | |

| Bit Name | Reset | Function |
|-------------------------|-----------|---|
| SCART_L_VOLUME_MSB[7:0] | 1101110 1 | SCART 10 bits volume Left channel 8 MSB in independent mode or SCART10 bits Left and Right volume 8 MSB in differential mode. See Figure 19: Volume Control on page 36 or Figure 20: Differential Balance on page 37 . |

SCART_L_VOLUME_LSB Register Description

Address: EBh

Type: R/W

| | | | | | | | |
|-------|-------|-------|-------|-------|-------|-------------------------|-------|
| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
| 0 | 0 | 0 | 0 | 0 | 0 | SCART_L_VOLUME_LSB[1:0] | |

| Bit Name | Reset | Function |
|-------------------------|--------|---|
| Bits[7:2] | 000000 | Reserved. |
| SCART_L_VOLUME_LSB[1:0] | 00 | SCART 10 bits volume Left channel 2 LSB in independent mode or SCART10 bits Left and Right volume 2 LSB in differential mode. See Figure 19: Volume Control on page 36 or Figure 20: Differential Balance on page 37 . |

The volume value is defined by the following formula:

Vol (dB) = Decimal value of SCART_L_VOLUME_MSB x 0.5 + Decimal value of SCART_L_VOLUME_LSB x 0.125 - 116 dB (each step is 0.125 dB).

SCART_R_VOLUME_MSB Register Description

Address: ECh

Type: R/W

| | | | | | | | |
|-------------------------|-------|-------|-------|-------|-------|-------|-------|
| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
| SCART_R_VOLUME_MSB[7:0] | | | | | | | |

| Bit Name | Reset | Function |
|-------------------------|----------|---|
| SCART_R_VOLUME_MSB[7:0] | 11011101 | SCART 10 bits volume Right channel 8 MSB in independent mode or SCART10 bits Left and Right balance 8 MSB in differential mode. See Figure 19: Volume Control on page 36 or Figure 20: Differential Balance on page 37 . |

SCART_R_VOLUME_LSB Register Description

Address: EDh

Type: R/W

| | | | | | | | |
|-------|-------|-------|-------|-------|-------|-------------------------|-------|
| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
| 0 | 0 | 0 | 0 | 0 | 0 | SCART_R_VOLUME_LSB[1:0] | |

| Bit Name | Reset | Function |
|-----------|--------|-----------|
| Bits[7:2] | 000000 | Reserved. |

| Bit Name | Reset | Function |
|-------------------------|-------|---|
| SCART_R_VOLUME_LSB[1:0] | 00 | SCART 10 bits volume Right channel 2 LSB in independent mode or SCART10 bits Left and Right balance 2 LSB in differential mode. See Figure 19: Volume Control on page 36 or Figure 20: Differential Balance on page 37 . |

12.19 Beeper

BEEPER_ON

Beeper Activation Register

Address: EEh

Type: R/W

| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|-------|-------|-------|-------|-------|-------|-------|-----------|
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | BEEPER_ON |

| Bit Name | Reset | Function |
|------------|---------|--|
| Bits [7:1] | 0000000 | Reserved. |
| BEEPER_ON | 0 | Beeper Enable 0: Beeper muted (Default.) 1: Beeper enabled. |

BEEPER_MODE

Beeper Control Register

Address: EFh

Type: R/W

| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|-------|-------|-------|-----------------|--------------|-------------|-------|-------|
| 0 | 0 | 0 | BEEPER_DURATION | BEEPER_PULSE | BEEPER_PATH | | |

| Bit Name | Reset | Function |
|-----------------------|-------|---|
| Bits [7:5] | 000 | Reserved. |
| BEEPER_DURATION [4:3] | 00 | Define beeper duration when set to pulse mode. |
| BEEPER_PULSE | 0 | Set beeper pulse mode 0: Pulse mode selected. 1: Continuous mode selected. |
| BEEPER_PATH [1:0] | 11 | Set the output channels when beeper is active 00: no channels. 01: Loudspeakers only. 10: Headphone only. 11: Loudspeakers and Headphone selected. |

BEEPER_FREQ_VOL**Beeper Frequency and Volume Settings Register**

Address: F0h

Type: R/W

| | | | | | | | |
|----------------|-------|-------|---------------|-------|-------|-------|-------|
| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
| BEEP_FREQ[2:0] | | | BEEP_VOL[4:0] | | | | |

| Bit Name | Reset | Function |
|----------------|-------|---|
| BEEP_FREQ[2:0] | 011 | Defines the frequency of the beeper tone from 62.5 Hz to 8 kHz in octaves 000: 62.5 Hz 100: 1 kHz 001: 125 Hz 101: 2 kHz 010: 250 Hz 110: 4 kHz 011: 500 Hz (Default) 111: 8 kHz |
| BEEP_VOL[4:0] | 10000 | Defines the Beeper volume from 0 to -93 dB in steps of 3 dB. 11111: 0 dB (1 V _{RMS}) ... 11110: -3 dB 00011: -84 dB 11101: -6 dB 00010: -87 dB ... 00001: -90 dB 10000: -48 dB (Default) 00000: -93 dB |

12.20 Mute**MUTE_DIGITAL****Register Description**

Address: F1h

Type: R/W

| | | | | | | | |
|-----------------|-------|-------|--------------|----------------|------------|----------|-----------|
| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
| AUTOSTD_MUTE_ON | 0 | 0 | SCART_D_MUTE | SRND_HP_D_MUTE | SUB_D_MUTE | C_D_MUTE | LS_D_MUTE |

| Bit Name | Reset | Function |
|-----------------|-------|---|
| AUTOSTD_MUTE_ON | 1 | 0: autostandard can not mute outputs 1: autostandard can mute outputs when no signal is detected |
| Bit s[6:5] | 00 | |
| SCART_D_MUTE | 1 | SCART left/right digital soft mute 0: signal un-muted 1: signal muted |
| SRND_HP_D_MUTE | 1 | LS Surround/HP left/right digital soft mute 0: signal un-muted 1: signal muted |
| SUB_D_MUTE | 1 | LS Subwoofer digital soft mute 0: signal un-muted 1: signal muted |

| Bit Name | Reset | Function |
|-----------|-------|--|
| C_D_MUTE | 1 | LS Center digital soft mute 0: signal un-muted 1: signal muted |
| LS_D_MUTE | 1 | LS left/right digital soft mute 0: signal un-muted 1: signal muted |

12.21 S/PDIF

S/PDIF_OUT_CONFIG

S/PDIF Output Configuration Register

www.DataSheet4U.com

Address: F2h

Type: R/W

| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|-------|-------|-------|-------|-------|-----------------|-------------------|-------|
| 0 | 0 | 0 | 0 | 0 | S/PDIF_OUT_MUTE | S/PDIF_OUT_SELECT | |

| Bit Name | Reset | Function |
|------------------------|-------|--|
| Bits [7:3] | 00000 | Reserved. |
| S/PDIF_OUT_MUTE | 1 | S/PDIF Output Mute: 0: S/PDIF Output unmuted. 1: S/PDIF Output muted. |
| S/PDIF_OUT_SELECT[1:0] | 00 | S/PDIF Output channel selection: 00: output SCART signal 01: output LS L-R signal 10: output C/SUB signal 11: ouptut Sur/HP signal |

12.22 Headphone Configuration

HEADPHONE_CONFIG

Headphone Configuration Register

Address: F3h

Type: R/W

| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|-------|-------|-------|-------|----------|------------|---------------|-------------|
| 0 | 0 | 0 | 0 | HP_FORCE | HP_LS_MUTE | HP_DET_ACTIVE | HP_DETECTED |

| Bit Name | Reset | Function |
|------------|-------|-----------|
| Bits [7:4] | 0000 | Reserved. |

| Bit Name | Reset | Function |
|---------------|-------|---|
| HP_FORCE | 0 | 1: force output of the HP signal (bypass surround) |
| HP_LS_MUTE | 0 | 0: when HP is detected and active, LS are not muted 1: when HP is detected and active, LS are muted |
| HP_DET_ACTIVE | 1 | 0: HP detection is not active 1: HP detection is active, when HP detected, Surround signal is bypassed and HP signal is output on HP |
| HP_DETECTED | 0 | 1: When a signal is detected on HP_DET pin (STATUS) |

12.23 DAC Control

www.DataSheet4U.com **DAC_CONTROL**

DAC Control Register

Address: F4h

Type: R/W

| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|-------|-------|------------|----------------|--------------|---------------|---------------|----------|
| 0 | 0 | S/PDIF_MUX | DAC_SCART_MUTE | DAC_SHP_MUTE | DAC_CSUB_MUTE | DAC_LSLR_MUTE | POWER_UP |

| Bit Name | Reset | Function |
|----------------|-------|--|
| Bits [7:6] | 00 | Reserved. |
| S/PDIF_MUX | 0 | redirect external or internal S/PDIF source to S/PDIF output : 0: internal S/PDIF 1: external S/PDIF |
| DAC_SCART_MUTE | 1 | SCART left/right analog soft mute 0: signal un-muted 1: signal muted |
| DAC_SHP_MUTE | 1 | Surround/HP left/right analog soft mute 0: signal un-muted 1: signal muted |
| DAC_CSUB_MUTE | 1 | Center/Subwoofer analog soft mute 0: signal un-muted 1: signal muted |
| DAC_LSLR_MUTE | 1 | LS left/right analog soft mute 0: signal un-muted 1: signal muted |
| POWER_UP | 1 | 0: DACs Power OFF 1: Power ON |

SPDIF_CHANNEL_STATUS

Register Description

Address: F9h

Type: R/W

| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|----------------|-------|-------|----------|-------|-----------|-----------|---------|
| CHANNEL_STATUS | | | EMPHASIS | | COPYRIGHT | NON_AUDIO | PRO_CON |

| Bit Name | Reset | Function |
|---------------------|-------|--|
| CHANNEL_STATUS[7:6] | 00 | Channel status mode: 00: Mode zero other values: reserved |
| EMPHASIS[5:3] | 000 | Emphasis: according to IEC60958 specification |
| COPYRIGHT | 0 | Copyright: 0: Asserted 1: Not asserted |
| NON_AUDIO | 0 | Non-audio: 0: Linear PCM 1: Non-audio signal |
| PRO_CON | 0 | Select Professional or Consumer modes: 0: Consumer 1: Professional |

12.24 AutoStandard Coefficients Settings

AUTOSTD_COEFF_CTRL

Register Description

Address: FBh

Type: R/W

| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|-------|-------|-------|-------|-------|-------|-------|-------------------------|
| 0 | 0 | 0 | 0 | 0 | 0 | | AUTOSTD_COEFF_CTRL[1:0] |

| Bit Name | Reset | Function |
|-------------------------|--------|--|
| Bits [7:2] | 000000 | Reserved. |
| AUTOSTD_COEFF_CTRL[1:0] | 01 | Control the Demod filter coeff table settings 01: init Coeffs to ROM values 10: Update Coeffs with I2C value |

AUTOSTD_COEFF_INDEX_MSB Register Description

Address: FCh

Type: R/W

| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|-------|-------|-------|-------|-------|-------|-------|-------------------------|
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | AUTOSTD_COEFF_INDEX_MSB |

| Bit Name | Reset | Function |
|-------------------------|---------|------------------------------------|
| Bits [7:2] | 0000000 | Reserved. |
| AUTOSTD_COEFF_INDEX_MSB | 0 | FIR Coefficients table index (MSB) |

AUTOSTD_COEFF_INDEX_LSB Register Description

Address: FDh

Type: R/W

| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|------------------------------|-------|-------|-------|-------|-------|-------|-------|
| AUTOSTD_COEFF_INDEX_LSB[7:0] | | | | | | | |

| Bit Name | Reset | Function |
|------------------------------|--------------|------------------------------------|
| AUTOSTD_COEFF_INDEX_LSB[7:0] | 0000 0000 | FIR Coefficients table index (LSB) |

AUTOSTD_COEFF_VALUE Register Description

Address: FEh

Type: R/W

| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|--------------------------|-------|-------|-------|-------|-------|-------|-------|
| AUTOSTD_COEFF_VALUE[7:0] | | | | | | | |

| Bit Name | Reset | Function |
|--------------------------|--------------|----------|
| AUTOSTD_COEFF_VALUE[7:0] | 0000 0000 | Reserved |

13 Electrical Characteristics

Test Conditions: $T_{\text{OPER}} = 25^{\circ}\text{C}$, $V_{\text{CC}_H} = 8\text{V}$, $V_{\text{XX}_{18}} = 1.8\text{V}$, $V_{\text{XX}_{33}} = 3.3\text{V}$, Crystal at 27MHz, default register values for synthesizer, otherwise specified.

13.1 Absolute Maximum Ratings

| Symbol | Parameter | Value | Units |
|----------------------|---|-------------|--------------------|
| $V_{\text{XX}_{18}}$ | Analog and Digital 1.8 V Supply Voltage ($V_{\text{CC}_{18_CLK1}}$, $V_{\text{CC}_{18_CLK2}}$, $V_{\text{CC}_{18_IF}}$, $V_{\text{DD}_{18}}$, $V_{\text{DD}_{18_CONV}}$, $V_{\text{DD}_{18_ADC}}$) | 2.5 | V |
| $V_{\text{XX}_{33}}$ | Analog and Digital 3.3 V Supply Voltage ($V_{\text{CC}_{33_SC}}$, $V_{\text{CC}_{33_LS}}$, $V_{\text{DD}_{33_IO1}}$, $V_{\text{DD}_{33_IO2}}$, $V_{\text{DD}_{33_CONV}}$, $V_{\text{CC}_{NISO}}$) | 4.0 | V |
| HV_{CC} | Analog Supply High Voltage (V_{CC_H}) | 8.8 | V |
| V_{ESD} | Capacitor 100 pF discharged via 1.5 k Ω serial resistor (Human Body Model) | 4 | kV |
| T_{OPER} | Operating Ambient Temperature | 0, +70 | $^{\circ}\text{C}$ |
| T_{STG} | Storage Temperature | -55 to +150 | $^{\circ}\text{C}$ |

13.2 Thermal Data

| Symbol | Parameter | Value | Units |
|-------------------|--|-------|-----------------------------|
| R_{thJA} | Junction-to-Ambient Thermal Resistance | 42 | $^{\circ}\text{C}/\text{W}$ |

13.3 Power Supply Data

| Symbol | Parameter | Min. | Typ. | Max. | Units |
|-----------------------|---|------|------|------|-------|
| $V_{\text{XX}_{18}}$ | Analog and Digital 1.8 V Supply Voltage ($V_{\text{CC}_{18_CLK1}}$, $V_{\text{CC}_{18_CLK2}}$, $V_{\text{CC}_{18_IF}}$, $V_{\text{DD}_{18}}$, $V_{\text{DD}_{18_CONV}}$, $V_{\text{DD}_{18_ADC}}$) | 1.70 | 1.80 | 1.90 | V |
| $V_{\text{XX}_{33}}$ | Analog and Digital 3.3 V Supply Voltage ($V_{\text{CC}_{33_SC}}$, $V_{\text{CC}_{33_LS}}$, $V_{\text{DD}_{33_IO1}}$, $V_{\text{DD}_{33_IO2}}$, $V_{\text{DD}_{33_CONV}}$, $V_{\text{CC}_{NISO}}$) | 3.13 | 3.30 | 3.47 | V |
| HV_{CC} | Analog Supply High Voltage (V_{CC_H}) | 7.6 | 8.0 | 8.4 | V |
| $I_{\text{VDD}_{18}}$ | Current Consumption for Digital 1.8 V Supply ($V_{\text{CC}_{18_CLK2}}$, $V_{\text{DD}_{18}}$, $V_{\text{DD}_{18_CONV}}$, $V_{\text{DD}_{18_ADC}}$) | | 210 | | mA |
| $I_{\text{VDD}_{33}}$ | Current Consumption for Digital 3.3 V Supply ($V_{\text{DD}_{33_IO1}}$, $V_{\text{DD}_{33_IO2}}$) | | 10 | | mA |
| $I_{\text{VCC}_{18}}$ | Current Consumption for Analog 1.8 V Supply ($V_{\text{CC}_{18_CLK1}}$, $V_{\text{CC}_{18_IF}}$) | | 50 | | mA |
| $I_{\text{VCC}_{33}}$ | Current Consumption for Analog 3.3 V Supply ($V_{\text{CC}_{33_SC}}$, $V_{\text{CC}_{33_LS}}$, $V_{\text{DD}_{33_CONV}}$, $V_{\text{CC}_{NISO}}$) | | 65 | | mA |
| I_{VCC_H} | Current Consumption for Analog Supply High Voltage (8 V) | | 4 | | mA |
| P_{DTOT} | Total Power Dissipation | | 750 | | mW |

13.4 Crystal Oscillator

| Symbol | Parameter | Min. | Typ. | Max. | Units |
|----------|--|------|------|------|----------|
| f_P | Crystal Series Resonance Frequency (at $C_{21} = C_{22} = 27$ pF load capacitor) | | 27 | | MHz |
| DF/F_P | Frequency Tolerance at 25 °C | -30 | | +30 | ppm |
| DF/F_T | Frequency Stability versus Temperature within a range from 0 to 70 °C | -30 | | +30 | ppm |
| C_1 | Motional Capacitor | | | 15 | fF |
| R_S | Serial Resistance | | | 30 | Ω |
| C_S | Shunt Capacitance | | | 7 | pF |

13.5 Analog Sound IF Signal

| Symbol | Parameter | Test Conditions | Min. | Typ. | Max. | Units |
|--------------|------------------------|--|------|------|------|------------|
| $BAND_{SIF}$ | SIF Frequency Flatness | AGC_ERR at 0, frequency range from 4 to 7MHz | | 0.6 | 3 | dB |
| R_{INSIF} | SIF Input Resistance | | 60 | 72 | 85 | k Ω |
| DC_{INSIF} | SIF Input DC Level | | | 0.9 | | V |
| C_{INSIF} | SIF Input Capacitance | | | 3 | | pF |

FM Carrier

| | | | | | | | |
|---------------|--|---|---|----------|-----------|--------------|-----|
| $VSIF_{FM}$ | SIF Input Sensitivity | SNR 40dB RMS unweighted, 20Hz-15kHz, Standard B/G 27 kHz FM Deviation, 1kHz | 350 | | | μV_{PP} | |
| DEV_{FM} | FM Maximum Deviation | FM50k (Standard) | Signal Lost, DK mode, FM prescale at 0 | ± 15 | ± 50 | ± 115 | kHz |
| | | FM200k | | | ± 200 | ± 320 | |
| | | FM350k | | | ± 350 | ± 560 | |
| | | FM500k | | | ± 500 | ± 700 | |
| $DFSIF_{FM}$ | SIF Carrier Accuracy for FM | Standard (FM50k) | | ± 1 | ± 5 | kHz | |
| | | Shifted Standard (FM50k with DCO compensation) | | | ± 120 | kHz | |
| $R_{FM/QPSK}$ | Carrier Ratio FM/QPSK for NICAM System | NICAM mute, FAR_MODE is active, standard BG, 100mV _{PP} level for FM carrier | | | 40 | dB | |

AM Carrier

| | | | | | | |
|---------------------|-------------------------|---|----|--|-----|------------------|
| $VSIF_{AM}$ | SIF Input Sensitivity | Unmodulated, -3 dB at output amplitude AGC_ERR at 21d Standard L, 54% AM Depth, 1 kHz | 19 | | | mV _{PP} |
| $V_{MAX_SIF_{AM}}$ | SIF Maximum Input Level | Unmodulated, THD at 1%, 54% AM Depth, AGC_ERR at 0 | | | 1.3 | V _{PP} |
| DEV_{AM} | Modulation Depth for AM | THD at 1% | 0 | | 100 | % |

| Symbol | Parameter | Test Conditions | Min. | Typ. | Max. | Units |
|----------------------|--|--|------|------|------|-------|
| DFSIF _{AM} | SIF Carrier Accuracy for AM | | | ±1 | ±5 | kHz |
| R _{AM/QPSK} | AM/QPSK Carrier Ratio for NICAM System | NICAM Mute, 100mV _{PP} AM carrier | | | 36 | dB |
| AGC | | | | | | |
| AGC _{step} | IF AGC Step | | 1.4 | 1.5 | 1.6 | dB |
| AGC _{dyn} | Relative maximum gain to step 0 | Valid from step 21 to step 31 | 29 | 30 | 31 | dB |

13.6 SIF to I²S Output Path Characteristics

Test Conditions: SIF amplitude = 100mV_{pp}, otherwise specified, I²S output.

www.DataSheet4U.com

| Symbol | Parameter | Test Conditions | Min. | Typ. | Max. | Units |
|---------------------------|---------------------------|---|------|------|------|-------|
| FM Demodulation | | | | | | |
| BAND _{FM} | Frequency Response | 20Hz - 15kHz | | | ±0.7 | dB |
| SNR _{FM} | Signal to Noise | RMS unweighted, 20Hz-15kHz, Standard B/G 27 kHz FM Deviation, 1kHz | 66 | | | dB |
| THD _{FM} | Total Harmonic Distortion | | | | 0.05 | % |
| SEP _{FM} | Stereo Channel Separation | Standard B/G stereo A2, 27 kHz FM deviation, 1 kHz | 48 | | | dB |
| NICAM Demodulation | | | | | | |
| BAND _{NIC} | Frequency Response | 20Hz - 15kHz | | | ±0.2 | dB |
| SNR _{NIC} | Signal to Noise | 200Hz - 60dBFS, trap filter 200 Hz RMS unweighted, 20Hz-15kHz, Standard B/G mono NICAM, 1 kHz | 74 | | | dB |
| THD _{NIC} | Total Harmonic Distortion | | | | 0.04 | % |
| AM Demodulation | | | | | | |
| BAND _{AM} | Frequency Response | 20 Hz - 15 kHz | | | ±0.5 | dB |
| SNR _{AM} | Signal to Noise | RMS unweighted 2 0Hz-15 kHz, Standard L, 54% AM Depth, 1 kHz AGC: 13d | 60 | | | dB |
| THD _{AM} | Total Harmonic Distortion | | | | 0.4 | % |

13.7 SCART to SCART Analog Path Characteristics

Test Conditions: R_{load}_{MAX} = 10kΩ, C_{load}_{MAX} = 330pF, MONO_IN voltage = 0.5 V_{RMS}

| Symbol | Parameter | Test Conditions | Min. | Typ. | Max. | Units |
|---|------------------------------|-----------------|------|------|------|-------|
| Analog-to-Analog STEREO and MONO | | | | | | |
| R _{INSCART} | SCART Input Resistance | | 29 | 34 | 39 | kΩ |
| R _{OUTSCART} | Output Resistance for SCARTs | | | 40 | 75 | Ω |
| VDC _{INSCART} | SCART Input DC Level | | | 1.57 | | V |
| VDC _{OUTSCART} | SCART Output DC Level | | | 3.64 | | V |

| Symbol | Parameter | | Test Conditions | Min. | Typ. | Max. | Units |
|-----------------------|---|---|---|------|------|------|------------------|
| CLIP _{SCART} | Clipping SCART | Clipping input level from SCART input | At 1 kHz 1% THD | 2.0 | | | V _{RMS} |
| | | Clipping input level from MONO_IN input | | 0.5 | | | V _{RMS} |
| THD _{SCART} | THD SCART | THD from SCART input | 1 V _{RMS} , at 1 KHz | | 0.02 | 0.05 | % |
| | | THD from MONO_IN input | 0.25 V _{RMS} , at 1 KHz | | 0.02 | 0.05 | % |
| SNR _{SCART} | Signal to Noise Ratio | SCART input | 1 V _{RMS} , 20 Hz to 20 kHz Bandwidth, RMS unweighted | | 82 | | dB |
| | | MONO_IN input | 0.25 V _{RMS} , 20 Hz to 20 kHz Bandwidth, RMS unweighted | | 76 | | dB |
| BAND _{SCART} | Frequency Flatness | SCART input | 20 Hz to 20 kHz | -0.5 | | 0.5 | dB |
| | | MONO_IN input | 20 Hz to 20 kHz | 11.5 | 12 | 12.5 | dB |
| XTALK _{L/R} | Left/Right Crosstalk | | 1 V _{RMS} @ 1 kHz on ref signal, the other one grounded | 80 | 90 | | dB |
| XTALK _{IN} | Audio Crosstalk from Input Channel <i>n</i> to Input Channel <i>m</i> | | 1 V _{RMS} @ 1 kHz on ref signal, all other inputs grounded | 80 | 90 | | dB |
| XTALK _{OUT} | Audio Crosstalk from Output Channel <i>n</i> to Output Channel <i>m</i> | | 1 V _{RMS} @ 1 kHz on reference output, signal on a single input, all other inputs grounded | 80 | 90 | | dB |

13.8 SCART and MONO IN to I²S Path Characteristics

Test Conditions: Sampling Frequency = 32KHz, Maximum MONO_IN voltage = 0.5 V_{RMS}.

| Symbol | Parameter | | Test Conditions | Min. | Typ. | Max. | Units |
|----------------------|-----------------------|------------------------|---|------|-------|------|-------|
| THD _{ADC} | THD ADC | THD from SCART input | V _{IN} = 2 V _{RMS} at 1 KHz | | 0.006 | 0.05 | % |
| | | THD from MONO_IN input | V _{IN} = 0.5 V _{RMS} at 1 KHz | | 0.006 | 0.05 | % |
| SNR _{ADC} | Signal to Noise Ratio | | 20 to 15 kHz Bandwidth, RMS unweighted V _{IN} = 200 mV _{RMS} SCART input | 62 | | | dB |
| BAND _{ADC} | Frequency Flatness | | 20 Hz to 15 kHz | | | ±0.5 | dB |
| XTALK _{ADC} | Left Right Crosstalk | | at 1 KHz, V _{IN} = 1 V _{RMS} | 95 | | | dB |

13.9 I²S to LS/HP/SUB/C Path Characteristics

Test Conditions: Sampling Frequency = 32KHz, L_{LOAD} = 100 μH, C_{LOAD} = 33nF, R_{LOAD} = 30KΩ

| Symbol | Parameter | | Test Conditions | Min. | Typ. | Max. | Units |
|-----------------------|------------------------------------|--|--|------|------|------|-------|
| R _{OUTDAC} | Output Resistance for Main Outputs | | LS_L, LS_R, LS_SUB, LS_C, HP_LSS_R and HP_LSS_L pins | | 90 | 140 | Ω |
| VDC _{OUTDAC} | MAIN Output DC Level | | | | 1.54 | | V |

| Symbol | Parameter | Test Conditions | Min. | Typ. | Max. | Units |
|------------------------|---------------------------|---|------|------|------|-------------------|
| THD _{DAC} | Total Harmonic Distortion | 90% Full-scale Range at 1 kHz | | | 0.06 | % |
| SNR _{DAC} | Signal to Noise Ratio | 20 to 15 kHz Bandwidth, RMS unweighted, at -20dB full range | 75 | | | dB |
| V _{OUTAMPDAC} | MAIN Output Amplitude | 100% Full-scale Range at 1 kHz | | 900 | | mV _{RMS} |
| XTALK _{DAC} | Left Right Crosstalk | at 1 KHz, -20dBFS | 87 | | | dB |

13.10 I²S to SCART Path Characteristics

Test Conditions: Sampling Frequency = 32KHz, C_{LOAD} = 33nF on DAC SCART pins, DAC SCART prescale at -5.5dB.

| Symbol | Parameter | Test Conditions | Min. | Typ. | Max. | Units |
|---------------------------|---------------------------|--|------|------|------|------------------|
| THD _{DACSCART} | Total Harmonic Distortion | 90% Full-scale Range at 1 kHz | | 0.08 | 0.12 | % |
| SNR _{DACSCART} | Signal to Noise Ratio | 20 Hz to 15 kHz Bandwidth unweighted, -20dB Full Range | 73 | | | dB |
| V _{ODACSCART} | MAIN Output Amplitude | 100% Full-scale Range at 1 kHz | | 2 | | V _{RMS} |
| XTALK _{DACSCART} | Left Right Crosstalk | at 1 KHz, -20 dBFS | 80 | | | dB |

13.11 MUTE Characteristics

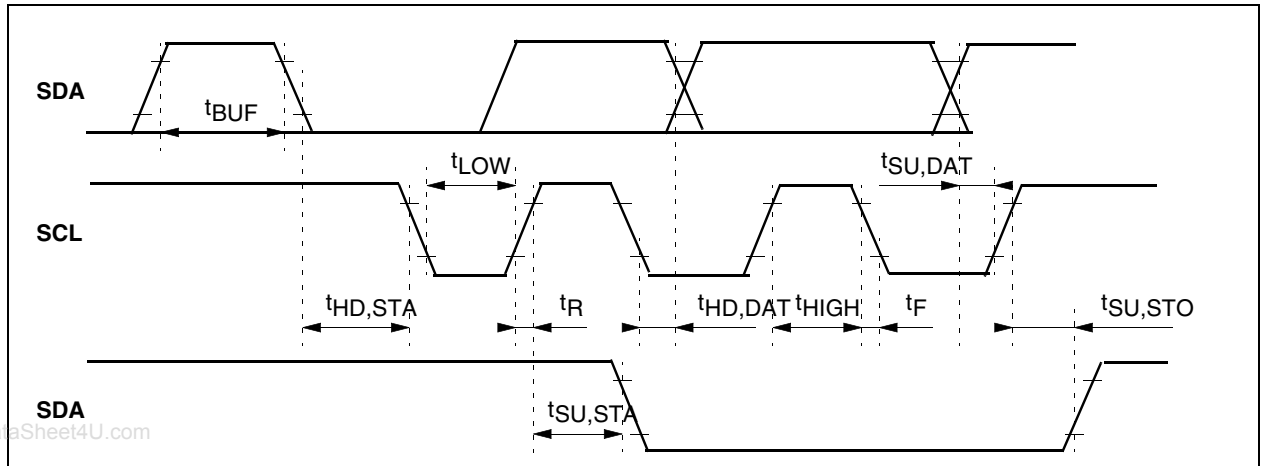
| Symbol | Parameter | Test Conditions | Min. | Typ. | Max. | Units |
|-----------------------|-----------------|---|------|------|------|-------|
| MUTE _{DAC} | DAC Mute analog | I ² S to DAC at 1 kHz | 90 | | | dB |
| MUTE _{SCART} | SCART Mute | 2 V _{RMS} @ 1 kHz on ref signal, all other inputs grounded | 81 | | | dB |

13.12 Digital I/Os Characteristics

| Symbol | Parameter | Test Conditions | Min. | Typ. | Max. | Units |
|------------------------|----------------------------------|--|------|------|------|-------|
| V _{IL} | Low Level Input Voltage | except SDA, SCL and CLK_SEL, 3.3V power supply | | | 0.5 | V |
| V _{IH} | High Level Input Voltage | except SDA, SCL and CLK_SEL, 3.3V power supply | 2.0 | | | V |
| I _{IN} | Input Current | | | | 1 | μA |
| V _{ILCLK_SEL} | CLK_SEL Low Level Input Voltage | 1.8V power supply | | | 0.3 | V |
| V _{IHCLK_SEL} | CLK_SEL High Level Input Voltage | 1.8V power supply | 1.2 | | | V |
| V _{OL} | Low Level Output Voltage | S/PDIF_OUT, IRQ, BUS_EXP | | | 0.3 | V |
| V _{OH} | High Level Output Voltage | S/PDIF_OUT, IRQ, BUS_EXP | 3.0 | | | V |

13.13 I²C Bus Characteristics

| Symbol | Parameter | Test Conditions | Min. | Typ | Max. | Unit |
|------------------------------|--|------------------------------|------|-----|------|------|
| SCL | | | | | | |
| V _{IL} | Low Level Input Voltage | | -0.3 | | 1.5 | V |
| V _{IH} | High Level Input Voltage | | 2.3 | | 5.5 | V |
| I _{IL} | Input Leakage Current | V _{IN} = 0 to 5.0 V | -10 | | 10 | μA |
| f _{SCL} | Clock Frequency | | | | 400 | kHz |
| t _R | Input Rise Time | 1 V to 2 V | | | 300 | ns |
| t _F | Input Fall Time | 2 V to 1 V | | | 300 | ns |
| C _I | Input Capacitance | | | | 10 | pF |
| SDA | | | | | | |
| V _{IL} | Low Level Input Voltage | | -0.3 | | 1.5 | V |
| V _{IH} | High Level Input Voltage | | 2.3 | | 5.5 | V |
| I _{IL} | Input Leakage Current | V _{IN} = 0 to 5.0 V | -10 | | 10 | μA |
| t _R | Input Rise Time | 1 V to 2 V | | | 300 | ns |
| t _F | Input Fall Time | 2 V to 1 V | | | 300 | ns |
| V _{OL} | Low Level Output Voltage | I _{OL} = 3 mA | | | 0.4 | V |
| t _F | Output Fall Time | 2 V to 1 V | | | 250 | ns |
| C _L | Load Capacitance | | | | 400 | pF |
| C _I | Input Capacitance | | | | 10 | pF |
| I²C Timing | | | | | | |
| t _{LOW} | Clock Low period | | 1.3 | | | μs |
| t _{HIGH} | Clock High period | | 0.6 | | | μs |
| t _{SU,DAT} | Data Set-up Time | | 100 | | | ns |
| t _{HD,DAT} | Data Hold Time | | 0 | | 900 | ns |
| t _{SU,STO} | Set-up Time from Clock High to Stop | | 0.6 | | | μs |
| t _{BUF} | Start Set-up Time following a Stop | | 1.3 | | | μs |
| t _{HD,STA} | Start Hold Time | | 0.6 | | | μs |
| t _{SU,STA} | Start Set-up Time following Clock Low to High Transition | | 0.6 | | | μs |

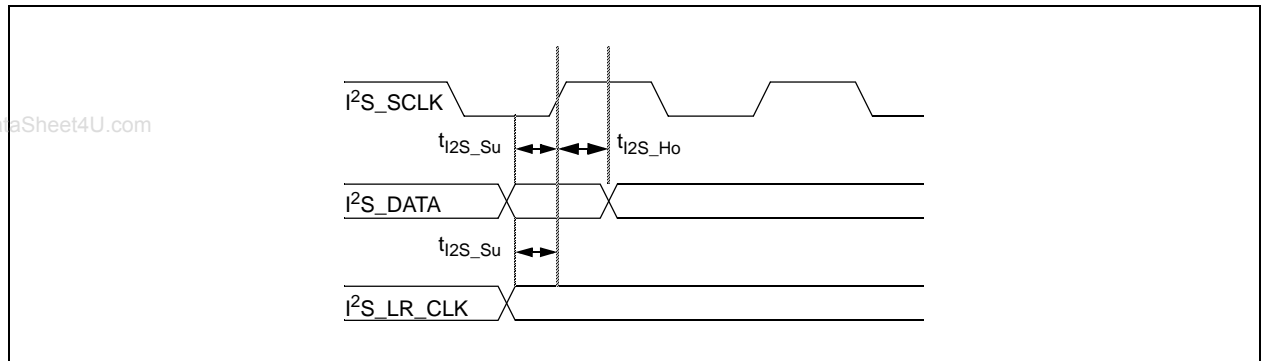
Figure 28: I²C Bus Timing

13.14 I²S Bus Interface

See timing for I²S on page 41.

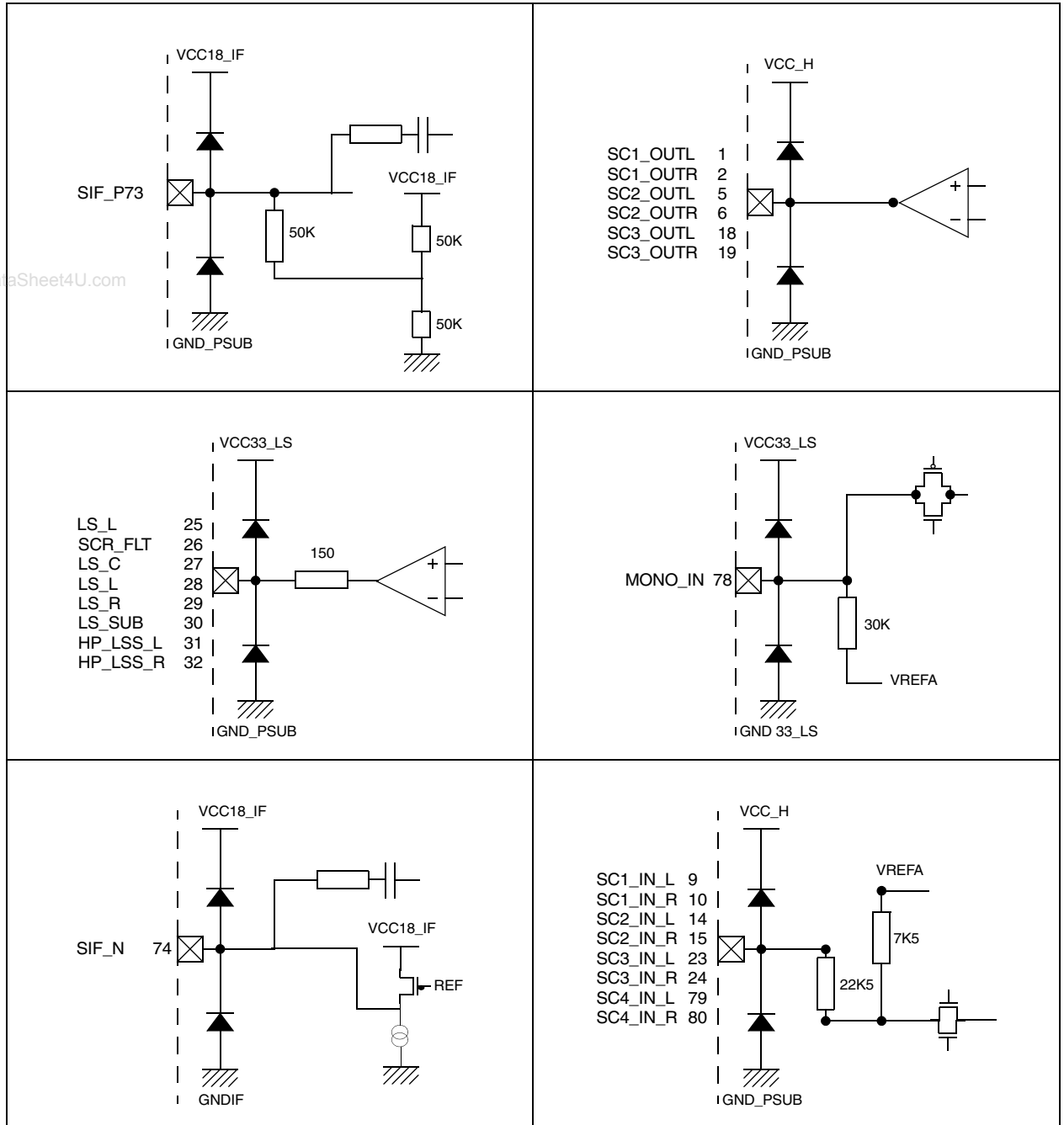
| Symbol | Parameter | Test Conditions | Min. | Typ | Max. | Unit |
|--|--|----------------------|-------|-----|-------|---------|
| I²S Input | | | | | | |
| V_{I2S_IL} | Input I ² S Low Level Voltage | | | | 0.8 | V |
| V_{I2S_IH} | Input I ² S High Level Voltage | | 2 | | | V |
| Z_{I2S} | Input I ² S Impedance | | | | 5 | pF |
| I_{I2S_Leak} | I ² S Leakage Current | | -1 | | 1 | μ A |
| t_{I2S_Su} | I ² S Input Setup Time before Rising Edge of Clock | See Figure 29 | 30 | | | ns |
| t_{I2S_Ho} | I ² S Input Hold Time after Rising Edge of Clock | See Figure 29 | 100 | | | ns |
| f_{I2S_LR0} | I ² S Left Right Strobe Input Frequency (I ² S_DATA0 only) | deviation =+/-250ppm | 8 | | 48 | KHz |
| f_{I2S_SCL0} | I ² S Serial Clock Input Frequency (I ² S_DATA0 only) | | 0.512 | | 3.072 | MHz |
| f_{I2S_LR} | I ² S Left Right Strobe Input Frequency (I ² S_DATA0,1,2) | deviation =+/-250ppm | 32 | | 48 | KHz |
| f_{I2S_SCL} | I ² S Serial Clock Input Frequency (I ² S_DATA0,1,2) | | 2.048 | | 3.072 | MHz |
| R_{I2S_SCL} | I ² S Serial Clock Input Ratio | | 0.9 | | 1.1 | |
| I²S Output (I²S_DATA0 only) | | | | | | |
| V_{I2SOL} | Output I ² S Low Level Voltage | IOL = 2 mA | | | 0.4 | V |
| V_{I2SOH} | Output I ² S High Level voltage | IOH = 2 mA | 2.4 | | | V |
| f_{I2S_OLR} | I ² S Left Right Strobe Output Frequency | deviation =+/-250ppm | 8 | | 48 | KHz |

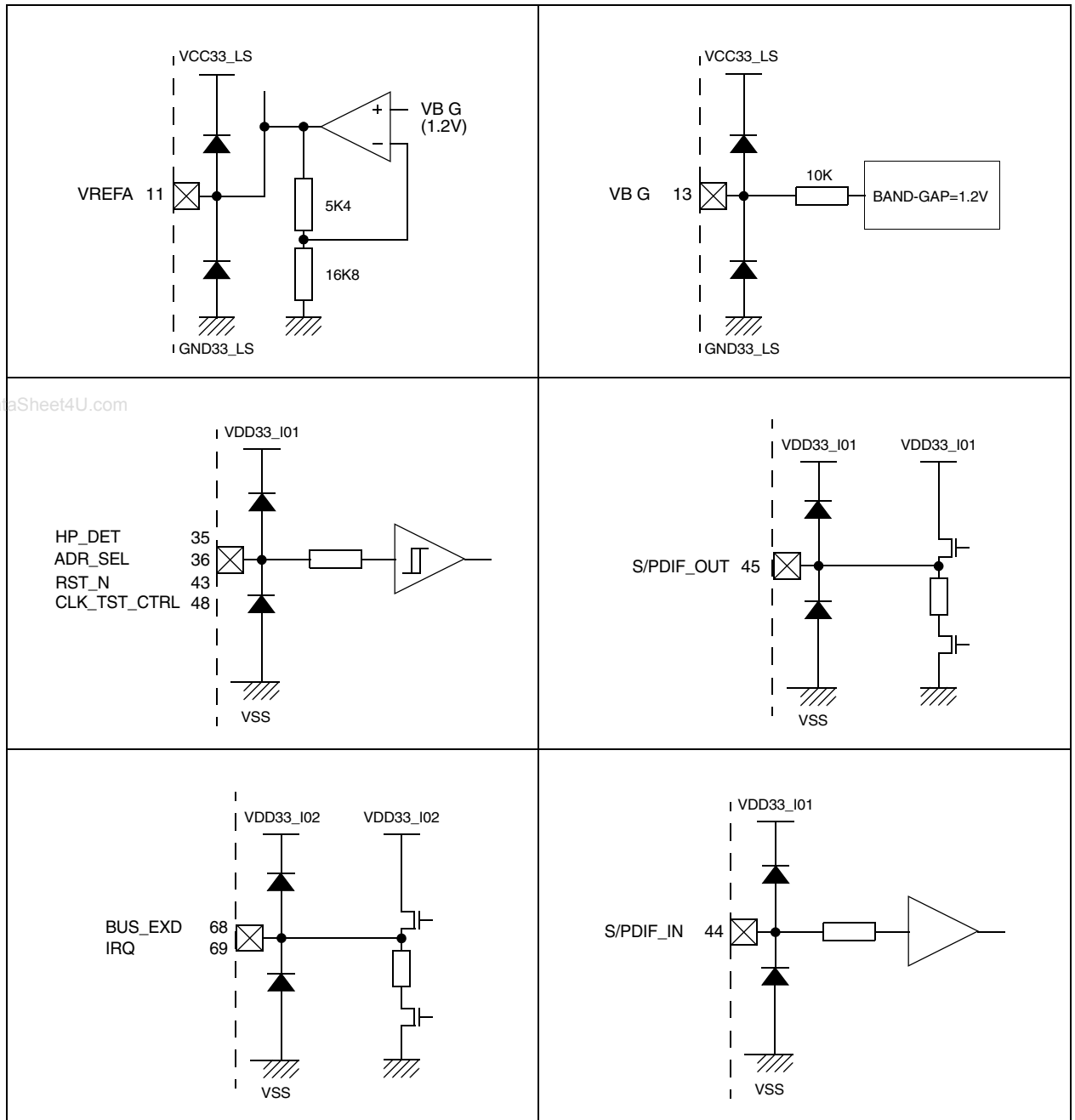
| Symbol | Parameter | Test Conditions | Min. | Typ | Max. | Unit |
|-----------------|---|------------------------|-------|-----|-------|------|
| f_{I2S_OSCI} | I ² S Serial Clock Output Frequency | | 0.512 | | 3.072 | MHz |
| R_{I2S_SCL} | I ² S Serial Clock Output Ratio | | 0.9 | | 1.1 | |
| t_{I2S_DeI} | I ² S Output Delay After Falling Edge of Clock | See Figure 29, CI=30pF | | | 30 | ns |

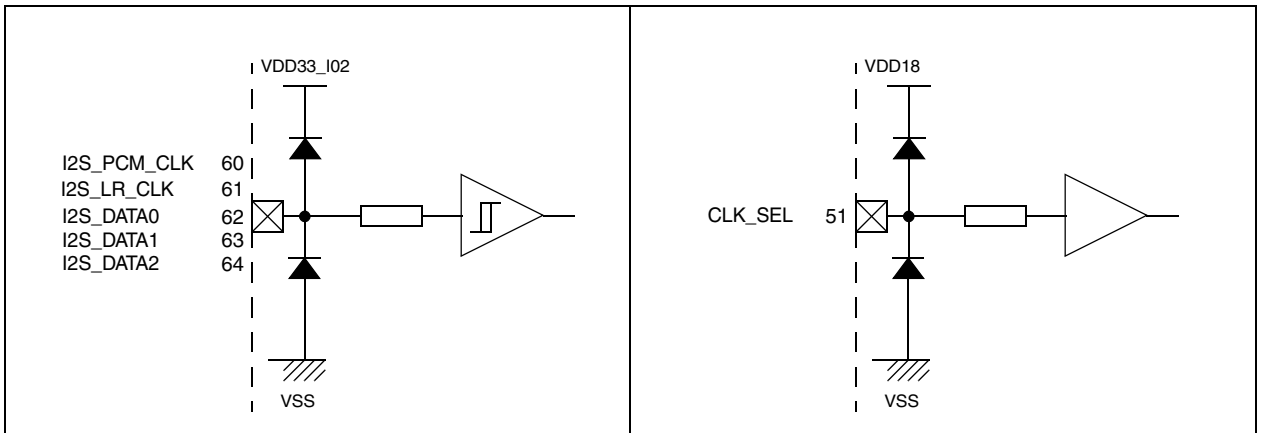
Figure 29: I²S Input Bus Timing

14 Input/Output Groups

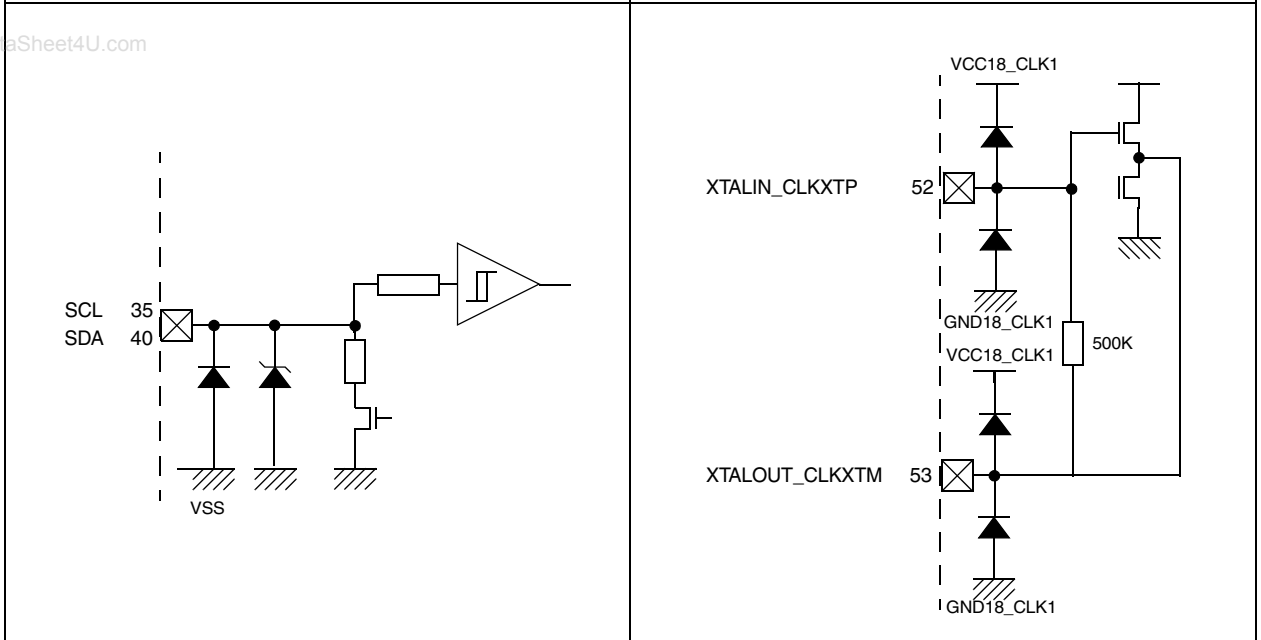
Pin numbers apply to SDIP package only.

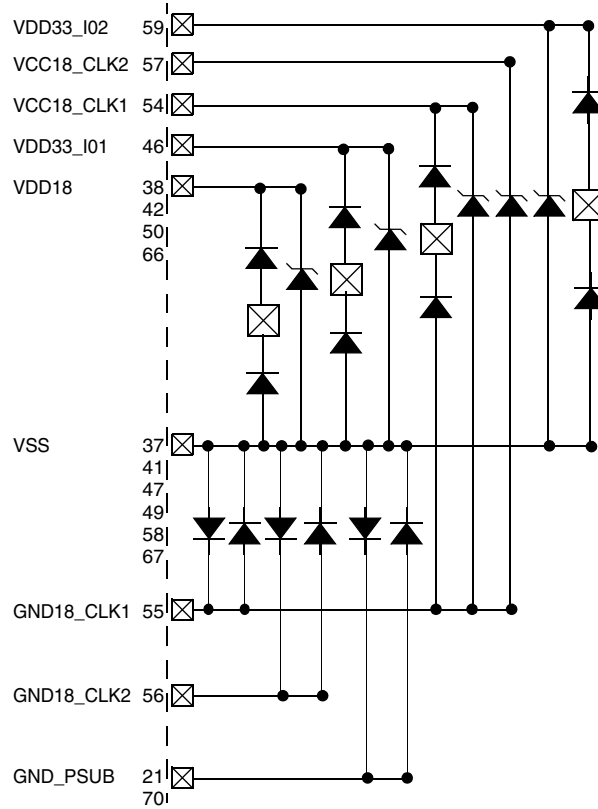




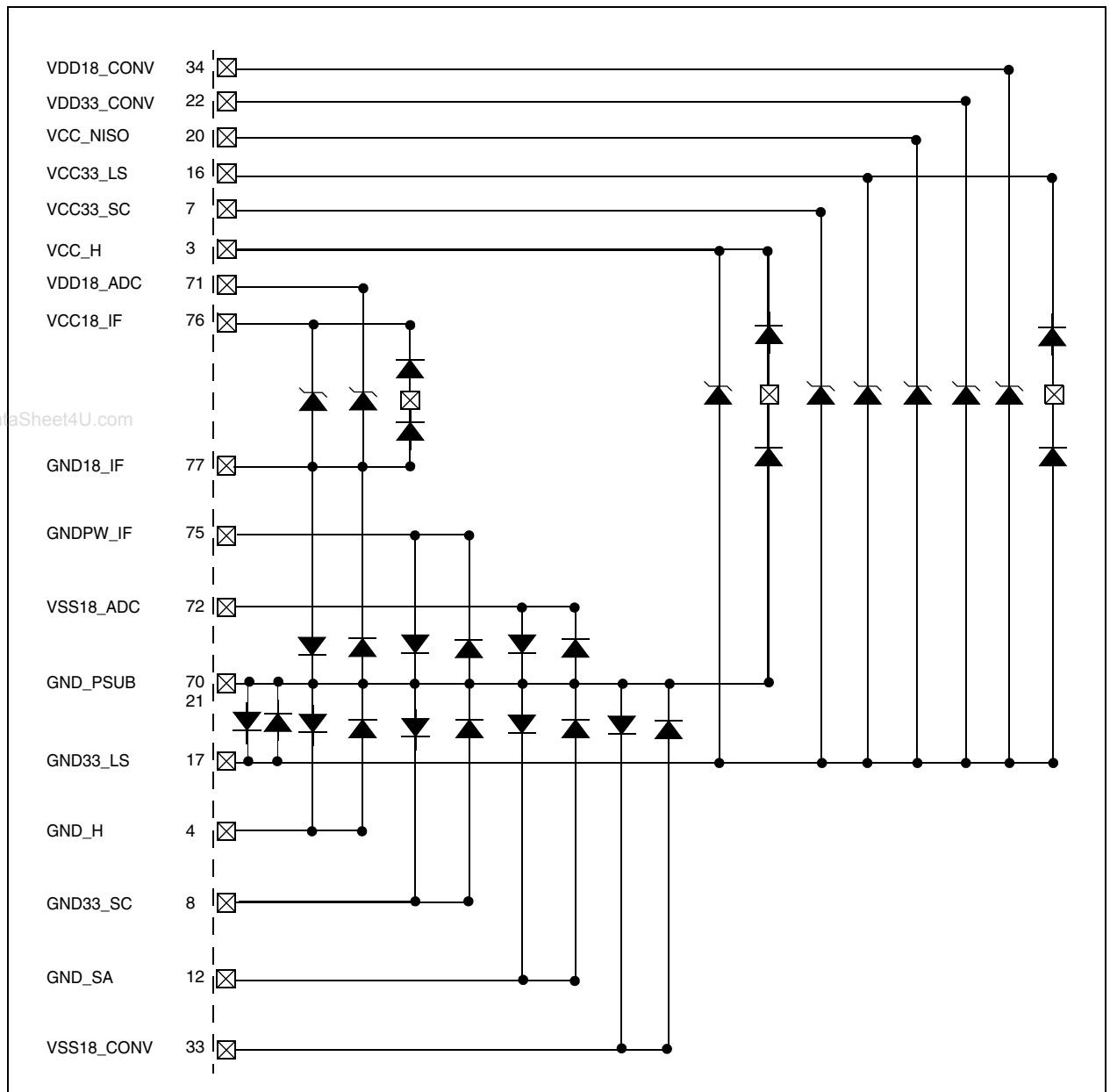


www.DataSheet4U.com





www.DataSheet4U.com



15 Package Mechanical Data

Figure 30: 80-Pin Thin Plastic Quad Flat Package

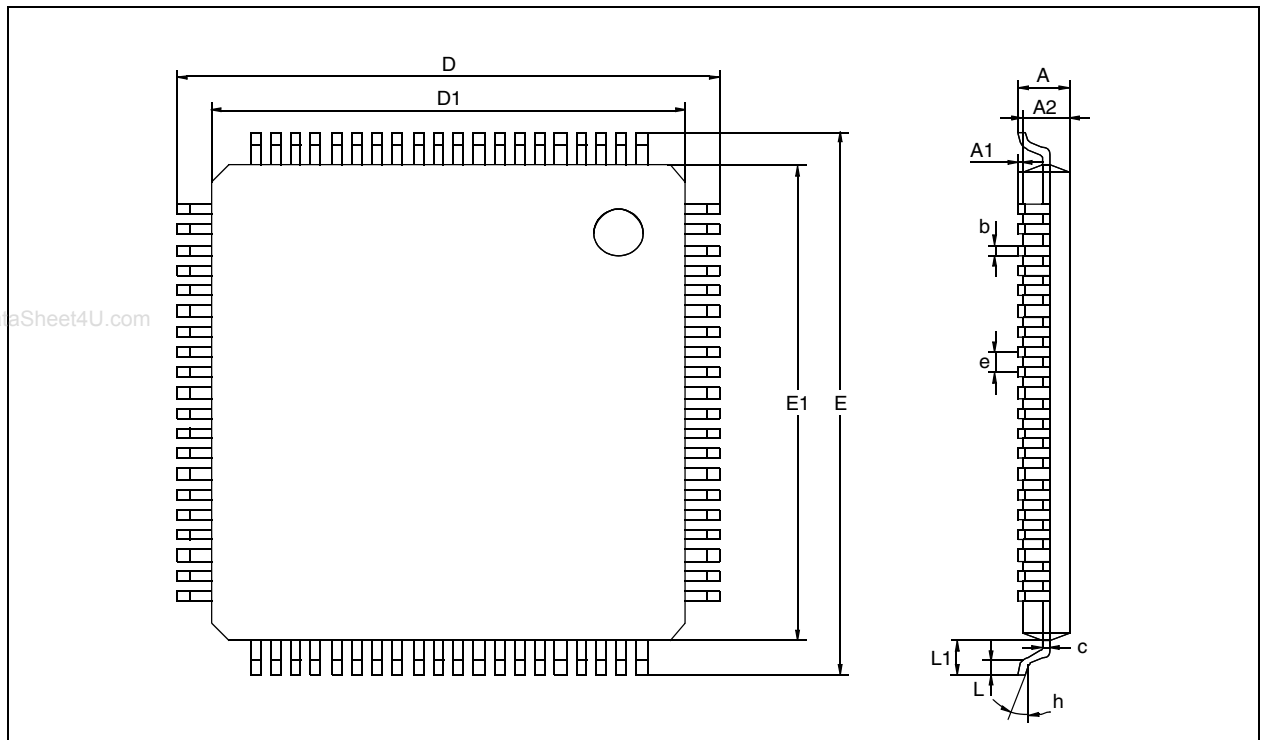


Table 31: Package Mechanical Dimensions

| Dim. | mm | | | inches | | |
|------|------|-------|-------|--------|-------|-------|
| | Min. | Typ. | Max. | Min. | Typ. | Max. |
| A | | | 1.60 | | | 0.063 |
| A1 | 0.05 | | 0.15 | 0.002 | | 0.006 |
| A2 | 1.35 | 1.40 | 1.45 | 0.053 | 0.055 | 0.057 |
| b | 0.22 | 0.32 | 0.38 | 0.009 | 0.013 | 0.015 |
| C | 0.09 | | 0.20 | 0.004 | | 0.008 |
| D | | 16.00 | | | 0.630 | |
| D1 | | 14.00 | | | 0.551 | |
| E | | 16.00 | | | 0.630 | |
| E1 | | 14.00 | | | 0.551 | |
| e | | 0.65 | | | 0.026 | |
| K | 0° | 3.5° | 0.75° | 0° | 3.5° | 0.75° |
| L | 0.45 | 0.60 | 0.75 | 0.018 | 0.024 | 0.030 |
| L1 | | 1.00 | | | 0.039 | |

16 Revision History

| Revision | Date | Modification |
|----------|---------------|---|
| 1.96 | April 2004 | Preliminary Datasheet - First Issue. |
| 1.97 | April 2004 | Updates to Chapter 13: Electrical Characteristics on page 132 . |
| 1.98 | April 2004 | Added Figure 8: STV82x6/STV82x7 Compatible Application Electrical Diagram on page 18 . Added Section 11.2: Start-up and Configuration Change Procedure on page 47 . Update of Table 21: Demod Matrix on page 94 . Changes to function descriptions in Section 12.18: Volume on page 116 . Other minor corrections. |
| 1.99 | June 2004 | Updates to Table 3: TQFP80 Pin Description on page 14 , Section 13.5: Analog Sound IF Signal on page 133 , Section 13.9: I2S to LS/HP/SUB/C Path Characteristics on page 135 , Section 13.10: I2S to SCART Path Characteristics on page 136 and Section 13.12: Digital I/Os Characteristics on page 136 . |
| 2.0 | June 2004 | Updates to Table 7: RESET Default Values on page 45 , Table 12: Audio Processing for Loudspeakers, Headphone, SCART and S/PDIF outputs on page 27 , Table 19: Volume Control on page 36 , Table 27: Flow chart on page 47 and Section 12.1: I2C Register Map on page 49 . Added Register : SPDIF_CHANNEL_STATUS. Other minor corrections and modifications. |
| 2.01 | July 2004 | Added logos to page 1 . Added notes to Figure 3 , Figure 4 and Figure 5 . Removed "Pro Logic OFF Switch" from Table 12 , Table 13 , Table 14 and Table 16 . Other minor modifications and cosmetic changes. |
| 2.02 | July 2004 | Added ST Voice logo to page 1 . Modification to ST OmniSurround version in Table 1 . Modifications to text in Section 4.1: Back-end Processing on page 24 . Other minor modifications and cosmetic changes. |
| 2.03 | January 2005 | Update of bits I2S_OUT_SELECT[1:0] of ADC_CTRL register (56h). |
| 3 | February 2005 | Modified STSRND-STEREO on page 52 (removed shading), ADC-CTRL register I2S0_DATA0_CTRL field modification on page 74 and OFF added in PL2_C_WIDTH and PL2_DIMENSION on page 102. |

Index

A

| | |
|--|--------|
| Analog-to-Digital Conversion | 21 |
| Audio Matrix | |
| Analog | 39 |
| Automatic Frequency Control | 23 |
| Automatic Gain Control | 21 |
| Automatic Overmodulation Detection | 22 |
| Automatic Standard Recognition System | 22, 49 |

B

| | |
|---------------------------|----|
| Back-end Processing | 24 |
| Bass-Treble Control | 35 |
| Beeper | 37 |

C

| | |
|-----------------------|----|
| Clock Generator | 20 |
|-----------------------|----|

D

| | |
|----------------------------|----|
| Demodulation | 22 |
| Dolby | |
| Pro Logic II Decoder | 28 |

E

| | |
|---|-----|
| Electrical Characteristics | 132 |
| Absolute Maximum Ratings | 132 |
| Analog Sound IF Signal | 133 |
| Crystal Oscillator | 133 |
| Digital I/Os | 136 |
| I ² C Bus | 137 |
| I ² S to LS/HP/SW Path | 135 |
| I ² S to SCART Path | 136 |
| MUTE Performance | 136 |
| SCART to LS/HP/SW Path | 135 |
| SCART to SCART Analog Path | 134 |
| SIF to LS/HP/SCART Path | 134 |
| Supply Data | 132 |
| Thermal Data | 132 |
| Equalizer | |
| 5-Band Audio | 35 |

I

| | |
|----------------------------------|-----|
| I ² C Address | 46 |
| I ² C Protocol | 46 |
| I ² S Interface | 40 |
| I ² C | 138 |
| I ² C Address | 46 |

L

| | |
|------------------|----|
| Loudness Control | |
| Automatic | 36 |

P

| | |
|-------------------------------|-----|
| Package Mechanical Data | 145 |
| Peak Detector | 22 |
| Power Supply Management | 43 |

R

| | |
|--|----------|
| Registers | |
| 5-Band Equalizer / Bass-Treble | 110, 112 |
| Analog Control | 74 |
| Audio Preprocessing and Selection | 85 |
| Audio Processing | 98 |
| Automatic Standard Recognition | 81 |
| AutoStandard Coefficients Settings | 130 |
| Beeper | 126 |
| Clocking 1 | 56 |
| Clocking 2 | 76 |
| DAC Control | 129 |
| Demodulator | 59 |
| Demodulator Channel 1 | 62 |
| Demodulator Channel 2 | 66 |
| DSP Control | 77 |
| General Control | 55 |
| Headphone Bass-Treble | 113 |
| Headphone Configuration | 128 |
| I ² C Map | 49 |
| Matrixing | 93 |
| Mute | 127 |
| NICAM | 71 |
| Stereo Mode | 73 |
| Volume | 116 |

S

| | |
|----------------------------|-----|
| SIF Signal | |
| Analog | 21 |
| Signal Processor | |
| Dedicated Digital | 24 |
| Signal to Noise | 134 |
| Smart Volume Control | 34 |
| Soft Mute Control | 37 |
| Software Information | 9 |
| SRS | |
| TruBass | 34 |
| TruSurround | 33 |
| WOW | 33 |
| SRS, | |
| TruSurround XT‰ | 33 |
| ST Dynamic Bass | 35 |
| ST OmniSurround | 28 |
| ST WideSurround | 28 |

T

| | |
|---------------------------------|-----|
| Total Harmonic Distortion | 134 |
|---------------------------------|-----|

V

| | |
|------------------------------|----|
| Volume/Balance Control | 36 |
|------------------------------|----|

Information furnished is believed to be accurate and reliable. However, STMicroelectronics assumes no responsibility for the consequences of use of such information nor for any infringement of patents or other rights of third parties which may result from its use. No license is granted by implication or otherwise under any patent or patent rights of STMicroelectronics. Specifications mentioned in this publication are subject to change without notice. This publication supersedes and replaces all information previously supplied. STMicroelectronics products are not authorized for use as critical components in life support devices or systems without express written approval of STMicroelectronics.

The ST logo is a registered trademark of STMicroelectronics
All other names are the property of their respective owners

© 2005 STMicroelectronics - All rights reserved

STMicroelectronics GROUP OF COMPANIES

Australia - Belgium - Brazil - Canada - China - Czech Republic - Finland - France - Germany - Hong Kong - India - Israel - Italy
- Japan - Malaysia - Malta - Morocco - Singapore - Spain - Sweden - Switzerland - United Kingdom - United States

www.st.com