2A Bus Termination Regulator

Features

- Sourcing and Sinking Current up to 2A
- Wide Input Voltage Range: 1.2V to 3.6V
- VTT and VTTREF Voltage Tracks at Half the VREF Voltage
- VTT and VTTREF Voltage with ±10mV Accuracy
- Excellent Load Transient Response
- Stable with 10㎜F Ceramic Output Capacitor
- Current-Limit Protection
- Thermal Shutdown Protection
- Power-On-Reset Function on VCNTL
- S3, S5 Input Signals for ACPI States
- Small MSOP-10P and TDFN3x3-10 Packages
- Lead Free and Green Devices Available (RoHS Compliant)

General Description

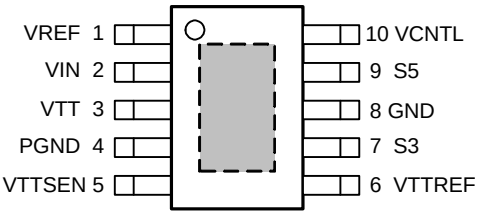
The APL5338 linear regulator is designed to provide a regulated voltage with bi-directional output current for DDR-SDRAM termination. The APL5338 integrates two power transistors to source or sink current up to 2A. It also incorporates current-limit and thermal shutdown into a single chip.

The output voltage of APL5338 tracks the voltage at VREF pin. An internal resistor divider is used to provide a half voltage of VREF for VTTREF and VTT Voltage. The VTT output voltage is only requiring 10µF of ceramic output capacitance for stability and fast transient response. The S3 and S5 pins provide the sleep state for VTT (S3 state) and suspend state (S4/S5 state) for device when S5 and S3 are both pulled low the device provides the soft-off for VTT and VTTREF. The MSOP-10P and TDFN3x3-10 package with a copper pad is available which provides excellent thermal impedance.

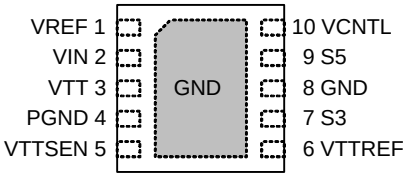
Applications

- DDR 2/3 Memory Termination

Pin Configuration



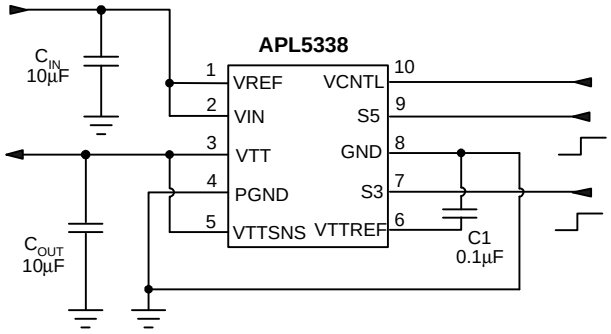
MSOP-10P (Top View)



TDFN3X3-10 (Top View)

= Exposed Pad
(connected to ground plane for better heat dissipation)

Simplified Application Circuit



Ordering and Marking Information

APL5338 □□□-□□□

- Assembly Material
- Handling Code
- Temperature Range
- Package Code

Package Code
XA : MSOP-10P QB : TDFN3x3-10
Operating Ambient Temperature Range
I : -40 to 85 °C
Handling Code
TR : Tape & Reel
Assembly Material
G : Halogen and Lead Free Device

APL5338 XA :	L5338 XXX ● XX	XXXXX - Date Code
APL5338 QB :	APL 5338 ● XXXXX	XXXXX - Date Code

Note : ANPEC lead-free products contain molding compounds/die attach materials and 100% matte tin plate termination finish; which are fully compliant with RoHS. ANPEC lead-free products meet or exceed the lead-free requirements of IPC/JEDEC J-STD-020D for MSL classification at lead-free peak reflow temperature. ANPEC defines "Green" to mean lead-free (RoHS compliant) and halogen free (Br or Cl does not exceed 900ppm by weight in homogeneous material and total of Br and Cl does not exceed 1500ppm by weight).

Absolute Maximum Ratings (Note 1)

Symbol	Parameter	Rating	Unit
V_{CNTL}	VCNTL Supply Voltage (VCNTL to GND)	-0.3 ~ 7	V
V_{IN}	VIN Supply Voltage (VIN to GND)	-0.3 ~ 7	V
V_{TT}	VTT Output Voltage (VTT to GND)	-0.3 ~ 7	V
V_{TTREF}	VTTREF Output Voltage (VTTREF to GND)	-0.3 ~ 7	V
	VTTSNS, VREF, S3 and S5 Voltage	-0.3 ~ 7	V
	PGND to GND Voltage	-0.3 ~ 0.3	V
P_D	Power Dissipation	Internally Limited	W
T_J	Maximum Junction Temperature	150	°C
T_{STG}	Storage Temperature Range	-65 ~ 150	°C
T_{SDR}	Maximum Lead Soldering Temperature, 10 Seconds	260	°C

Note1: Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Thermal Characteristics

Symbol	Parameter	Typical Value	Unit
θ_{JA}	Junction-to-Ambient Resistance in Free Air (Note 2) MSOP-10P TDFN3x3-10	60	°C/W

Note 2 : θ_{JA} is measured with the component mounted on a high effective thermal conductivity test board in free air. The exposed pad of MSOP-10P and TDFN3x3-10 is soldered directly on the PCB.

Recommended Operating Conditions (Note 3)

Symbol	Parameter	Range	Unit
V_{CNTL}	VCNTL to GND	4.5 ~ 5.5	V
V_{IN}	VIN to GND	1.2 ~ 3.6	V
V_{REF}	VREF to GND	1.2 ~ 3.6	V
V_{S3}, V_{S5}	S3, S5 to GND	0 ~ 5.5	V
I_{VTT}	VTT Output Current (Note 4)	-2 ~ +2	A
C_{IN}	VIN Input Capacitor	10 ~ 100	µF
C_{OUT}	Capacitance of VTT Output Multi-layer Ceramic Capacitor (MLCC)	10 ~ 47	µF
T_A	Ambient Temperature	-40 ~ 85	°C
T_J	Junction Temperature	-40 ~ 125	°C

Note 3 : Refer to the typical application circuit.

Note 4 : If the VTT output current is "+2A", then VTT source would be 2A current, and vice versa.

Electrical Characteristics

Unless otherwise specified, these specifications apply over V_{CNTL}=5V, V_{IN}=V_{REF}=1.8V, C_{IN}=10µF, C_{OUT}=10µF and T_A= -40 ~ 85 °C. Typical values are at T_A=25°C.

Symbol	Parameter	Test Conditions	APL5338			Unit
			Min.	Typ.	Max.	
SUPPLY CURRENT						
I_{VCNTL}	VCNTL Supply Current	T_J = 25°C, V_{CNTL}=5V, V_{S3}=V_{S5}=5V, no load	0.2	0.5	1	mA
	VCNTL Standby Current	T_J = 25°C, V_{CNTL}=5V, V_{S3}=0V, V_{S5}=5V, no load	20	50	80	µA
	VCNTL Shutdown Current	T_J = 25°C, V_{CNTL}=5V, V_{S3}=V_{S5}=0V, no load, V_{IN}=V_{REF}=0V	-	0.3	1.0	
V_{IN}	VIN Supply Current	T_J = 25°C, V_{CNTL}=5V, V_{S3}=V_{S5}=5V, no load	0.3	0.6	1.0	mA
	VIN Standby Current	T_J = 25°C, V_{CNTL}=5V, V_{S3}=0V, V_{S5}=5V, no load	-	5	10	µA
	VIN Shutdown Current	T_J = 25°C, V_{CNTL}=5V, V_{S3}=V_{S5}=0V, no load, V_{IN}=V_{REF}=0V	-	0.5	1.0	
INPUT IMPEDANCE						
I_{VREF}	VREF Input Impedance	V_{CNTL}=5V, V_{S3}=V_{S5}=5V	1	3	5	µA
I_{VTTSNS}	VTTSNS Input Current	V_{CNTL}=5V, V_{S3}=V_{S5}=5V	-	10	-	nA
POWER-ON-RESET (POR) AND LOCKOUT VOLTAGE THRESHOLDS						
	VCNTL POR Voltage Threshold	V_{CNTL} rising	3.6	3.8	4.0	V
	VCNTL POR Hysteresis		-	0.2	-	
VTT OUTPUT						
	VTT Output Voltage	V_{IN}=V_{REF}=3.15V	-	1.575	-	V
		V_{IN}=V_{REF}=1.8V	-	0.9	-	
		V_{IN}=V_{REF}=1.5V	-	0.75	-	
		V_{IN}=V_{REF}=1.35V	-	0.675	-	

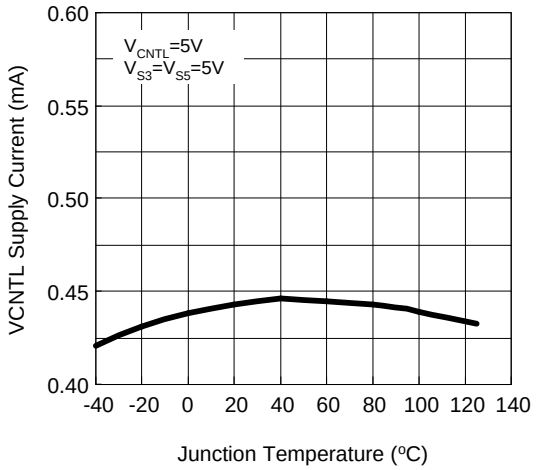
Electrical Characteristics (Cont.)

Unless otherwise specified, these specifications apply over V_{CNTL}=5V, V_{IN}=V_{REF}=1.8V, C_{IN}=10µF, C_{OUT}=10µF and T_A= -40 ~ 85 °C. Typical values are at T_A=25°C.

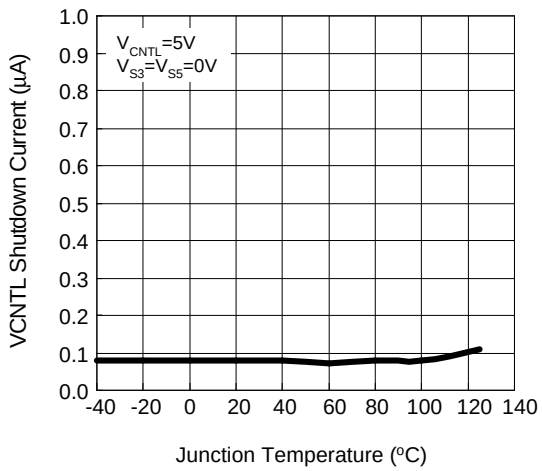
Symbol	Parameter	Test Conditions	APL5338			Unit
			Min.	Typ.	Max.	
VTT OUTPUT (Cont.)						
	VTT Output Accuracy to VTTREF	V_{IN}=V_{REF}=1.35V/1.5V/1.8V/3.15V, over temperature and load current range	-10	-	10	mV
I_{LIM}	VTT Current Limit	Sourcing Current	2.8	3.0	3.5	A
		Sinking Current	-2.8	-3.0	-3.5	
	VTT Leakage Current	V_{TT}=0.9V, V_{S3}=0V, V_{S5}=5V, T_J =25 °C	-	2.5	4.0	µA
	VTTSNS Leakage Current	V_{TT}=0.9V, T_J =25 °C	-1.0	-	1.0	
	VTT Discharge Current	V_{TT}=0.5V, V_{S3}=V_{S5}=0V, T_J =25 °C, V_{REF}=0V	15	25	35	mA
VTTREF OUTPUT						
V_{TTREF}	VTTREF Output Voltage	V_{IN}=V_{REF}=3.15V	-	1.575	-	V
		V_{IN}=V_{REF}=1.8V	-	0.9	-	
		V_{IN}=V_{REF}=1.5V	-	0.75	-	
		V_{IN}=V_{REF}=1.35V	-	0.675	-	
	VTTREF Output Voltage Tolerance to 0.5VREF	V_{IN}=V_{REF}, I_{VTTREF}<10mA	-10	-	+10	mV
I_{VTTREF}	VTTREF Source Current Limit	V_{TTREF}=0V	10	20	30	mA
$I_{VTTREFDIS}$	VTTREF Discharge Current	V_{TTREF}=0.5V, V_{S3}=V_{S5}=0V, T_J =25 °C	0.3	0.5	0.8	
LOGIC THRESHOLD						
V_{IH}	High Threshold Voltage	V_{S3}, V_{S5} Rising	1.6	-	-	V
V_{IL}	Low Threshold Voltage	V_{S3}, V_{S5} Falling	-	-	0.4	
	S3, S5 Hysteresis		-	0.2	-	
	Leakage Current	S3, S5, T_J =25 °C	-	-	4	µA
THERMAL SHUTDOWN						
T_{SD}	Thermal Shutdown Temperature	T_J Rising	-	150	-	°C
	Thermal Shutdown Hysteresis		-	30	-	

Typical Operating Characteristics

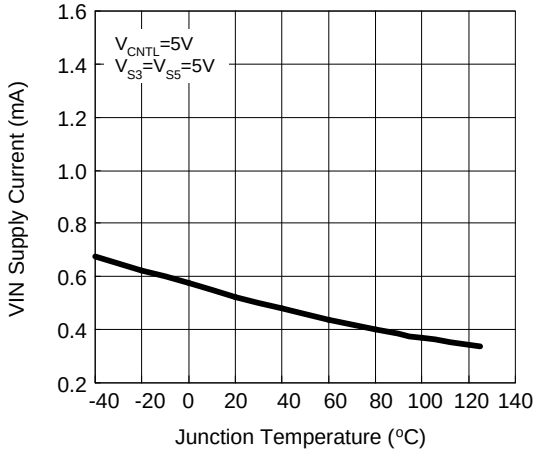
VCNTL Supply Current vs. Temperature



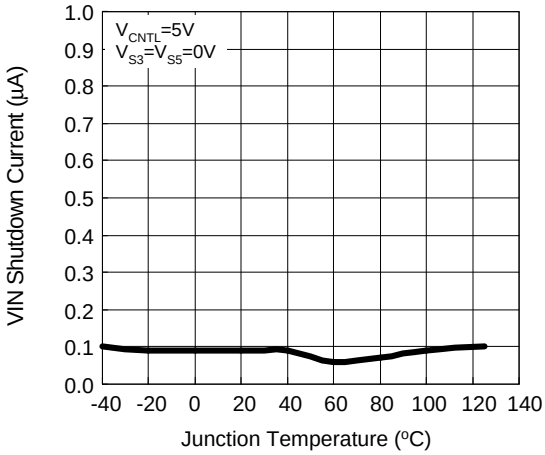
VCNTL Shutdown Current vs. Temperature



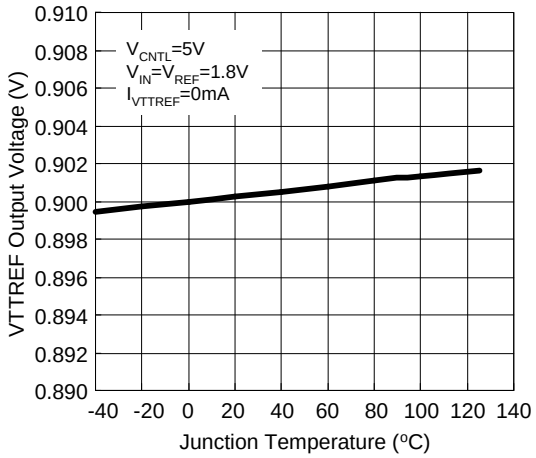
VIN Supply Current vs. Temperature



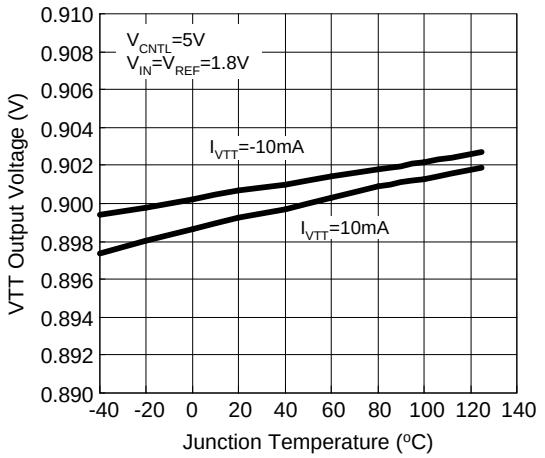
VIN Shutdown Current vs. Temperature



VTTREF Output Voltage vs. Temperature

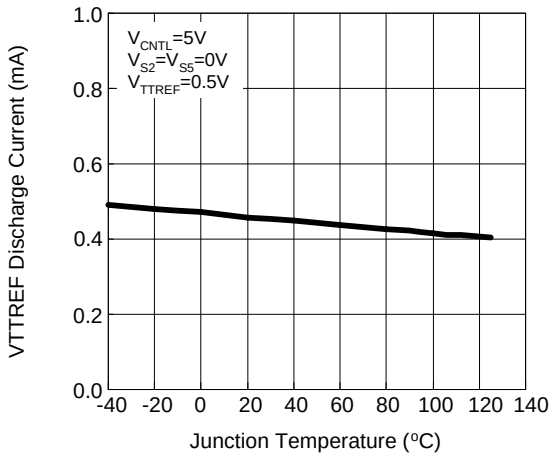


VTT Output Voltage vs. Temperature

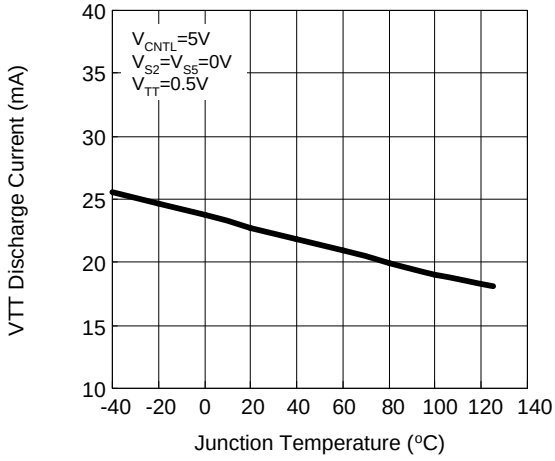


Typical Operating Characteristics (Cont.)

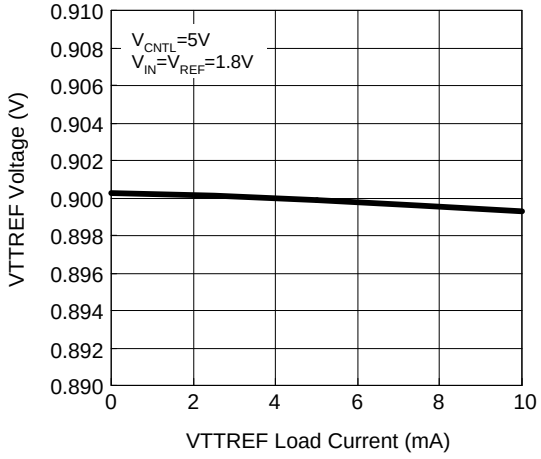
VTTREF Discharge Current vs. Temperature



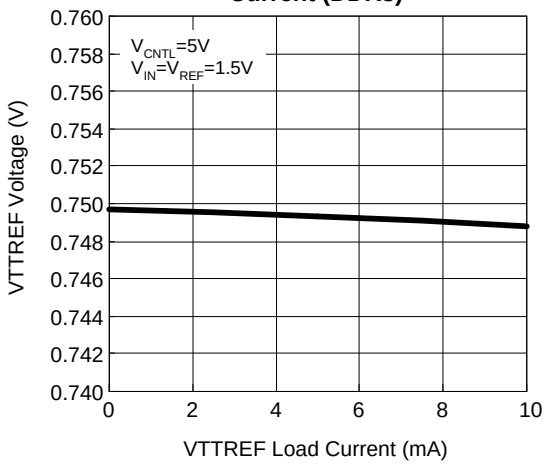
VTT Discharge Current vs. Temperature



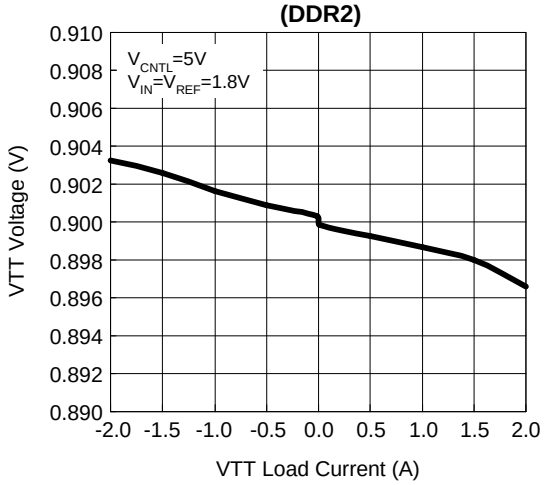
VTTREF Voltage vs. VTTREF Load Current (DDR2)



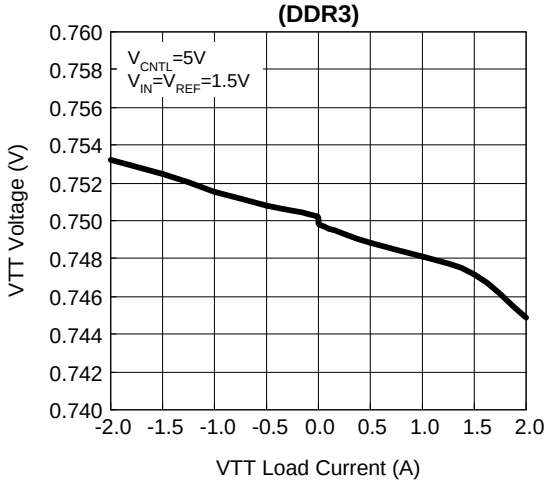
VTTREF Voltage vs. VTTREF Load Current (DDR3)



VTT Voltage vs. VTT Load Current (DDR2)



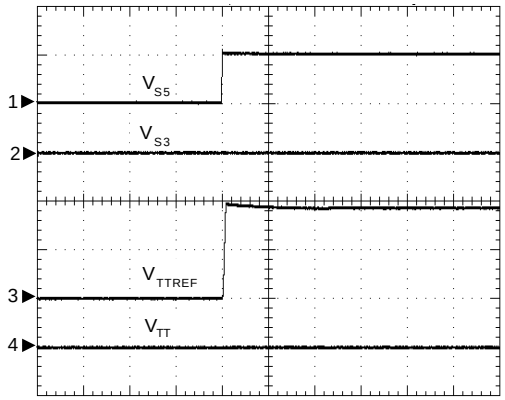
VTT Voltage vs. VTT Load Current (DDR3)



Operating Waveforms

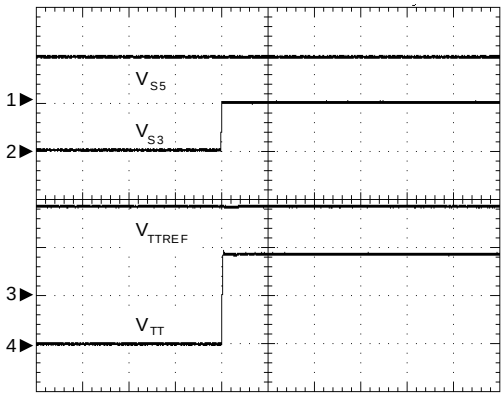
(Refer to the section "Typical Application Circuits" V_{CNTL}=5V, V_{IN}=V_{REF}=1.8V, T_A=25°C)

Startup Waveform-S5 Low to High



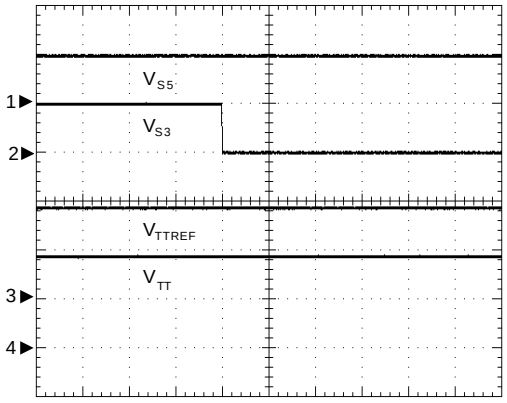
I_{VTT}=I_{VTTREF}=0A
CH1: V_{S5}, 5V/Div, DC
CH2: V_{S3}, 5V/Div, DC
CH3: V_{TTREF}, 500mV/Div, DC
CH4: V_{TT}, 500mV/Div, DC
TIME:100µs/Div

Startup Waveform-S3 Low to High



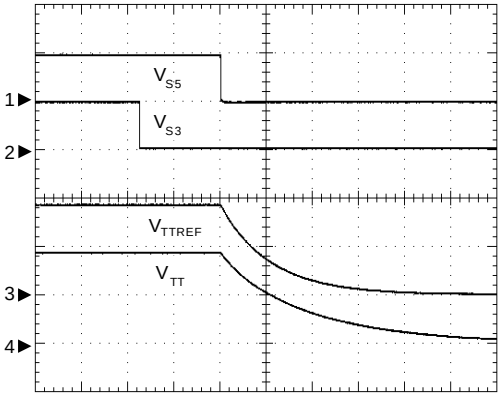
I_{VTT}=I_{VTTREF}=0A
CH1: V_{S5}, 5V/Div, DC
CH2: V_{S3}, 5V/Div, DC
CH3: V_{TTREF}, 500mV/Div, DC
CH4: V_{TT}, 500mV/Div, DC
TIME:100µs/Div

Shutdown Waveform-S3 High to Low



I_{VTT}=I_{VTTREF}=0A
CH1: V_{S5}, 5V/Div, DC
CH2: V_{S3}, 5V/Div, DC
CH3: V_{TTREF}, 500mV/Div, DC
CH4: V_{TT}, 500mV/Div, DC
TIME:100µs/Div

Shutdown Waveform-S3 and S5 High to Low

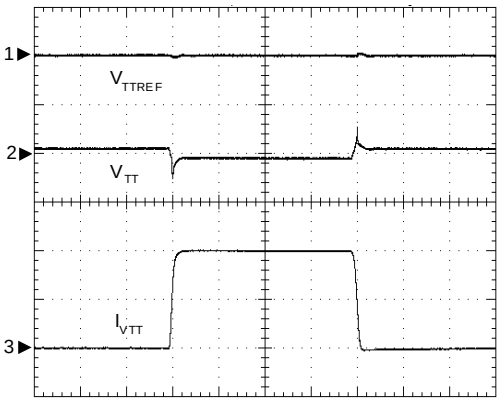


I_{VTT}=I_{VTTREF}=0A
CH1: V_{S5}, 5V/Div, DC
CH2: V_{S3}, 5V/Div, DC
CH3: V_{TTREF}, 500mV/Div, DC
CH4: V_{TT}, 500mV/Div, DC
TIME:100µs/Div

Operating Waveforms (Cont.)

(Refer to the section "Typical Application Circuits" V_{CNTL}=5V, V_{IN}=V_{REF}=1.8V, T_A=25°C)

VTT Load Transient Response

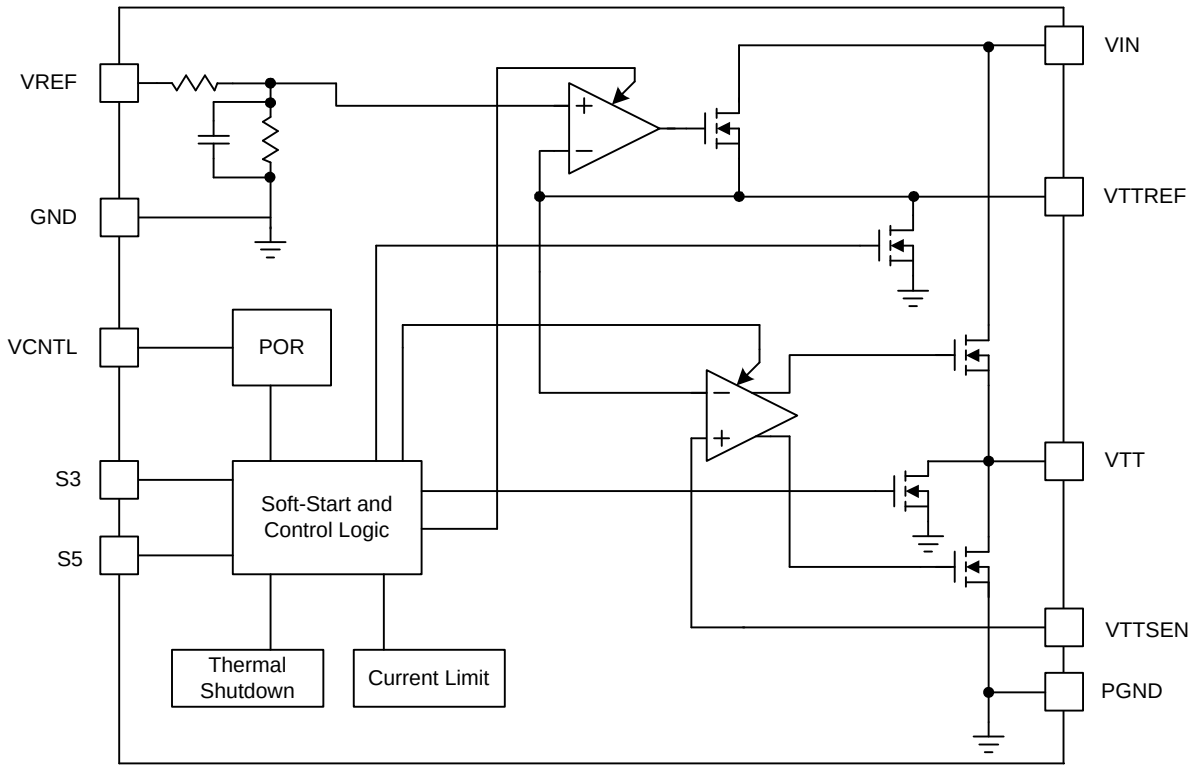


I_{VTT}=-2A (Sink) to 2A (Source) to -2A
CH1: V_{TTREF}, 50mV/Div, DC
CH2: V_{TT}, 50mV/Div, DC
CH3: I_{VTT}, 2A/Div, DC
TIME:100µs/Div

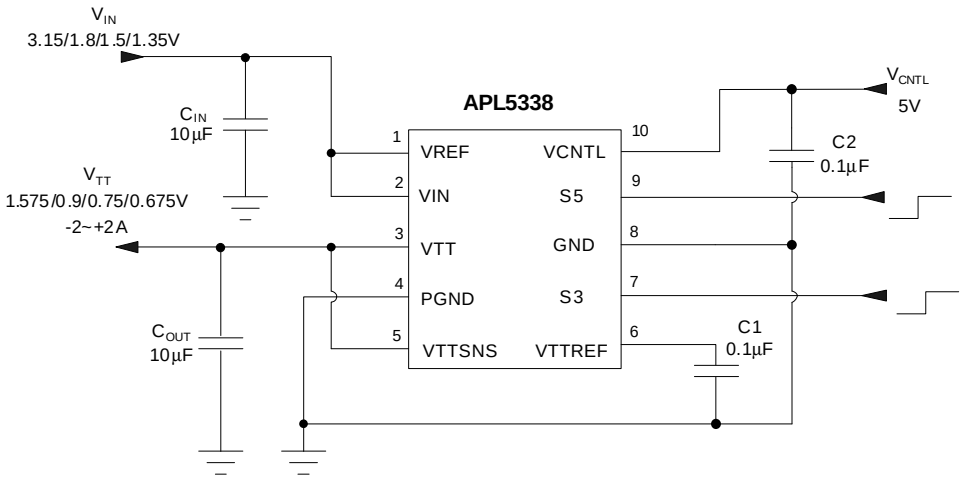
Pin Description

PIN		I/O	FUNCTION
NO.	NAME		
1	VREF	I	Reference Voltage Input for VTT and VTTREF Regulator.
2	VIN	I	Power Input for VTT and VTTREF Pin. An input capacitor should be connected from VIN to PGND.
3	VTT	O	VTT Output Voltage Pin. Source and sink current up to 2A. To insure the stability issue, the output capacitor typical 10µF should be connected from VTT to PGND.
4	PGND	I/O	Power Ground for VIN and VTT.
5	VTTSNS	I	Voltage Sense for VTT. Connect to the positive node of V_{TT} output capacitors.
6	VTTREF	O	VTT Reference Output Pin. A small capacitor 0.1µF should be connected from VTTREF to GND.
7	S3	I	S3 Signal Input.
8	GND	I/O	Signal Ground.
9	S5	I	S5 Signal Input.
10	VCNTL	I	Power Input for Internal Control Circuitry. A bypass capacitor 0.1µF should be connected near the pin.

Block Diagram



Typical Application Circuit



Function Description

VTT Source/Sink Regulator

The APL5338 is a low dropout source/sink linear regulator with maximum 2A source/sink current. Two internal N-channel MOSFETs controlled by separate high bandwidth error amplifiers regulate the output voltage by sourcing current from VIN or sinking current to PGND. To prevent two pass elements from shoot-through, a voltage offset is created between two positive inputs of the error amplifiers.

Power-On-Reset (POR)

The APL5338 monitors the VCNTL pin voltage for power-on-reset function to prevent erroneous operation. The built-in POR circuit keeps the outputs shutoff until internal circuit is operating properly. Typical POR threshold is 3.8V with 0.2V hysteresis.

VTTREF Regulator

VTTREF voltage follows 1/2VREF voltage which is the reference of the VTT regulator. The VTTREF block consists of a resistor divider and a low pass filter. The regulator can source current up to 20mA (typical). To insure the stability, a 0.1µF ceramic capacitor should be connected from VTTREF to GND.

Soft-Start and Current Limit

The APL5338 monitors the output current, both sourcing and sinking current, and limits the maximum output current to prevent damages during current overload or short circuit (shorted from VOUT to GND or VIN) conditions. The APL5338 provides a soft-start function, using the constant current to charge the output capacitor that gives a rapid and linear output voltage rise. If the load current is above the current limit start-up, the VTT cannot start successfully.

Table1. The truth table of S3 and S5 pins

STATE	S3	S5	VTTREF	VTT
S0	H	H	1	1
S3	L	H	1	0(high-Z)
S4/5	L	L	0(discharge)	0(discharge)

S3, S5 Control

The S3 and S5 signals control the VTT and VTTREF states and these pins should be connected to SLP_S3 and SLP_S5 signals respectively. The table1 shows the truth table of the S3 and S5 pins. When both S3 and S5 are above the logic threshold voltage, the VTT and VTTREF are turned on at S0 state. When S3 is low and S5 is high, the VTT voltage is disabled and left high impedance in S3 state. When both S3 and S5 are low, the VTT and VTTREF are turned off and discharged to the ground through internal MOSFETs during S4/S5 state. (Note that if the S3 is forced high and S5 is forced low, then VTTREF is discharged and VTT is at high-Z state. Such condition is not recommended.)

Thermal Shutdown

A thermal shutdown circuit limits the junction temperature of the APL5338. When the junction temperature exceeds +150°C, the device will turn off the MOSFETs, allowing the device to cool down. The regulator regulates the output again through initiation of a new soft-start cycle after the junction temperature cools by 30°C, resulting in a pulsed output during continuous thermal overload conditions. The thermal shutdown is designed with a 30°C hysteresis to lower the average junction temperature during continuous thermal overload conditions, extending lifetime of the device. For normal operation, device power dissipation should be externally limited so that junction temperatures will not exceed +125°C.

Application Information

Input Capacitor

The APL5338 requires proper input capacitors to supply surge current during stepping load transients to prevent the input rail from dropping. Because the parasitic inductor from the voltage sources or other bulk capacitors to the VIN limits the slew rate of the surge current, it is necessary to place the input capacitors near VIN as close as possible. Input capacitors should be greater than 10µF. A capacitor of 0.1µF (MLCC) or above is recommended for VCNTL pin noise decoupling.

Output Capacitor

The APL5338 needs a proper output capacitor to maintain circuit stability and improve transient response over temperature and current. In order to insure the circuit stability, a 10µF MLCC (minimum) as an output capacitor must be placed near the VTT. With X5R and X7R dielectrics.

Thermal Consideration

The APL5338 maximum power dissipation depends on the differences of the thermal resistance and temperature between junction and ambient air. The power dissipation P_D across the device is:

$$P_D = (T_J - T_A) / \theta_{JA}$$

where (T_J-T_A) is the temperature difference between the junction and ambient air. θ_{JA} is the thermal resistance between junction and ambient air. Assuming the T_A=25°C and maximum T_J=150°C (typical thermal limit threshold), the maximum power dissipation is calculated as:

$$P_{D(max)}=(150-25)/60$$
$$= 2.08(W)$$

For normal operation, do not exceed the maximum operating junction temperature of T_J = 125°C. The calculated power dissipation should be less than:

$$P_D=(125-25)/60$$
$$= 1.66(W)$$

The exposed pad provides an electrical connection to ground and channels heat away. Connect the exposed pad to ground by using a large ground plane.

Layout Consideration

Figure 1 illustrates the layout. Below is a checklist for your layout:

1. Please place the input capacitors close to the VIN.
2. Output capacitors for VTT must be close to the pin with short and wide track.
3. VTTSNS should be connected to the output capacitors of VTT separated from large current path to avoid effect of ESR and ESL. The ESR and ESL of ground track between VTT and GND should be minimized.
4. VREF should be connected to VIN by a separate track. VREF is the reference voltage of VTTREF, so avoid any noise to get into the VREF.
5. PGND is the ground of VIN and VTT. GND is the signal ground of VREF, VTTREF S3 and S5. GND and PGND should be isolated with a single point connection between them.
6. Soldering the exposed pad to ground is good for heatsinking. Numerous vias 0.33 mm in diameter connected from the thermal land to the internal/solder-side ground plane(s) should be used to enhance dissipation.

Large ground plane is good for heatsinking. Optimum performance can only be achieved when the device is mounted on a PC board according to the board layout diagrams which are shown as Figure 2.

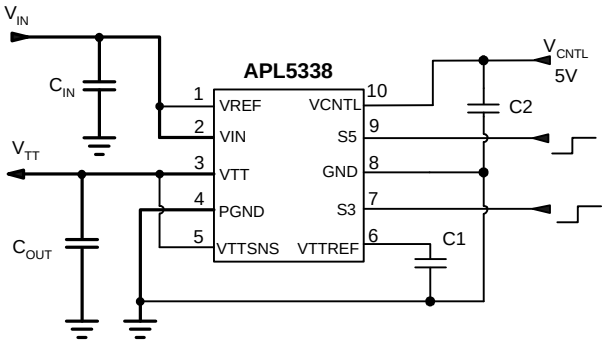


Figure 1

Application Information (Cont.)

Layout Consideration (Cont.)

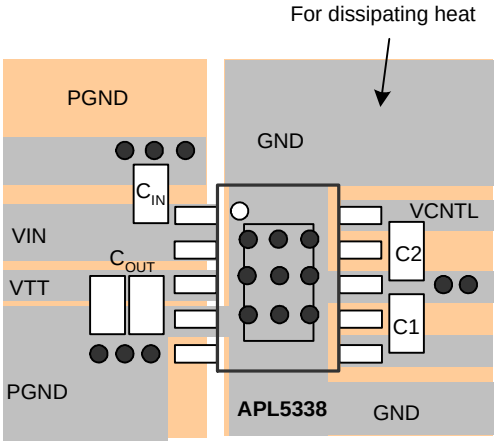
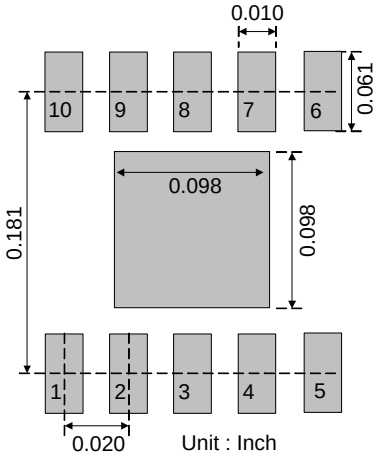
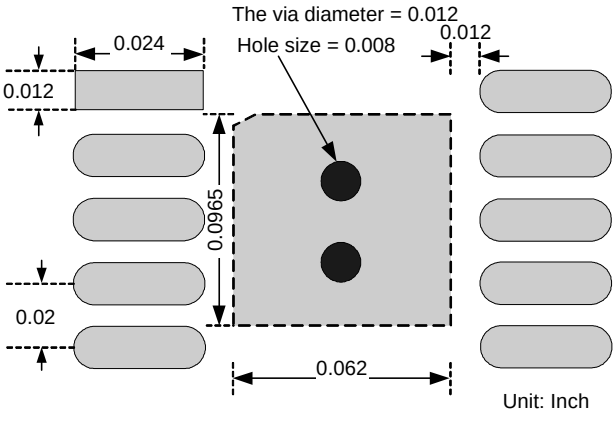


Figure 2. Recommended Layout

Recommended Minimum Footprint



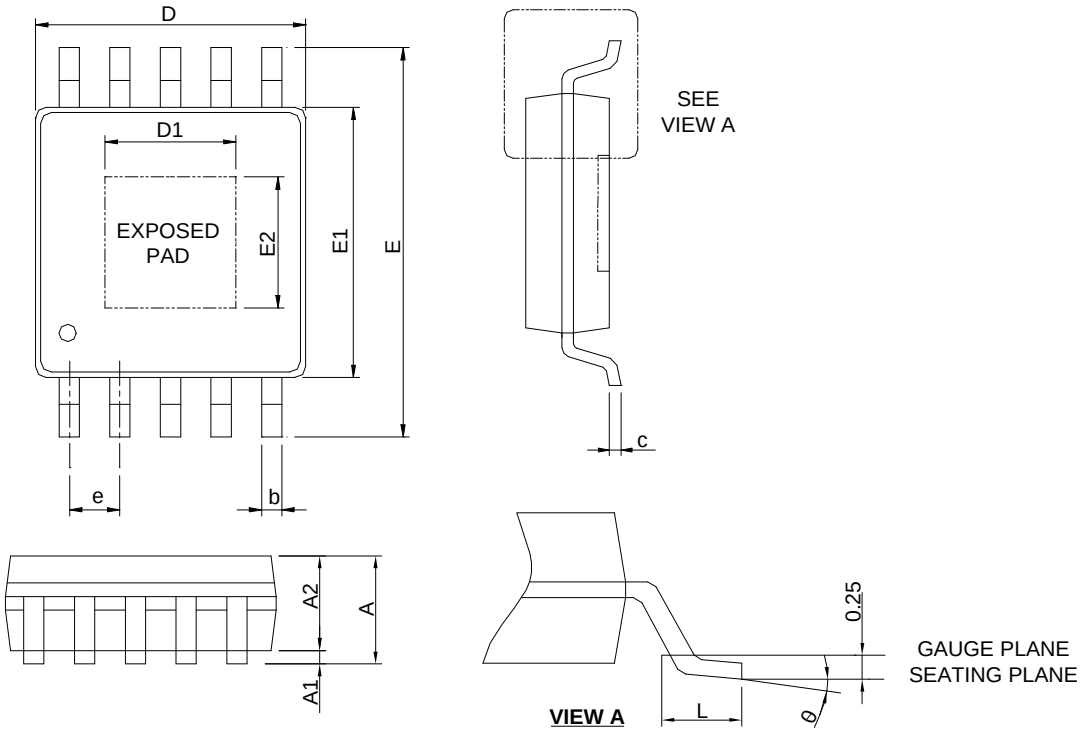
MSOP-8P



TDFN3x3-10

Package Information

MSOP-10P

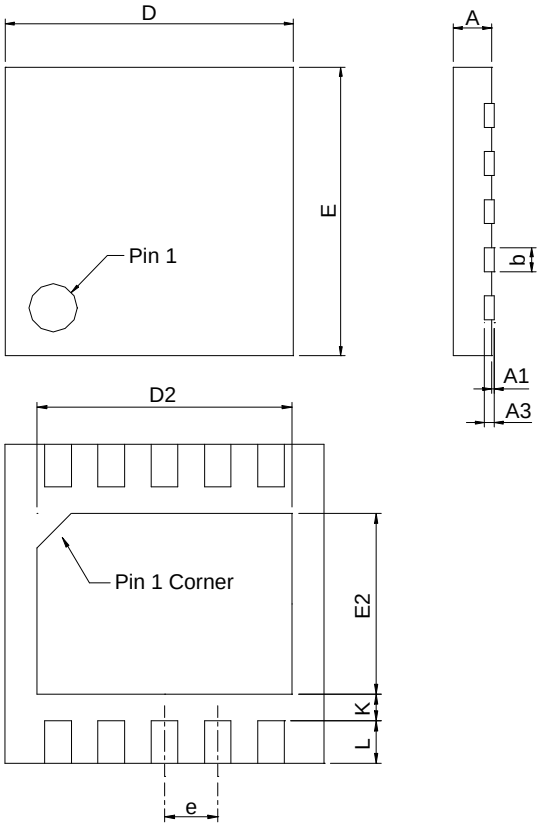


SYMBOL	MSOP-10P			
	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A		1.10		0.043
A1	0.00	0.15	0.000	0.006
A2	0.75	0.95	0.030	0.037
b	0.17	0.33	0.007	0.013
c	0.08	0.23	0.003	0.009
D	2.90	3.10	0.114	0.122
D1	1.50	2.50	0.059	0.098
E	4.70	5.10	0.185	0.201
E1	2.90	3.10	0.114	0.122
E2	1.50	2.50	0.059	0.098
e	0.50 BSC		0.020 BSC	
L	0.40	0.80	0.016	0.031
θ	0°	8°	0°	8°

Note: 1. Follow JEDEC MO-187 BA-T.
2. Dimension "D" does not include mold flash, protrusions or gate burrs. Mold flash, protrusion or gate burrs shall not flash or protrusions.
3. Dimension "E1" does not include inter-lead flash or protrusions. Inter-lead flash and protrusions shall not exceed 6 mil per side.

Package Information

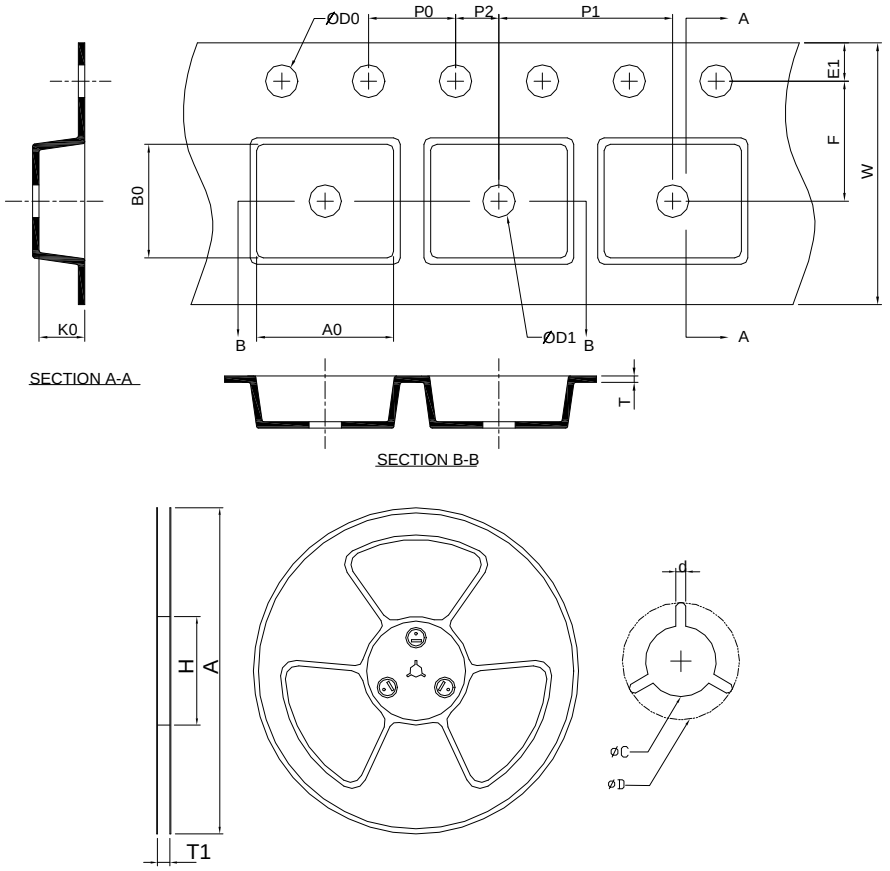
TDFN3x3-10



SYMBOL	TDFN3x3-10			
	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A	0.70	0.80	0.028	0.031
A1	0.00	0.05	0.000	0.002
A3	0.20 REF		0.008 REF	
b	0.18	0.30	0.007	0.012
D	2.90	3.10	0.114	0.122
D2	2.20	2.70	0.087	0.106
E	2.90	3.10	0.114	0.122
E2	1.40	1.75	0.055	0.069
e	0.50 BSC		0.020 BSC	
L	0.30	0.50	0.012	0.020
K	0.20		0.008	

Note : 1. Followed from JEDEC MO-229 VEED-5.

Carrier Tape & Reel Dimensions



Application	A	H	T1	C	d	D	W	E1	F
MSOP-10P	330.0±2.00	50 MIN.	12.4+2.00 -0.00	13.0+0.50 -0.20	1.5 MIN.	20.2 MIN.	12.0±0.30	1.75±0.10	5.5±0.05
	P0	**P1**	**P2**	**D0**	**D1**	**T**	**A0**	**B0**	**K0**
	4.00±0.10	8.00±0.10	2.00±0.05	1.5+0.10 -0.00	1.5 MIN.	0.6+0.00 -0.40	5.30±0.20	3.30±0.20	1.40±0.20
Application	**A**	**H**	**T1**	**C**	**d**	**D**	**W**	**E1**	**F**
TDFN3x3-10	330.0±2.00	50 MIN.	12.4+2.00 -0.00	13.0+0.50 -0.20	1.5 MIN.	20.2 MIN.	12.0±0.30	1.75±0.10	5.5±0.05
	P0	**P1**	**P2**	**D0**	**D1**	**T**	**A0**	**B0**	**K0**
	4.0±0.10	8.0±0.10	2.0±0.05	1.5+0.10 -0.00	1.5 MIN.	0.6+0.00 -0.40	3.30±0.20	3.30±0.20	1.30±0.20

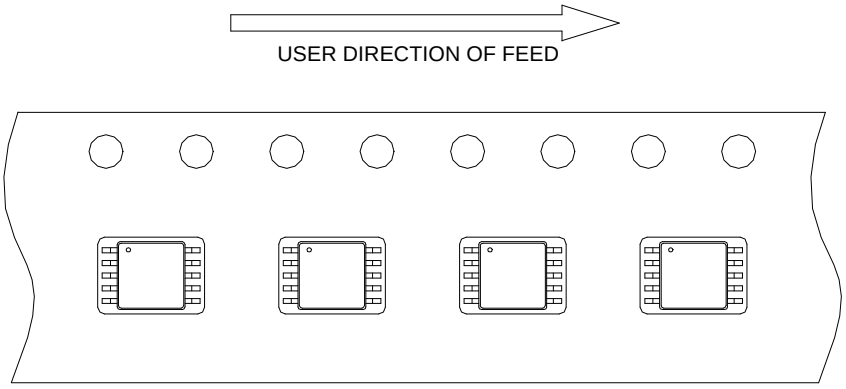
(mm)

Devices Per Unit

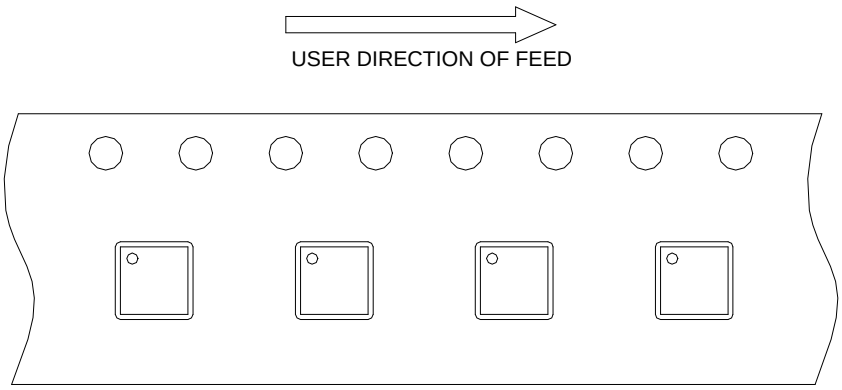
Package Type	Unit	Quantity
MSOP-10P	Tape & Reel	3000
TDFN3x3-10	Tape & Reel	3000

Taping Direction Information

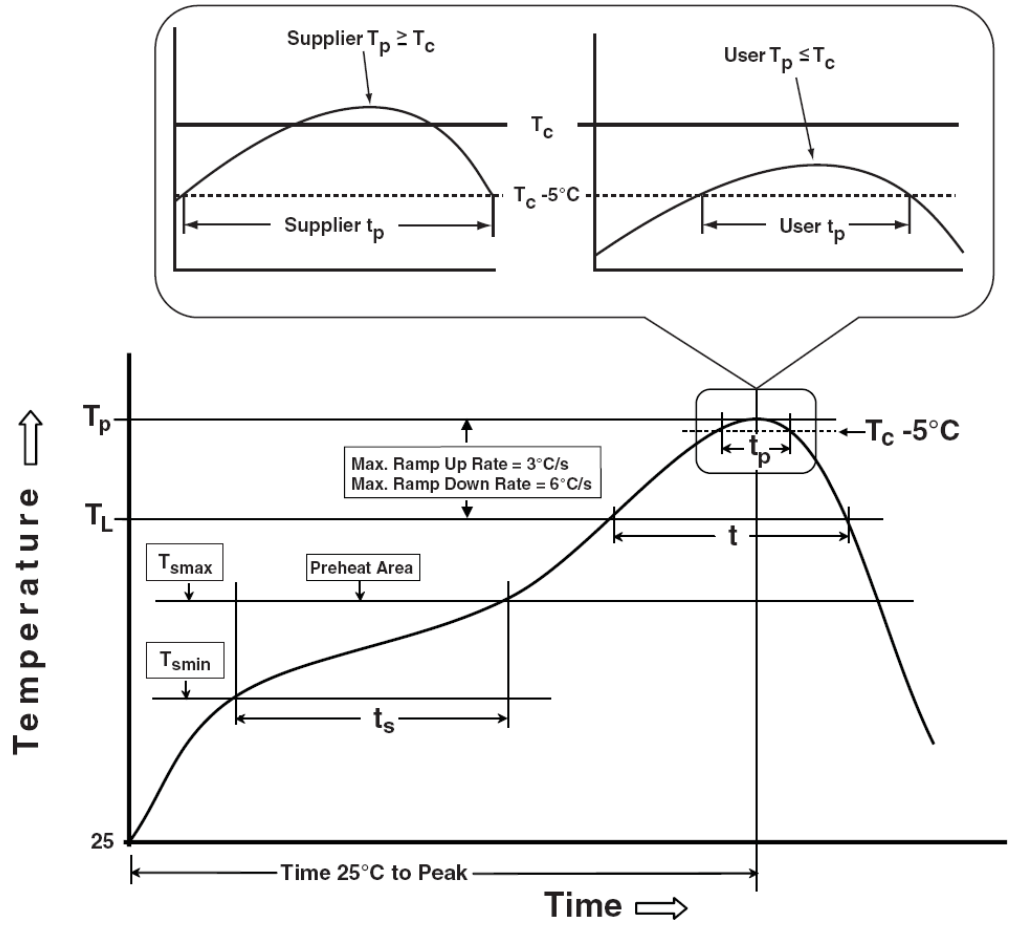
MSOP-10P



TDFN3x3-10



Classification Profile



Classification Reflow Profiles

Profile Feature	Sn-Pb Eutectic Assembly	Pb-Free Assembly
Preheat & Soak Temperature min (T_{smin}) Temperature max (T_{smax}) Time (T_{smin} to T_{smax}) (t_s)	 100 °C 150 °C 60-120 seconds	 150 °C 200 °C 60-120 seconds
Average ramp-up rate (T_{smax} to T_P)	3 °C/second max.	3°C/second max.
Liquidous temperature (T_L) Time at liquidous (t_L)	183 °C 60-150 seconds	217 °C 60-150 seconds
Peak package body Temperature (T_p)*	See Classification Temp in table 1	See Classification Temp in table 2
Time (t_P)** within 5°C of the specified classification temperature (T_c)	20** seconds	30** seconds
Average ramp-down rate (T_p to T_{smax})	6 °C/second max.	6 °C/second max.
Time 25°C to peak temperature	6 minutes max.	8 minutes max.
* Tolerance for peak profile Temperature (T_p) is defined as a supplier minimum and a user maximum. ** Tolerance for time at peak profile temperature (t_p) is defined as a supplier minimum and a user maximum.		

Table 1. SnPb Eutectic Process – Classification Temperatures (Tc)

Package Thickness	Volume mm^3 <350	Volume mm^3 ³350
<2.5 mm	235 °C	220 °C
≥2.5 mm	220 °C	220 °C

Table 2. Pb-free Process – Classification Temperatures (Tc)

Package Thickness	Volume mm^3 <350	Volume mm^3 350-2000	Volume mm^3 >2000
<1.6 mm	260 °C	260 °C	260 °C
1.6 mm – 2.5 mm	260 °C	250 °C	245 °C
≥2.5 mm	250 °C	245 °C	245 °C

Reliability Test Program

Test item	Method	Description
SOLDERABILITY	JESD-22, B102	5 Sec, 245°C
HOLT	JESD-22, A108	1000 Hrs, Bias @ T_j=125°C
PCT	JESD-22, A102	168 Hrs, 100%RH, 2atm, 121°C
TCT	JESD-22, A104	500 Cycles, -65°C~150°C
HBM	MIL-STD-883-3015.7	VHBM≧2KV
MM	JESD-22, A115	VMM≧200V
Latch-Up	JESD 78	10ms, 1_{tr}≧100mA

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