Data Sheet | November 3, 2011 | FN6491.2

1.4GHz Current Feedback Amplifiers with Enable

The 5962-0625601QXC and 5962-0625602QXC are fully DLA SMD compliant parts and the SMD data sheets are available on the DLA website (http://www.landandmaritime.dla.mil/Programs/MilSpec/DocSearch.aspx). The 5962-0625601QXC is electrically equivalent to the EL5166, the 5962-0625602QXC is electrically equivalent to the EL5167. Reference equivalent “EL” data sheet for additional information. The amplifiers are of the current feedback variety and exhibit a very high bandwidth of 1.4GHz at A_V = +1 and 800MHz at A_V = +2. This makes these amplifiers ideal for today's high speed video and monitor applications, as well as a number of RF and IF frequency designs.

With a supply current of just 12mA and the ability to run from a single supply voltage from 5V to 12V, these amplifiers offer very high performance for little power consumption.

The 5962-0625601QXC also incorporates an enable and disable function to reduce the supply current to 13µA typical per amplifier. Allowing the CE pin to float or applying a low logic level will enable the amplifier.

Ordering Information

PART NUMBER	PART MARKING	PACKAGE	PKG. DWG. #
5962-0625601QXC	06256 01QXC	10 Ld Flat Pack	K10.A
5962-0625602QXC	06256 02QXC	10 Ld Flat Pack	K10.A

NOTE: These Intersil Pb-free Hermetic packaged products employ 100% Au plate - e4 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations.

Features

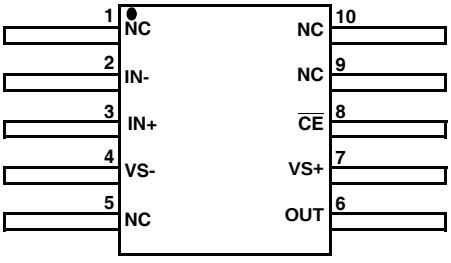
- Gain-of-1 bandwidth = 1.4GHz/gain-of-2 bandwidth = 800MHz
- 6000V/µs slew rate
- Single and dual supply operation from 5V to 12V
- Low noise = 1.5nV/√Hz
- 12mA supply current
- Fast enable/disable (5962-0625601QXC only)

Applications

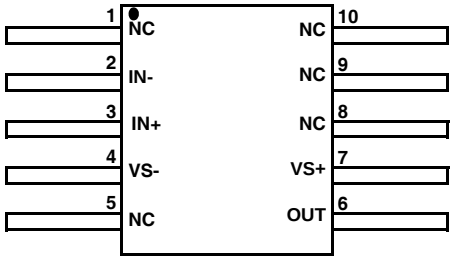
- Video amplifiers
- Cable drivers
- RGB amplifiers
- Test equipment
- Instrumentation
- Current to voltage converters

Pinouts

5962-0625601QXC
(10 LD FLAT PACK)
TOP VIEW



5962-0625602QXC
(10 LD FLAT PACK)
TOP VIEW



Absolute Maximum Ratings (T_A = +25°C)

Supply Voltage between V_S+ and V_S- 12.6V
Slewrate between V_S+ and V_S- 1V/µs
Maximum Continuous Output Current 20mA
I into V_{IN}+, V_{IN}-, Enable Pins . . . . . ±4mA
Pin Voltages . . . . . V_S- -0.5V to V_S+ +0.5V

Thermal Information

Thermal Resistance (Typical)	θ_{JA} (°C/W)	θ_{JC} (°C/W)
Flat Pack Package (Notes 1, 2)	165	60

Storage Temperature . . . . . -65°C to +150°C
Ambient Operating Temperature . . . . . -55°C to +125°C
Die Junction Temperature . . . . . +150°C
Power Dissipation 144mW

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.

NOTES:

1. θ_{JA} is measured with the component mounted on a low effective thermal conductivity test board in free air. See Tech Brief TB379 for details.
2. For θ_{JC}, the “case temp” location is the center of the exposed metal pad on the package underside.

IMPORTANT NOTE: All parameters having Min/Max specifications are guaranteed. Typical values are for information purposes only. Unless otherwise noted, all tests are at the specified temperature and are pulsed tests, therefore: $T_J = T_C = T_A$

Electrical Specifications

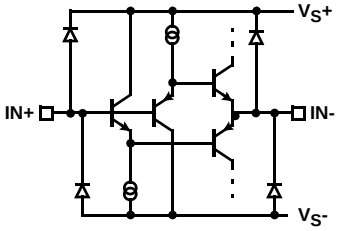
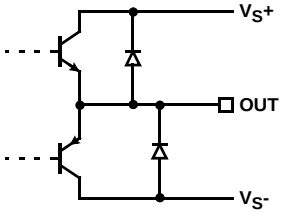
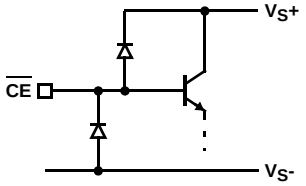
V_S+ = +5V, V_S- = -5V, R_F = 392Ω for A_V = 1, R_F = 250Ω for A_V = 2, R_L = 150Ω, T_A = +25°C Unless Otherwise Specified.

PARAMETER	DESCRIPTION	CONDITIONS	MIN	TYP	MAX	UNIT
AC PERFORMANCE						
BW	-3dB Bandwidth	A_V = +1		1400		MHz
		A_V = +2		800		MHz
BW1	0.1dB Bandwidth	A_V = +2		100		MHz
SR	Slew Rate	V_O = -2.5V to +2.5V, A_V = +2		6000		V/µs
t_S	0.1% Settling Time	V_{OUT} = -2.5V to +2.5V, A_V = -1		8		ns
e_N	Input Voltage Noise			1.7		nV/√Hz
i_N-	IN- Input Current Noise			19		pA/√Hz
i_N+	IN+ Input Current Noise			50		pA/√Hz
dG	Differential Gain Error (Note 3)	A_V = +2		0.01		%
dP	Differential Phase Error (Note 3)	A_V = +2		0.03		°
INPUT CHARACTERISTICS						
C_{IN}	Input Capacitance			1.5		pF
ENABLE (5962-0625601QXC ONLY)						
t_{EN}	Enable Time			170		ns
t_{DIS}	Disable Time			1.25		µs

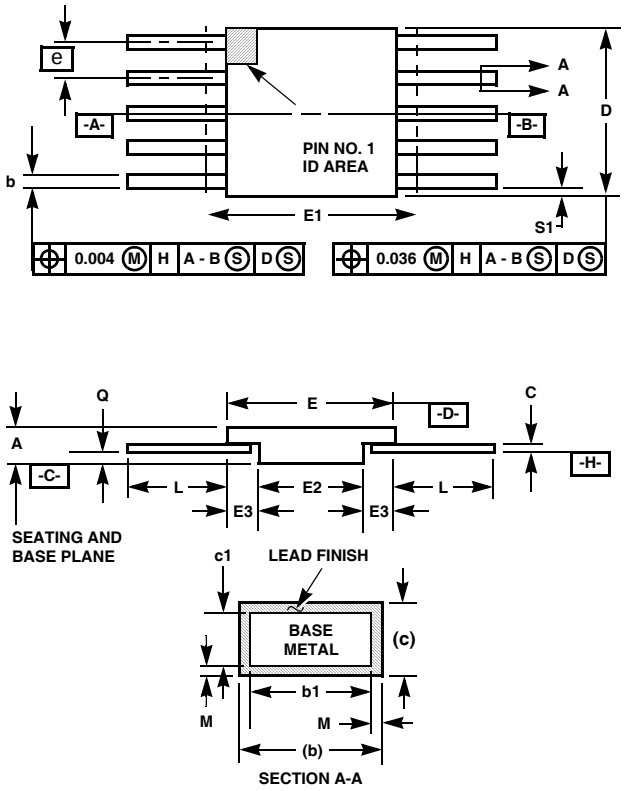
NOTE:

3. Standard NTSC test, AC signal amplitude = 286mV, f = 3.58MHz.

Pin Descriptions

5962-0625601QXCIS (10 Ld FLAT PACK)	5962-0625602QXCIS (10 ld FLAT PACK)	Pin Name	Function	Equivalent Circuit
1, 5, 9, 10	1, 5, 8 , 9 ,10	NC	Not connected	
2	2	IN-	Inverting input	 CIRCUIT 1
3	3	IN+	Non-inverting input	(See circuit 1)
4	4	VS-	Negative supply	
6	6	OUT	Output	 CIRCUIT 2
7	7	VS+	Positive supply	
8		$\overline{CE}$	Chip enable	 CIRCUIT 3

Ceramic Metal Seal Flatpack Packages (Flatpack)



K10.A MIL-STD-1835 CDFP3-F10 (F-4A, CONFIGURATION B)
10 LEAD CERAMIC METAL SEAL FLATPACK PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.045	0.115	1.14	2.92	-
b	0.015	0.022	0.38	0.56	-
b1	0.015	0.019	0.38	0.48	-
c	0.004	0.009	0.10	0.23	-
c1	0.004	0.006	0.10	0.15	-
D	-	0.290	-	7.37	3
E	0.240	0.260	6.10	6.60	-
E1	-	0.280	-	7.11	3
E2	0.125	-	3.18	-	-
E3	0.030	-	0.76	-	7
e	0.050 BSC		1.27 BSC		-
k	0.008	0.015	0.20	0.38	2
L	0.250	0.370	6.35	9.40	-
Q	0.026	0.045	0.66	1.14	8
S1	0.005	-	0.13	-	6
M	-	0.0015	-	0.04	-
N	10		10		-

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NOTES:

1. Index area: A notch or a pin one identification mark shall be located adjacent to pin one and shall be located within the shaded area shown. The manufacturer's identification shall not be used as a pin one identification mark. Alternately, a tab (dimension k) may be used to identify pin one.
2. If a pin one identification mark is used in addition to a tab, the limits of dimension k do not apply.
3. This dimension allows for off-center lid, meniscus, and glass overrun.
4. Dimensions b1 and c1 apply to lead base metal only. Dimension M applies to lead plating and finish thickness. The maximum limits of lead dimensions b and c or M shall be measured at the centroid of the finished lead surfaces, when solder dip or tin plate lead finish is applied.
5. N is the maximum number of terminal positions.
6. Measure dimension S1 at all four corners.
7. For bottom-brazed lead packages, no organic or polymeric materials shall be molded to the bottom of the package to cover the leads.
8. Dimension Q shall be measured at the point of exit (beyond the meniscus) of the lead from the body. Dimension Q minimum shall be reduced by 0.0015 inch (0.038mm) maximum when solder dip lead finish is applied.
9. Dimensioning and tolerancing per ANSI Y14.5M - 1982.
10. Controlling dimension: INCH.