INTEGRATED TECHNOLOGY EXPRESS, INC.

IT8673F

Advanced Input / Output (Advanced I/O)

Preliminary Specification V0.5

INTEGRATED TECHNOLOGY EXPRESS, INC.

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ITE, Inc.
Marketing Department
8F, No. 233-1, Bao Chiao Rd., Hsin Tien
Taipei County 231, Taiwan, R.O.C.

Phone: (02) 2912-6889
Fax: (02) 2910-2551, 2910-2552

ITE (USA) Inc.
Marketing Department
1235 Midas Way
Sunnyvale, CA 94086
U.S.A.

Phone: (408) 530-8860
Fax: (408) 530-8861

ITE (USA) Inc.
Eastern U.S.A. Sales Office
896 Summit St., #105
Round Rock, TX 78664
U.S.A.

Phone: (512) 388-7880
Fax: (512) 388-3108

If you have any marketing or sales questions, please contact:

Lawrence Liu, at ITE Taiwan: E-mail: lawrence.liu@ite.com.tw, Tel: 886-2-29126889 X6071, Fax: 886-2-29102551
David Lin, at ITE U.S.A: E-mail: david.lin@iteusa.com, Tel: (408) 980-8168 X238, Fax: (408) 980-9232
Don Gardenhire, at ITE Eastern USA Office: E-mail: don.gardenhire@iteusa.com, Tel: (512) 388-7880, Fax: (512) 388-3108

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Revision History

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1. Features

- **PC98/99, ACPI & LANDesk Compliant**
  - ISA Plug and Play register set compatible
  - ACPI V. 1.0 and LANDesk 3.1 compliant
  - Supports eight logical devices
  - 16-bit address decoding
  - Three selectable DMA channels
  - PC98/99 I/O solution
  - Supports IRQ sharing

- **Fan Controller**
  - Provides FAN ON/OFF and speed control
  - Up to 3 programmable Pulse Width Modulation (PWM) FAN control outputs
  - Each PWM output supports 128 steps of PWM modes
  - Up to 3 Fan tachometer inputs

- **2 Serial Ports**
  - Supports two standard 16C550 UARTs
  - UART2 also supports IrDA 1.0 (SIR) and ASKIR infrared protocols
  - Supports MIDI baud rate

- **IEEE 1284 Parallel Port**
  - Standard mode—Bi-directional SPP
  - Enhanced mode—EPP V. 1.7 and EPP V. 1.9 compliant
  - High speed mode—ECP, IEEE 1284 compliant
  - Backdrive current reduction
  - Printer power-on damage reduction

- **Floppy Disk Controller**
  - Enhanced digital data separator
  - Drives A and B can be logically swapped via registers
  - 3-Mode drive supported
  - Supports automatic write protection via software
  - Supports two 360K/720K/1.2M/1.44M/2.88M floppy disk drives

- **Keyboard Controller**
  - 8042 compatible
  - 2KB programmable ROM
  - 256-byte data RAM
  - GateA20 and Keyboard reset output
  - Supports keylock function (Thru GPIO)
  - Supports PS/2 mouse
  - Supports any key, or 2-5 sequential keys, or 1-3 simultaneous keys keyboard power-on feature
  - Supports mouse double-click and/or mouse move power on event

- **Consumer Remote Control (TV Remote) IR**

- **8 General Purpose I/O Pins**
  - Input mode supports either switch de-bounce
  - Output mode supports 2 sets of programmable LED blinking periods

- **Chasis Open Detection Support**

- **Serial IRQ Support**

- **ITE innovative automatic power-failure resume & power button De-bounce**

- **Vbat & Vcch Support**

- **Single 24 MHz or 48 MHz Clock Input**

- **Single +5V Power Supply**

- **128-pin QFP**

2. General Description

The IT8673F is an ISA-based highly integrated I/O device. The IT8673F provides all the functions required by legacy Super I/O and FAN Controller functionalities. The IT8673F meets the "Microsoft® PC98/99 system design guide" requirements and is ACPI and LANDesk compliant.

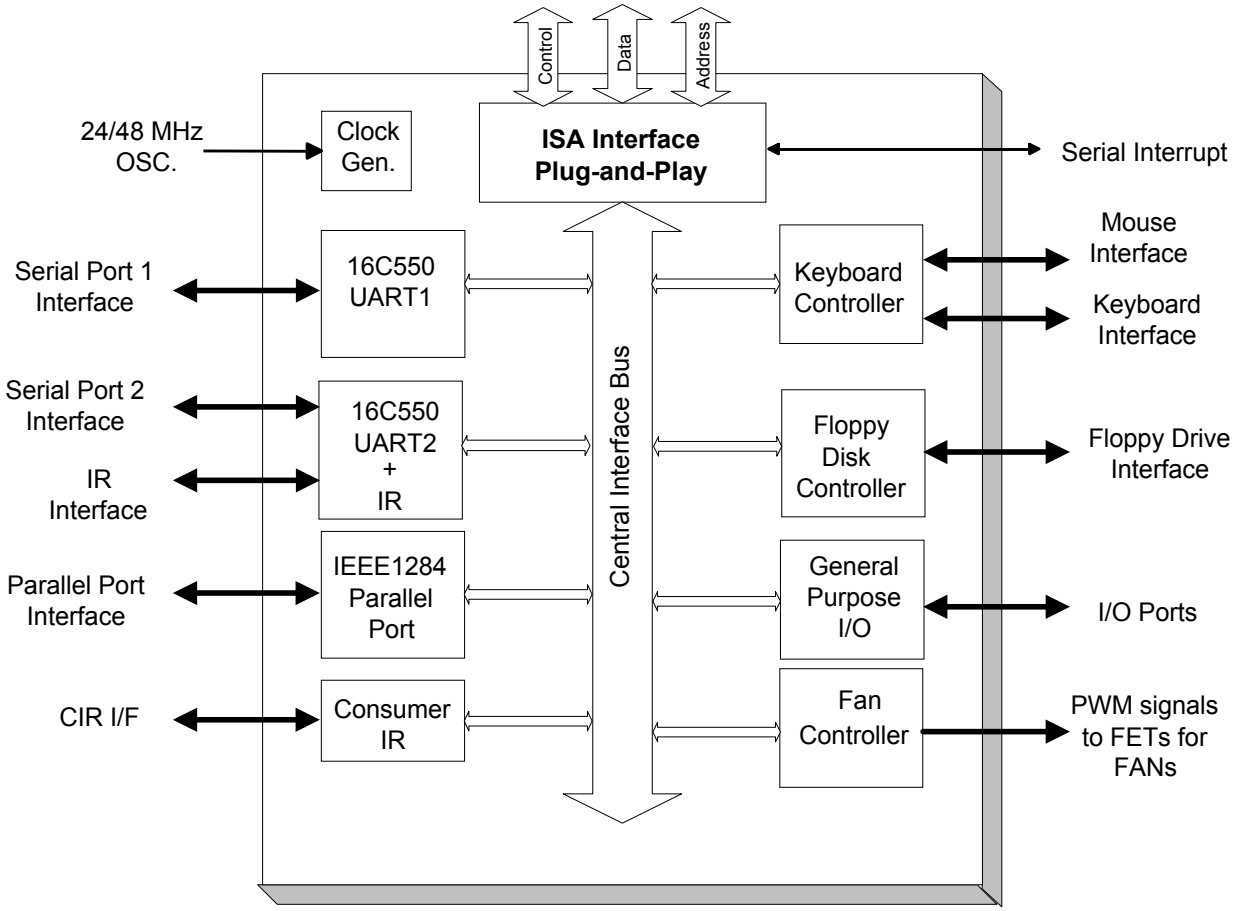
The IT8673F has integrated eight logical devices, featuring an FAN Controller. The fan speed controller is responsible to control three fan speeds through three 128 steps of Pulse Width Modulation (PWM) output pins and to monitor three fans' tachometer inputs.

Other features include a high-performance 2.88MB floppy disk controller with digital data separator, which is able to support two 360K/720K/1.2M/1.44M/2.88M floppy disk drives. One multi-mode high-performance parallel port features the bi-directional Standard Parallel Port (SPP), the Enhanced Parallel Port (EPP, V.1.7 and V.1.9 are supported), and the IEEE1284 compliant Extended Capabilities Port (ECP). Two 16C550 standard compatible enhanced UARTs perform asynchronous communication with enhanced wireless IrDA 1.0 or ASKIR protocols. One Consumer IR controller supports multiple remote control IR protocols. The I/O device also has an integrated 8042 compatible Keyboard Controller with 2KB of programmable ROM for customer application.

These eight logical devices can be individually enabled or disabled via software configuration registers. The IT8673F utilizes power-saving circuitry to reduce power consumption and once a logical device is disabled the inputs are gated, the outputs are tri-state and the input clock is disabled. The IT8673F requires just a single 24/48 MHz clock input and operates with only single +5V power supply.

The IT8673F is available in 128-pin QFP (Quad Flat package).

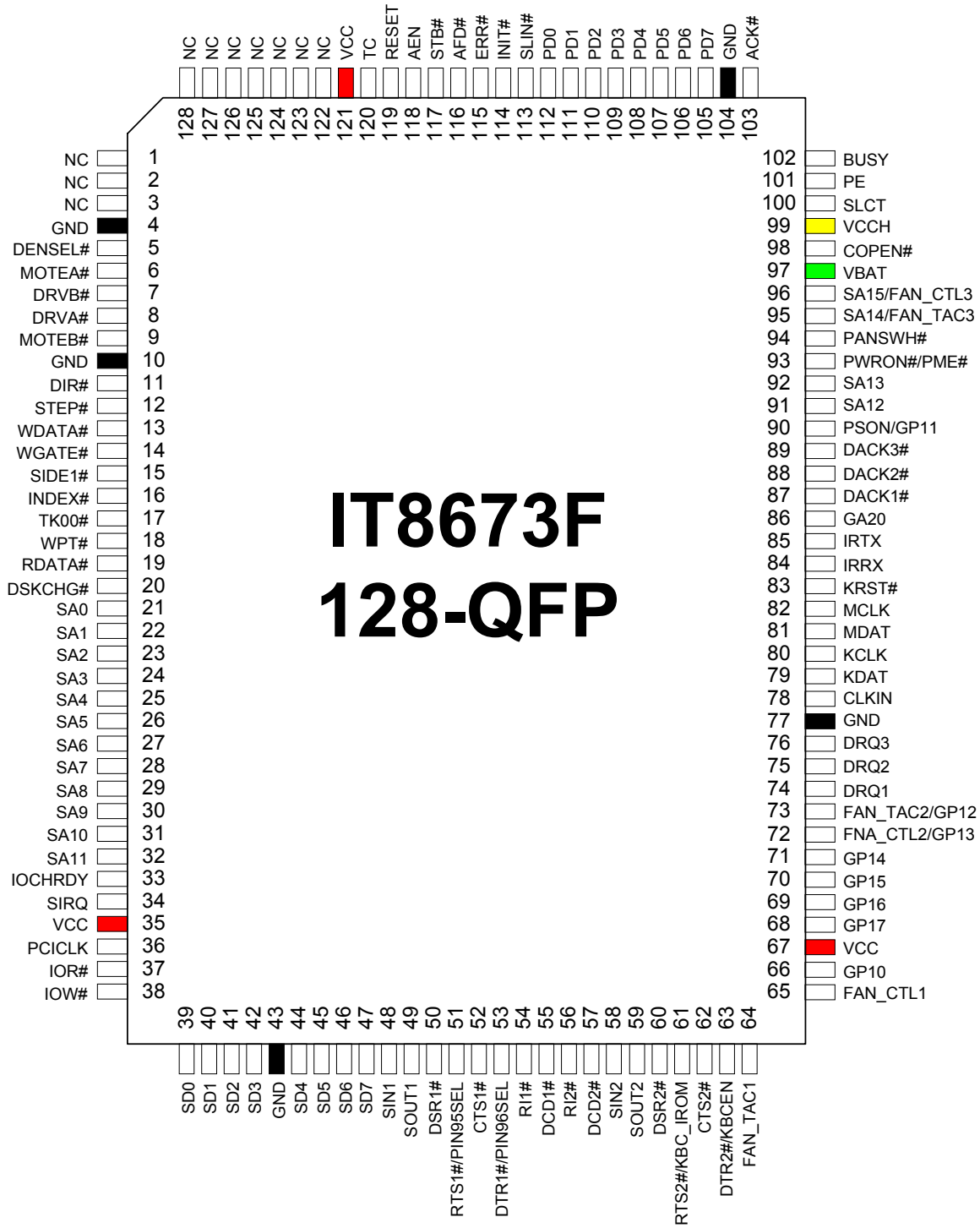
3. Block Diagram



4. Pinout Table

Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal
1	NC	33	IOCHRDY	65	FAN_CTL1	97	VBAT
2	NC	34	SIRQ	66	GP10	98	COPEN#
3	NC	35	VCC	67	VCC	99	VCCH
4	GND	36	PCICLK	68	GP17	100	SLCT
5	DENSEL#	37	IOR#	69	GP16	101	PE
6	MOTEA#	38	IOW#	70	GP15	102	BUSY
7	DRVB#	39	SD0	71	GP14	103	ACK#
8	DRVA#	40	SD1	72	FAN_CTL2/GP13	104	GND
9	MOTEB#	41	SD2	73	FAN_TAC2/GP12	105	PD7
10	GND	42	SD3	74	DRQ1	106	PD6
11	DIR#	43	GND	75	DRQ2	107	PD5
12	STEP#	44	SD4	76	DRQ3	108	PD4
13	WDATA#	45	SD5	77	GND	109	PD3
14	WGATE#	46	SD6	78	CLKIN	110	PD2
15	SIDE1#	47	SD7	79	KDAT	111	PD1
16	INDEX#	48	SIN1	80	KCLK	112	PD0
17	TK00#	49	SOUT1	81	MDAT	113	SLIN#
18	WPT#	50	DSR1#	82	MCLK	114	INIT#
19	RDATA#	51	RTS1#/PIN95SEL	83	KRST#	115	ERR#
20	DSKCHG#	52	CTS1#	84	IRRX	116	AFD#
21	SA0	53	DTR1#/PIN96SEL	85	IRTX	117	STB#
22	SA1	54	RI1#	86	GA20	118	AEN
23	SA2	55	DCD1#	87	DACK1#	119	RESET
24	SA3	56	RI2#	88	DACK2#	120	TC
25	SA4	57	DCD2#	89	DACK3#	121	VCC
26	SA5	58	SIN2	90	PSON/GP11	122	NC
27	SA6	59	SOUT2	91	SA12	123	NC
28	SA7	60	DSR2#	92	SA13	124	NC
29	SA8	61	RTS2#/KBC_IROM	93	PWRON#/PME#	125	NC
30	SA9	62	CTS2#	94	PANSWH#	126	NC
31	SA10	63	DTR2#/KBCEN	95	SA14/FAN_TAC3	127	NC
32	SA11	64	FAN_TAC1	96	SA15/FAN_CTL3	128	NC

5. Pin Configuration



Top View

6. IT8673F Pin Descriptions

Table 6-1. Signal Names (by pin numbers in alphabetical order)

Pin(s) No.	Signal	I/O	Power	Description
Supplies				
35, 67, 121	**VCC**	PWR	-	***+5V Digital Power Supply.***
99	**VCCH**	PWR	-	***+5V VCC Help Supply.***
97	**VBAT**	PWR	-	***+3.3V Battery Supply.***
4,10,43, 77, 104	**GNDD**	GND	-	***Digital Ground.***
ISA Bus Interface Signals				
21-32	**SA[0:11]**	DI	VCC	***ISA Address 0 - 11.*** Input signals used to determine which internal register is accessed. SA0-SA11 are ignored during a DMA access.
96	**SA15/ FAN_CTL3**	DI/ DOD8	VCCH	***ISA Address 15 / FAN Control Output 3.*** • The default function of this pin is ISA address 15. • The second function of this pin is the **FAN** Control Output 3. • The function of this pin is decided by the power-on strapping of DTR1#.
95	**SA14/ FAN_TAC3**	DI/DI	VCCH	***ISA Address 14 / FAN Tachometer Input 3.*** • The default function of this pin is ISA address 14. • The second function of this pin is the **FAN** Tachometer Input 3. (0 to +5V amplitude **FAN** tachometer input). • The function of this pin is decided by the power-on strapping of RTS1#.
92-91	**SA[13:12]**	DI	VCCH	***ISA Address 13 - 12.*** Input signals used to determine which internal register is accessed. SA13-SA12 are ignored during a DMA access.
39 - 42, 44 - 47	**SD[0:7]**	DIO24	VCC	***ISA Data 0 - 7.*** 8-bit bi-directional data lines used to transfer data between IT8673F and the CPU or DMA controller. SD0 is the LSB and SD7 is the MSB.
118	**AEN**	DI	VCC	***Address Enable***. AEN is used to disable the internal address decoder when it is high. This pin is always ignored during DMA accesses.
74 - 76	**DRQ[1:3]**	DO8	VCC	***DMA Request 1 - 3.*** Active high outputs to signal the DMA controller that a data transfer from IT8673F is required.
87 – 89	**DACK[1:3]#**	DI	VCCH	***DMA Acknowledge 1 - 3 #.*** Active low inputs to acknowledge the corresponding DMA requests and enable the RD or WR signals during a DMA access cycle.
36	**PCICLK**	DI	VCC	***PCI Clock***. the PCI CLOCK input.
34	**SIRQ**	DIO24	VCC	***Serial Interrupt***.
119	**RESET**	DI	VCC	***Reset***. A high level on this input resets IT8673F. This signal asynchronously terminates any activity and places the device in the Disable state.
37	**IOR#**	DI	VCC	***I/O Read #***. Active low input asserted by the CPU or DMA controller to read data or status information from IT8673F.
120	**TC**	DI	VCC	***Terminal Count***. This input is asserted by the DMA controller to indicate the end of a DMA transfer. The signal is only effective during a DMA access cycle.
38	**IOW#**	DI	VCC	***I/O Write #.*** Active low input asserted by the CPU or DMA controller to write data or control information to IT8673F.
33	**IOCHRDY**	DOD24	VCC	***I/O Channel Ready.*** Pulled low to extend the Read/Write command under the EPP mode.

Pin(s) No.	Signal	I/O	Power	Description
FAN Speed Controller Signals				
65	**FAN_CTL1**	DOD8	VCC	***FAN Control Output 1.*** (PWM output signal to **FAN**'s FET.)
72	**FAN_CTL2/ GP13**	DOD8/ DIOD8	VCC	***FAN Control Output 2 / General Purpose I/O 13.*** • The default function of this pin is **FAN** Control Output 2 (PWM output signal to **FAN**'s FET). • The second function of this pin is the GP13. • The function configuration of this pin is decided by the GPIO configuration registers.
64	**FAN_TAC1**	DI	VCC	***FAN Tachometer Input 1.*** (0 to +5V amplitude **FAN** tachometer input)
73	**FAN_TAC2/ GP12**	DI/ DIOD8	VCC	***FAN Tachometer Input 2 / General Purpose I/O 12.*** • The default function of this pin is **FAN** Tachometer Input 2. (0 to +5V amplitude **FAN** tachometer input) • The second function of this pin is the GP12. • The function configuration of this pin is decided by the GPIO configuration registers.
Serial Port 1 Signals				
52	**CTS1#**	DI	VCC	***Clear to Send 1 #.*** When low, indicates that the MODEM or Data Set is ready to accept data. The CTS# signal is a MODEM status input whose condition can be tested by reading the MSR register.
55	**DCD1#**	DI	VCC	***Data Carrier Detect 1 #.*** When low, indicates that the MODEM or Data Set has detected a carrier. The DCD# signal is a MODEM status input whose condition can be tested by reading the MSR register.
50	**DSR1#**	DI	VCC	***Data Set Ready 1 #.*** When low, indicates that the MODEM or Data Set is ready to establish a communications link. The DSR# signal is a MODEM status input whose condition can be tested by reading the MSR register.
53	**DTR1#/ PIN96SEL**	DO8/DI	VCC	***Data Terminal Ready 1 # / Pin 96 Multiplex Select .*** • The default function of this pin is Data Terminal Ready 1 #. The DTR# signal is used to indicate to the MODEM or Data Set that the device is ready to exchange data. DTR# is activated by setting the appropriate bit in the MCR register to 1. After a Master Reset operation or during Loop mode, DTR# is set to its inactive state. • The second function of this pin is the power-on strapping of Pin 96 multiplex select. When high, the pin 96 is selected as SA15. This pin is weak pull-up internally.
54	**RI1#**	DI	VCC	***Ring Indicator 1 #.*** When low, indicates that a telephone ring signal has been received by the MODEM. The RI# signal is a MODEM status input whose condition can be tested by reading the MSR register.
51	**RTS1#/ PIN95SEL**	DO8/DI	VCC	***Request to Send 1 # / Pin 95 Multiplex Select.*** • The default function of this pin is Request To Send 1 #. When low, this output indicates to the MODEM or Data Set that the device is ready to send data. RTS# is activated by setting the appropriate bit in the MCR register to 1. After a Master Reset operation or during Loop mode, RTS# is set to its inactive state. • The second function of this pin is the power-on strapping of Pin 95 multiplex select. When high, the pin 95 is selected as SA14. This pin is weak pull-up internally.
48	**SIN1**	DI	VCC	***Serial Data In 1.*** This input receives serial data from the communications link.

Pin(s) No.	Signal	I/O	Power	Description
49	**SOUT1**	DO8	VCC	• ***Serial Data Out 1.*** This output sends serial data to the communications link. This signal is set to a marking state (logic 1) after a Master Reset operation or when the device is in one of the Infrared communications modes.
Serial Port 2 Signals				
62	**CTS2#**	DI	VCC	***Clear to Send 2 #.*** When low, indicates that the MODEM or Data Set is ready to accept data. The CTS# signal is a MODEM status input whose condition can be tested by reading the MSR register.
57	**DCD2#**	DI	VCC	***Data Carrier Detect 2 # .*** When low, indicates that the MODEM or Data Set has detected a carrier. The DCD# signal is a MODEM status input whose condition can be tested by reading the MSR register.
60	**DSR2#**	DI	VCC	***Data Set Ready 2 #.*** When low, indicates that the MODEM or Data Set is ready to establish a communications link. The DSR# signal is a MODEM status input whose condition can be tested by reading the MSR register.
63	**DTR2#/ KBCEN**	DO8/DI	VCC	***Data Terminal Ready 2 # / KBC Enable.*** • The default function of this pin is Data Terminal Ready 2 #. DTR# is used to indicate to the MODEM or Data Set that the device is ready to exchange data. DTR# is activated by setting the appropriate bit in the MCR register to 1. After a Master Reset operation or during Loop mode, DTR# is set to its inactive state. • The second function of this pin is the power-on strapping of KBC (LDN 4) enable. This pin is weak pull-up internally.
56	**RI2#**	DI	VCC	***Ring Indicator 2 #.*** When low, indicates that a telephone ring signal has been received by the MODEM. The RI# signal is a MODEM status input whose condition can be tested by reading the MSR register.
61	**RTS2#/ KBC_IROM**	DO8/DI	VCC	***Request to Send 2 # / KBC Internal ROM Selected*** • The default function of this pin is Request To Send 2 #. When low, this output indicates to the MODEM or Data Set that the device is ready to send data. RTS# is activated by setting the appropriate bit in the MCR register to 1. After a Master Reset operation or during Loop mode, RTS# is set to its inactive state. • The second function of this pin is the power-on strapping of KBC intrusion ROM select. When high (default), the internal ROM is selected. When low, the external ROM is selected. This pin is weak pull-up internally.
58	**SIN2**	DI	VCC	***Serial Data In 2.*** This input receives serial data from the communications link.
59	**SOUT2**	DO8	VCC	***Serial Data Out 2.*** This output sends serial data to the communications link. This signal is set to a marking state (logic 1) after a Master Reset operation or when the device is in one of the Infrared communications modes.
Parallel Port Signals				
100	**SLCT**	DI	VCC	***Printer Select.*** This signal goes high when the line printer has been selected.
101	**PE**	DI	VCC	***Printer Paper End.*** This signal is set high by the printer when it runs out of paper.
102	**BUSY**	DI	VCC	***Printer Busy.*** This signal goes high when the line printer has a local operation in progress and cannot accept data.
103	**ACK#**	DI	VCC	***Printer Acknowledge #.*** This signal goes low to indicate that the printer has already received a character and is ready to accept another.

Pin(s) No.	Signal	I/O	Power	Description
112 - 105	**PD[0:7]**	DIO24	VCC	***Parallel Port Data Bus 0-7.*** This bus provides a byte-wide input or output to the system. The eight lines are held in a high impedance state when the port is deselected.
113	**SLIN#**	DIO24	VCC	***Printer Select Input #.*** When low, the printer is selected. This signal is derived from the complement of bit 3 of the printer control register.
114	**INIT#**	DIO24	VCC	***Printer Initialize #,*** active low. This signal is derived from bit 2 of the printer control register, and is used to initialize the printer.
115	**ERR#**	DI	VCC	***Printer Error #,*** when active low it indicates that the printer has encountered an error. The error message can be read from bit 3 of the printer status register.
116	**AFD#**	DIO24	VCC	***Printer AutoLline feed #,*** active low. This signal is derived from the complement of bit 1 of the printer control register, and is used to advance one line after each line is printed.
117	**STB#**	DIO24	VCC	***Printer Strobe #,*** active low. This signal is the complement of bit 0 of the printer control register, and is used to strobe the printing data into the printer.
Floppy Disk Controller Signals				
5	**DENSEL#**	DO40	VCC	***Density Select #.*** DENSEL# is high for high data rates (500Kbps, 1Mbps). DENSEL# is low for low data rates (250Kbps, 300Kbps)
6	**MOTEA#**	DO40	VCC	***FDD Motor A Enable #.*** Active low.
7	**DRVB#**	DO40	VCC	***FDD Drive B Enable #.*** Active low.
8	**DRVA#**	DO40	VCC	***FDD Drive A Enable #.*** Active low.
9	**MOTEB#**	DO40	VCC	***FDD Motor B Enable #.*** Active low.
11	**DIR#**	DO40	VCC	***FDC Head Direction #.*** Step in when low, step out when high during a SEEK operation.
12	**STEP#**	DO40	VCC	***FDC Step Pulse #.*** Active low.
13	**WDATA#**	DO40	VCC	***FDC Write Serial Data to the drive #.*** Active low.
14	**WGATE#**	DO40	VCC	***FDC Write Gate Enable #.*** Active low.
15	**SIDE1#**	DO40	VCC	***Floppy Disk Side 1 Select #.*** Active low.
16	**INDEX#**	DI	VCC	***FDC Index #.*** Active low. Indicates the beginning of a disk track.
17	**TK00#**	DI	VCC	***Floppy Disk Track 0 #.*** Active low. Indicates that the head of the selected drive is on track 0.
18	**WPT#**	DI	VCC	***FDD Write Protect #.*** Active low. Indicates that the disk of the selected drive is write-protected.
19	**RDATA#**	DI	VCC	***FDC Read Disk Data #.*** Active low, serial data input from FDD
20	**DSKCHG#**	DI	VCC	***Floppy Disk Change #.*** Active low. This is an input pin that senses whether the drive door has been opened or a diskette has been changed.
Keyboard Controller Signals				
79	**KDAT**	DIOD16	VCCH	***Keyboard Data.***
80	**KCLK**	DIOD16	VCCH	***Keyboard Clock.***
81	**MDAT**	DIOD16	VCCH	***PS/2 Mouse Data.***
82	**MCLK**	DIOD16	VCCH	***PS/2 Mouse Clock.***
83	**KRST#**	DOD8	VCCH	***Keyboard Reset #.***
86	**GA20**	DOD8	VCCH	***Gate Address 20.***

Pin(s) No.	Signal	I/O	Power	Description
Infrared Controller Signals				
85	**IRTX**	DO16	VCCH	***Infrared Data Transmit.*** Infrared Data Transmit.
84	**IRRX**	DI	VCCH	***Infrared Data Receive.*** Infrared Data Receive Low.
Miscellaneous Signals				
78	**CLKIN**	DI	VCCH	***24 MHz or 48 MHz Clock Input.***
66	**GP10**	DIOD8	VCC	***General Purpose I/O 10***
68 – 71	**GP[17:14]**	DIOD8	VCC	***General Purpose I/O 17 - 14***
98	**COPEN#**	DOD8	VCCH or VBAT	***Case Open Detection #.*** The Case Open input is connected to a low power CMOS Flip-Flop, which is especially designed to support the case open state by the battery during power loss state.
93	**PWRON#/ PME#**	DOD8/ DOD8	VCCH	***Power On Switch Output #/ Power Management Event #.*** • The first function of this pin is the Main power On-Off switch Output # (Bug fix for PIIX40). • The second function of this pin is the power management event #. It supports the PCI PME# interface. This signal allows the peripheral to request the system to wake up from D3 (cold) state. This pin is backed by VTR. • The function configuration of this pin is decided by the software configuration registers.
94	**PANSWH#**	DI	VCCH	***Panel Switch Input #.*** Main power On-Off switch Input. (Bug fix for PIIX4)
90	**PSON/GP11**	DOD8/ DIOD8	VCCH	***Power Supply On Output / General Purpose I/O 11.*** • The default function of this pin is Main power supply On Output. (Bug fix for PIIX4) • The second function of this pin is the GP11. • The function configuration of this pin is decided by the GPIO configuration registers.
1 – 3, 133 – 128	**NC**	--	VCC	• ***No Connection.***

IO Cell:

DO8: 8mA Digital output buffer
DO16: 16mA Digital output buffer
DO40: 48mA Digital output buffer

DOD8: 8mA Digital Open-Drain output buffer
DOD24: 24mA Digital Open-Drain output buffer

DIO24: 24mA Digital Input/Output buffer

DIOD8: 8mA Digital Open-Drain Input/Output buffer
DIOD16: 16mA Digital Open-Drain Input/Output buffer

DI: Digital Input

7. Special Pin Routings

PSB - Power Supply Bypass
The PSB will be internally routed to PSON pin.

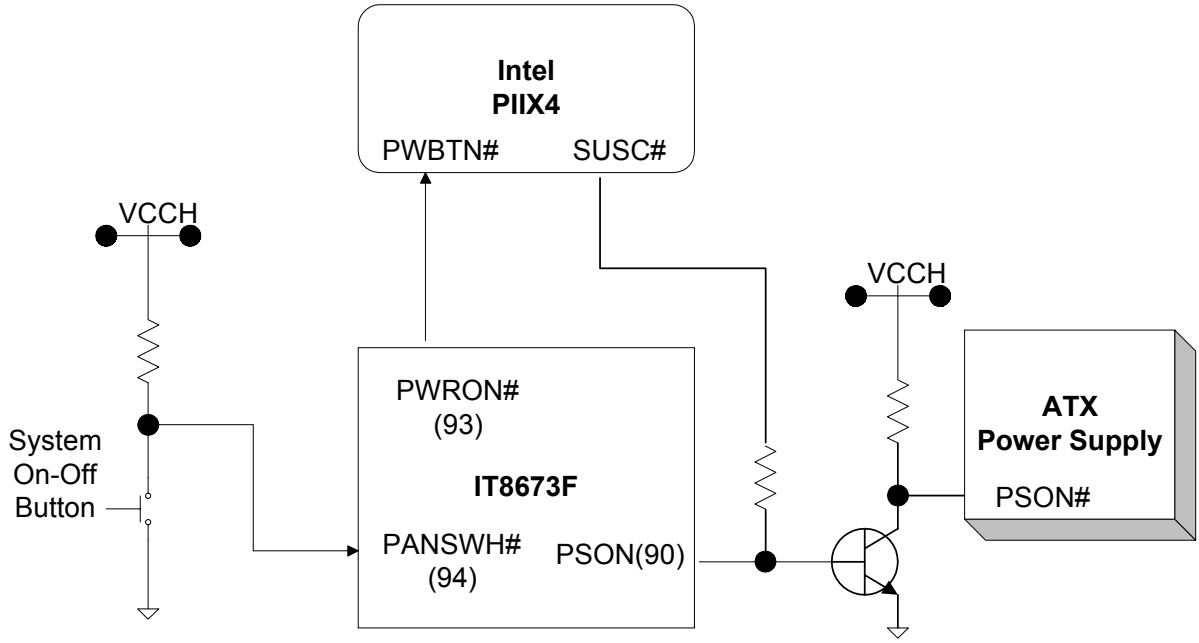


Figure 7-1. IT8673F Special Applications Circuitry for Intel PIIX4

8. List of GPIO Pins

Table 8-1. General Purpose I/O

Pin(s) No.	Signal	Description
66	GP10	General Purpose I/O 10.
90	PSON/GP11	Power Supply On Output / General Purpose I/O 11.
73	FAN_TAC2/GP12	FAN Tachometer Input 2 / General Purpose I/O 12.
72	FAN_CTL2/GP13	FAN Control Output 2 / General Purpose I/O 13.
71	GP14	General Purpose I/O 14.
70	GP15	General Purpose I/O 15.
69	GP16	General Purpose I/O 16.
68	GP17	General Purpose I/O 17.

9. Power On Strapping Options

Table 9-1. Power On Strapping

Pin No.	Signal	Value	Description
51	PIN95SEL	1	The function of the pin 95 is selected SA14. (default)
		0	The function of the pin 95 is selected FAN_TAC3.
53	PIN96SEL	1	The function of the pin 96 is selected SA15. (default)
		0	The function of the pin 96 is selected FAN_CTL3.
61	KBC_IROM	1	KBC's ROM is built in. (default)
		0	KBC's ROM is external. This is used for custom code verification. A special application circuit is required.
63	KBCEN	1	KBC is enabled. (default)
		0	KBC is disabled.

10. Configuration

10.1 Configuring Sequence Description

After the hardware reset or power-on reset, IT8673F enters the normal mode with all logical devices disabled except KBC. The initial state (enable bit) of this logical device (KBC) is determined by the state of pin 63 (DTR2#) at the falling edge of the system reset during power-on reset.

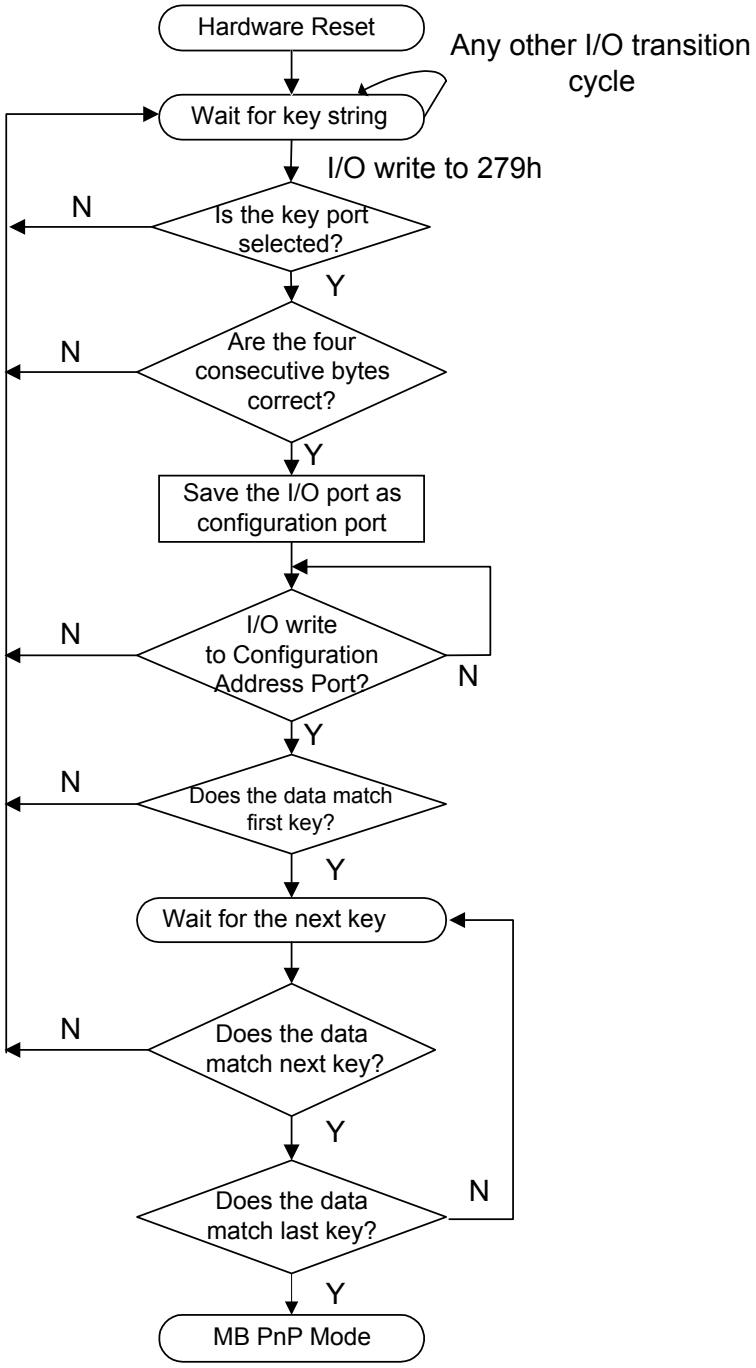


Figure 10-1. Configuration Sequence Flow Chart

There are three steps to completing configuration setup: (1) Enter the MB PnP Mode; (2) Modify the data of configuration registers; (3) Exit the MB PnP Mode. Without normal exiting, it may cause undesired results.

(1) Enter the MB PnP Mode

To enter the MB PnP Mode, 36 special I/O write operations are to be performed during Wait for Key state. To insure the initial state of the key-check logic, it is first necessary to perform two write operations to the Address port (279h) of the ISA PnP.

The Entering Key includes two steps. In the first step, four bytes are used to determine the I/O address and data port of configuration register. In the second step, 32 bytes are written to the Address port determined by the first four bytes. All 36 bytes must be written properly and sequentially. The corresponding sequential data for the first four bytes are as follows:

		Address port	Data port
	86h, 80h, 55h, 55h;	3F0h	3F1h
or	86h, 80h, 55h, AAh;	3BDh	3BFh
or	86h, 80h, AAh, 55h;	370h	371h

The sequential data for the other 32 bytes (same as the initial key of ISA PnP, but written to different I/O ports) are listed below in hexadecimal numeration:

6A, B5, DA, ED, F6, FB, 7D, BE,
DF, 6F, 37, 1B, 0D, 86, C3, 61,
B0, 58, 2C, 16, 8B, 45, A2, D1,
E8, 74, 3A, 9D, CE, E7, 73, 39,

(2) Modify the Data of the Registers

All configuration registers can be accessed after entering the MB PnP Mode. Before accessing a selected register, the content of Index 07h must be changed to the LDN to which the register belongs.

(3) Exit the MB PnP Mode

Set bit 1 of the configure control register (Index 02h) to “1” to exit the MB PnP Mode.

10.2 Description of the Configuration Registers

All the registers except APC/PME# registers will be reset to the default state when RESET is activated.

Table 10-1. Global Configuration Registers

LDN	Index	R/W	Reset	Configuration Register or Action
All	02h	W	NA	Configure Control
All	07h	R/W	NA	Logical Device Number (LDN)
All	20h	R	86h	Chip ID Byte 1
All	21h	R	73h	Chip ID Byte 2
All	22h	R	01h	Chip Version
All	23h	R/W	00h	Clock Selection Register
All	24h	R/W	00h	Software Suspend
07h[*1]	25h	R/W	00h	GPIO Multi-Function Pin Selection Register
07h[*1]	26h	R/W	00h	Reserved
07h[*1]	27h	R/W	00h	Reserved
07h[*1]	28h	R/W	00h	Reserved
07h[*1]	29h	R/W	00h	Reserved
F4h[*1]	2Eh	R/W	00h	Test 1 Register
F4h[*1]	2Fh	R/W	00h	Test 2 Register

Table 10-2. FDC Configuration Registers

LDN	Index	R/W	Reset	Configuration Register or Action
00h	30h	R/W	00h	FDC Activate
00h	60h	R/W	03h	FDC Base Address MSB Register
00h	61h	R/W	F0h	FDC Base Address LSB Register
00h	70h	R/W	06h	FDC Interrupt Level Select
00h	74h	R/W	02h	FDC DMA Channel Select
00h	F0h	R/W	00h	FDC Special Configuration Register

Table 10-3. Serial Port 1 Configuration Registers

LDN	Index	R/W	Reset	Configuration Register or Action
01h	30h	R/W	00h	Serial Port 1 Activate
01h	60h	R/W	03h	Serial Port 1 Base Address MSB Register
01h	61h	R/W	F8h	Serial Port 1 Base Address LSB Register
01h	70h	R/W	04h	Serial Port 1 Interrupt Level Select
01h	F0h	R/W	00h	Serial Port 1 Special Configuration Register

Table 10-4. Serial Port 2 Configuration Registers

LDN	Index	R/W	Reset	Configuration Register or Action
02h	30h	R/W	00h	Serial Port 2 Activate
02h	60h	R/W	02h	Serial Port 2 Base Address MSB Register
02h	61h	R/W	F8h	Serial Port 2 Base Address LSB Register
02h	62h	R/W	03h	Consumer IR Base Address MSB Register
02h	63h	R/W	00h	Consumer IR Base Address LSB Register
02h	70h	R/W	03h	Serial Port 2 Interrupt Level Select
02h	72h	R/W	00h	Consumer IR Interrupt Level Select
02h	F0h	R/W	00h	Serial Port 2 Special Configuration Register 1
02h	F1h	R/W	40h	Serial Port 2 Special Configuration Register 2

Table 10-5. Parallel Port Configuration Registers

LDN	Index	R/W	Reset	Configuration Register or Action
03h	30h	R/W	00h	Parallel Port Activate
03h	60h	R/W	03h	Parallel Port Primary Base Address MSB Register
03h	61h	R/W	78h	Parallel Port Primary Base Address LSB Register
03h	62h	R/W	07h	Parallel Port Secondary Base Address MSB Register
03h	63h	R/W	78h	Parallel Port Secondary Base Address LSB Register
03h	70h	R/W	07h	Parallel Port Interrupt Level Select
03h	74h	R/W	03h	Parallel Port DMA Channel Select[*2]
03h	F0h	R/W	03h[*3]	Parallel Port Special Configuration Register

Table 10-6. FAN Controller Configuration Registers

LDN	Index	R/W	Reset	Configuration Register or Action
04h	30h	R/W	00h	FAN Controller Activate
04h	60h	R/W	00h	FAN Controller Base Address MSB Register
04h	61h	R/W	80h	FAN Controller Base Address LSB Register
04h	62h	R/W	02h	PME# Direct Access Base Address MSB Register
04h	63h	R/W	00h	PME# Direct Access Base Address LSB Register
04h	70h	R/W	09h	FAN Controller Interrupt Level Select
04h	F0h	R/W	00h	APC/PME# Event Enable Register
04h	F1h	R/W	00h	APC/PME# Status Register
04h	F2h	R/W	00h	APC/PME# Control Register 1
04h	F3h	R/W	00h	FAN Controller Special Configuration Register
04h	F4h	R-R/W	00h	APC/PME# Control Register 2
04h	F5h	R/W		APC/PME# Special Code Index Register
04h	F6h	R/W		APC/PME# Special Code Data Register

Table 10-7. KBC(Keyboard) Configuration Registers

LDN	Index	R/W	Reset	Configuration Register or Action
05h	30h	R/W	*4	KBC Activate
05h	60h	R/W	00h	KBC Data Base Address MSB Register
05h	61h	R/W	60h	KBC Data Base Address LSB Register
05h	62h	R/W	00h	KBC Command Base Address MSB Register
05h	63h	R/W	64h	KBC Command Base Address LSB Register
05h	70h	R/W	01h	KBC Interrupt Level Select
05h	71h	R-R/W	02h	KBC Interrupt Type[*5]
05h	F0h	R/W	00h	KBC Special Configuration Register

Table 10-8. KBC(Mouse) Configuration Registers

LDN	Index	R/W	Reset	Configuration Register or Action
06h	30h	R/W	00h	KBC (Mouse) Activate
06h	70h	R/W	0Ch	KBC (Mouse) Interrupt Level Select
06h	71h	R-R/W	02h	KBC (Mouse) Interrupt Type[*5]
06h	F0h	R/W	00h	KBC (Mouse) Special Configuration Register

Table 10-9. GPIO Configuration Registers

LDN	Index	R/W	Reset	Configuration Register or Action
07h	60h	R/W	00h	CS0 Base Address MSB Register
07h	61h	R/W	00h	CS0 Base Address LSB Register
07h	62h	R/W	00h	CS1 Base Address MSB Register
07h	63h	R/W	00h	CS1 Base Address LSB Register
07h	64h	R/W	00h	CS2 Base Address MSB Register
07h	65h	R/W	00h	CS2 Base Address LSB Register
07h	66h	R/W	00h	Simple I/O Base Address MSB Register
07h	67h	R/W	00h	Simple I/O Base Address LSB Register
07h	68h	R/W	00h	Panel Button De-bounce Base Address MSB Register
07h	69h	R/W	00h	Panel Button De-bounce Base Address LSB Register
07h	70h	R/W	00h	GP IRQ Steering 1 Control Register
07h	71h	R/W	00h	GP IRQ Steering 1 Pin Mapping Register
07h	72h	R/W	00h	GP IRQ Steering 2 Control Register
07h	73h	R/W	00h	GP IRQ Steering 2 Pin Mapping Register
07h	F0h	R/W	00h	GP Set Selection Register
07h	F1h	R/W	00h	CSX Pin Mapping Register
07h	F2h	R/W	00h	CSX Control Register
07h	F3h	R/W	00h	GPIO Pin Polarity Register
07h	F4h	R/W	00h	GPIO Pin Internal Pull-up Enable Register

Table 10-9. GPIO & Alternate Function Configuration Registers (cont'd)

LDN	Index	R/W	Reset	Configuration Register or Action
07h	F5h	R/W	00h	Simple I/O Enable Register
07h	F6h	R/W	00h	Simple I/O Direction Selection Register
07h	F7h	R/W	00h	Panel Button De-bounce Enable Register
07h	F8h	R/W	00h	Panel Button De-bounce Control Register / GP LED Blinking 2 Control Register
07h	F9h	R/W	00h	Keyboard Lock Pin Mapping Register
07h	FAh	R/W	00h	GP LED Blinking 1 Pin Mapping Register
07h	FBh	R/W	00h	GP LED Blinking Control & RING# Pin Mapping Register
07h	FCh	R/W	00h	GP LED Blinking 2 Pin Mapping Register
07h	FDh	R/W	00h	Reserved Register
07h	FEh	R/W	00h	PCI CLKRUN# Pin Mapping Register
07h	FFh	R/W	00h	SMI# Pin Mapping Register
07h	E0h	R/W	00h	SMI# Control Register 1
07h	E1h	R/W	00h	SMI# Control Register 2
07h	E2h	R	00h	SMI# Status Register 1
07h	E3h	R-R/W	00h	SMI# Status Register 2

Notes:

*1: All these registers can be read from all LDNs.

*2: When the ECP mode is not enabled, this register is **read only** as "04h", and cannot be written.

*3: When bit 2 of the base address of Parallel Port is set to 1, the EPP mode cannot be enabled. Bit 0 of this register is always 0.

*4: The initial value of the activate bit of KBC is determined by the latched state of DTR2# at the falling edge of the RESET signal.

*5: These registers are **read only** unless the write enable bit (Index=F0h) is asserted.

10.2.1 Logical Device Base Address

The base I/O range of logical devices shown below is located in the base I/O address range of each logical device.

Table 10-10. Base Address of Logical Devices

Logical Devices	Address	Notes
LDN=0 FDC	Base + (2-5) and +7	
LDN=1 SERIAL PORT 1	Base + (0-7)	
LDN=2 SERIAL PORT 2	Base1 + (0-7) Base2 + (0-7)	COM port CIR
LDN=3 PARALLEL PORT	Base1 + (0-3) Base1 + (0-7) Base1 + (0-3) and Base2 + (0-3) Base1 + (0-7) and Base2 + (0-3)	SPP SPP+EPP SPP+ECP SPP+EPP+ECP
LDN=4 FAN Controller	Base1 + (0-7) Base2 + (0-3)	FAN Controller (FAN) PME#
LDN=5 KBC	Base1 + Base2	KBC

10.3 Global Configuration Registers (LDN: All)

10.3.1 Configure Control (Index=02h)

This register is **write only**. Its values are not sticky; that is to say, a hardware reset will automatically clear the bits, and does not require the software to clear them.

Bit	Description
7-2	Reserved
1	Returns to the "Wait for Key" state. This bit is used when configuration sequence is completed.
0	Resets all logical devices and restores configuration registers to their power-on states.

10.3.2 Logical Device Number (LDN, Index=07h)

This register is used to select the current logical devices. By reading from or writing to the configuration of I/O, Interrupt, DMA and other special functions, all registers of the logical devices can be accessed. In addition, ACTIVATE command is only effective for the selected logical devices. This register is **read/write**.

10.3.3 Chip ID Byte 1 (Index=20h, Default=86h)

This register is the Chip ID Byte 1 and is **read only**. Bits [7:0]=86h when read.

10.3.4 Chip ID Byte 2 (Index=21h, Default=73h)

This register is the Chip ID Byte 2 and for **read only**. Bits [7:0]=73h when read.

10.3.5 Chip Version (Index=22h, Default=01h)

This register is the Chip Version and for **read only**.

10.3.6 Clock Selection Register (Index=23h, Default=00h)

Bit	Description
7-1	Reserved
0	CLKIN frequency. 1: 48 MHz. 0: 24 MHz.

10.3.7 Software Suspend (Index=24h, Default=00h, MB PnP)

This register is the Software Suspend register. When bit 0 is set, IT8673F enters the "Software Suspend" state. All the devices, except KBC, remain inactive until this bit is cleared or when the wake-up event occurs. The wake-up event occurs at any transition on signals RI1# (pin 54) and RI2# (pin 56).

10.3.8 GPIO Multi-Function Pin Selection Register (Index=25h, Default=00h)

If the enabled bits are not set, the multi-function pins will perform the original functions. On the other hand, if they are set, they will perform the GPIO functions. This register can be read from any LDN, but can only be written if LDN=07h.

Bit	Description
7	Selects the GPIO function of General Purpose I/O 17 (GP17) of pin 68.
6	Selects the GPIO function of General Purpose I/O 16 (GP16) of pin 69.
5	Selects the GPIO function of General Purpose I/O 15 (GP15) of pin 70.
4	Selects the GPIO function of General Purpose I/O 14 of pin 71.
3	Performs the function selection of FAN_CTL2 or GP 13 of pin 72. 1: Selects the function of General Purpose I/O 13 (GP13). 0: Selects the function of FAN Control Output 2 (FAN_CTL2).
2	Performs the function selection of FAN_TAC2 or GP 12 of pin 73. 1: Selects the function of General Purpose I/O 12 (GP12). 0: Selects the function of FAN Tachometer Input 2 (FAN_TAC2).
1	Performs the function selection of PSON or GP 11 of pin 90. 1: Selects the function of General Purpose I/O 11 (GP11). 0: Selects the function of Power Supply On Output (PSON).
0	Selects the GPIO function of General Purpose I/O 10 (GP10) of pin 66.

10.3.9 Reserved Register (Index=26h, Default=00h)

10.3.10 Reserved Register (Index=27h, Default=00h)

10.3.11 Reserved Register (Index=28h, Default=00h)

10.3.12 Reserved Register (Index=29h, Default=00h)

10.3.13 Test 1 Register (Index=2Eh, Default=00h)

This register is the Test 1 Register and is reserved for ITE. It should not be set.

10.3.14 Test 2 Register (Index=2Fh, Default=00h)

This register is the Test 2 Register and is reserved for ITE. It should not be set.

10.4 FDC Configuration Registers (LDN=00h)

10.4.1 FDC Activate (Index=30h, Default=00h)

Bit	Description
7-1	Reserved
0	FDC Enable. 1: Enabled. 0: Disabled.

10.4.2 FDC Base Address MSB Register (Index=60h, Default=03h)

Bit	Description
7-4	**Read only**, with "0h" for Base Address [15:12].
3-0	Mapped as Base Address [11:8].

10.4.3 FDC Base Address LSB Register (Index=61h, Default=F0h)

Bit	Description
7-3	**Read/write**, mapped as Base Address[7:3].
2-0	**Read only** as "000b".

10.4.4 FDC Interrupt Level Select (Index=70h, Default=06h)

Bit	Description
7-4	Reserved with default "0h".
3-0	Select the interrupt level [note1] for FDC.

10.4.5 FDC DMA Channel Select (Index=74h, Default=02h)

Bit	Description
7-3	Reserved with default "00h".
2-0	Select the DMA channel [note2] for FDC.

10.4.6 FDC Special Configuration Register (Index=F0h, Default=00h)

Bit	Description
7-4	Reserved with default "00h".
3	1 : IRQ sharing. 0 : Normal IRQ.
2	1 : Swap Floppy Drives A, B. 0 : Normal.
1	1 : 3-Mode. 0 : AT Mode.
0	1 : Software Write Protect. 0 : Normal.

10.5 Serial Port 1 Configuration Registers (LDN=01h)

10.5.1 Serial Port 1 Activate (Index=30h, Default=00h)

Bit	Description
7-1	Reserved
0	Serial Port 1 Enabled. 1: Enabled. 0: Disabled.

10.5.2 Serial Port 1 Base Address MSB Register (Index=60h, Default=03h)

Bit	Description
7-4	**Read only** as "0h" for Base Address[15:12].
3-0	**Read/write**, mapped as Base Address[11:8].

10.5.3 Serial Port 1 Base Address LSB Register (Index=61h, Default=F8h)

Bit	Description
7-3	**Read/write**, mapped as Base Address[7:3].
2-0	**Read only** as "000b".

10.5.4 Serial Port 1 Interrupt Level Select (Index=70h, Default=04h)

Bit	Description
7-4	Reserved with default "0h".
3-0	Select the interrupt level [note1] for Serial Port 1.

10.5.5 Serial Port 1 Special Configuration Register (Index=F0h, Default=00h)

Bit	Description
7-3	Reserved with default "00h".
2-1	Clock Source. 00: 24 MHz/13 (Standard) 01: 24 MHz/12 (MIDI) 10: Reserved 11: Reserved
0	1 : IRQ sharing. 0 : Normal.

10.6 Serial Port 2 Configuration Registers (LDN=02h)

10.6.1 Serial Port 2 Activate (Index=30h, Default=00h)

Bit	Description
7-1	Reserved
0	Serial Port 2 Enable. 1: Enabled. 0: Disabled.

10.6.2 Serial Port 2 Base Address MSB Register (Index=60h, Default=02h)

Bit	Description
7-4	**Read only** with "0h" for Base Address[15:12].
3-0	**Read/write**, mapped as Base Address[11:8].

10.6.3 Serial Port 2 Base Address LSB Register (Index=61h, Default=F8h)

Bit	Description
7-3	**Read/write**, mapped as Base Address[7:3].
2-0	**Read only** as "000b".

10.6.4 Consumer IR Base Address MSB Register (Index=62h, Default=03h)

Bit	Description
7-4	**Read only** with "0h" for Base Address[15:12].
3-0	**Read/write,** mapped as Base Address[11:8].

10.6.5 Consumer IR Base Address LSB Register (Index=63h, Default=00h)

Bit	Description
7-3	**Read/write**, mapped as Base Address[7:3].
2-0	**Read only** as "000b".

10.6.6 Serial Port 2 Interrupt Level Select (Index=70h, Default=03h)

Bit	Description
7-4	Reserved with default "0h".
3-0	Select the interrupt level [note1] for Serial Port 2.

10.6.7 Consumer IR Interrupt Level Select (Index=72h, Default=00h)

Bit	Description
7-4	Reserved with default "0h."
3-0	Select the interrupt level [note1] for Serial Port 2.

10.6.8 Serial Port 2 Special Configuration Register 1 (Index=F0h, Default=00h)

Bit	Description
7-3	Reserved with default "00h."
2-1	Clock Source. 00: 24 MHz/13 (Standard) 01: 24 MHz/12 (MIDI) 10: Reserved 11: Reserved
0	1 : IRQ sharing. 0 : Normal.

10.6.9 Serial Port 2 Special Configuration Register 2 (Index=F1h, Default=40h)

Bit	Description
7	1: No transmission delay (40 bits) when the SIR or ASKIR is changed from RX mode to TX mode. 0: Transmission delay (40 bits) when the SIR or ASKIR is changed from RX mode to TX mode.
6	1: No reception delay (40 bits) when the SIR or ASKIR is changed from TX mode to RX mode. 0: Reception delay (40 bits) when the SIR or ASKIR is changed from TX mode to RX mode.
5	Single Mask Mode: When set, the RX of UART is masked under TX transmission.
4	1 : Half Duplex. 0 : Full Duplex (default).
3	CIR enable.
2-0	IR Mode Select 000: Standard (default). 001: IrDA 1.0 (HP SIR). 010 : ASKIR. else : Reserved.

10.7 Parallel Port Configuration Registers (LDN=03h)

10.7.1 Parallel Port Activate (Index=30h, Default=00h)

Bit	Description
7-1	Reserved
0	Parallel Port Enabled. 1: Enabled. 0: Disabled.

10.7.2 Parallel Port Primary Base Address MSB Register (Index=60h, Default=03h)

Bit	Description
7-4	**Read only** as "0h" for Base Address[15:12].
3-0	**Read/write**, mapped as Base Address[11:8].

10.7.3 Parallel Port Primary Base Address LSB Register (Index=61h, Default=78h)

If bit 2 is set to 1, the EPP mode is disabled automatically.

Bit	Description
7-2	**Read/write**, mapped as Base Address[7:2].
1-0	**Read only** as "00b".

10.7.4 Parallel Port Secondary Base Address MSB Register (Index=62h, Default=07h)

Bit	Description
7-4	**Read only** as "0h" for Base Address[15:12].
3-0	**Read/write**, mapped as Base Address[11:8].

10.7.5 Parallel Port Secondary Base Address LSB Register (Index=63h, Default=78h)

Bit	Description
7-2	**Read/write**, mapped as Base Address[7:2].
1-0	**Read only** as "00b".

10.7.6 Parallel Port Interrupt Level Select (Index =70h, Default=07h)

Bit	Description
7-4	Reserved with default "0h".
3-0	Select the interrupt level [note1] for Parallel Port.

10.7.7 Parallel Port DMA Channel Select (Index=74h, Default=03h)

Bit	Description
7-3	Reserved with default "00h."
2-0	Select the DMA channel [note2] for Parallel Port.

10.7.8 Parallel Port Special Configuration Register (Index=F0h, Default=03h)

Bit	Description
7-3	Reserved
2	1 : IRQ sharing. 0 : Normal.
1-0	Parallel Port mode 00 : Standard Parallel Port mode (SPP) 01 : EPP mode 10 : ECP mode 11 : EPP mode and ECP mode

If bit 1 is set, ECP mode is enabled. If bit 0 is set, EPP mode is enabled. These two bits are independent. However, according to the EPP spec., when Parallel Port Primary Base Address bit 2 is set to 1, the EPP mode cannot be enabled.

10.8 FAN Controller Configuration Registers (LDN=04h)

10.8.1 FAN Controller Activate Register (Index=30h, Default=00h)

Bit	Description
7-1	Reserved
0	FAN Controller Enabled. 1: Enabled. 0: Disabled.

10.8.2 FAN Controller Base Address MSB Register (Index=60h, Default=00h)

Bit	Description
7-4	**Read only** as "0h" for Base Address[15:12].
3-0	**Read/write**, mapped as Base Address[11:8].

10.8.3 FAN Controller Base Address LSB Register (Index=61h, Default=80h)

Bit	Description
7-3	**Read/write**, mapped as Base Address[7:3].
2-0	**Read only** as "000b".

10.8.4 PME# Direct Access Base Address MSB Register (Index=62h, Default=02h)

Bit	Description
7-4	**Read only** as "0h" for Base Address[15:12].
3-0	**Read/write**, mapped as Base Address[11:8].

10.8.5 PME# Direct Access Base Address LSB Register (Index=63h, Default=00h)

Bit	Description
7-3	**Read/write**, mapped as Base Address[7:3].
2-0	**Read only** as "000b".

10.8.6 FAN Controller Interrupt Level Select (Index=70h, Default=09h)

Bit	Description
7-4	Reserved with default "0h".
3-0	Select the interrupt level [note1] for FAN Controller.

10.8.7 APC/PME# Event Enable Register (PER) (Index=F0h, Default=00h)

Bit	Description
7	It is set to 1 when VCCH is OFF. Writing 1 to clear this bit. This bit is ineffective if a 0 is written to this bit.
6	Reserved
5	RING# event enable. 1 : Enabled. 0 : Disabled.
4	PS/2 Mouse event enable. 1 : Enabled. 0 : Disabled.
3	Keyboard event enable. 1 : Enabled. 0 : Disabled.
2	RI2# event enable. 1 : Enabled. 0 : Disabled.
1	RI1# event enable. 1 : Enabled. 0 : Disabled.
0	Reserved

10.8.8 APC/PME# Status Register (PSR) (Index=F1h, Default=00h)

Bit	Description
7	It is set to 1 when VCC is ON at last AC power failure and 0 when VCC is OFF.
6	Reserved
5	RING# Event Detected.
4	PS/2 Mouse Event Detected.
3	Keyboard Event Detected.
2	RI2# Event Detected.
1	RI1# Event Detected.
0	Reserved

10.8.9 APC/PME# Control Register 1 (PCR 1) (Index=F2h, Default=00h)

Bit	Description
7	PER and PSR normal run access enable.
6	Reserved
5	This bit is restored automatically to the previous VCC state before power failure occurs.
4	Disables all APC events after the power failure occurs, excluding PANSWH#.
3	Keyboard event mode selection when VCC is ON. 1 : Determined by PCR 2. 0 : Pulse falling edge on KCLK.
2	Mouse event when VCC is OFF. 1 : Double click Key. 0 : Pulse falling edge on MCLK.
1	Mouse event when VCC is ON. 1 : Double click Key. 0 : Pulse falling edge on MCLK.
0	RING# Event Mode Selection. 1 : Pulse train mode. 0 : Pulse falling edge mode.

10.8.10 FAN Controller Special Configuration Register (Index=F3h, Default=00h)

Bit	Description
7-1	Reserved
0	1 : IRQ sharing. 0 : Normal.

10.8.11 APC/PME# Control Register 2 (PCR 2) (Index=F4h, Default=00h)

Bit	Description
7	Pin 93 function selection. 1: PME#. 0: APC PWRON#.
6	Reserved
5	PSON state when VCCH is switched from OFF to ON under VCC OFF state.
4	Masks PANSWH# power-on event.
3-2	Key Number of the Keyboard power-up event. 00: 5 (Key string mode), 3(Stroke keys at same time mode) 01: 4 (Key string mode), 2(Stroke keys at same time mode) 10: 3 (Key string mode), 1(Stroke keys at same time mode) 11: 2 (Key string mode), Reserved (Stroke keys at same time mode)
1-0	Keyboard power-up event mode selection. 00: KCLK falling edge 01: Key string mode 10: Stroke keys at same time mode 11: Reserved

10.8.12 APC/PME# Special Code Index Register (Index=F5h)

Bit	Description
7-6	Reserved (should be "00")
5-0	Indicate which Identification Key Code or CIR code register is to be read/written via 0xF6.

10.8.13 APC/PME# Special Code Data Register (Index=F6h)

There are 5 bytes for Key String mode, and 3 bytes for Stroke Keys at same time mode.

10.9 KBC (keyboard) Configuration Registers (LDN=05h)

10.9.1 KBC (keyboard) Activate (Index=30h, Default=01h or 00h)

Bit	Description
7-1	Reserved
0	KBC(Keyboard) Enable. 1: Enabled. 0: Disabled. This is a **read/write** register. The default value depends on the state of the DTR2# when RESET is activated. The default value is 1b for the High state of DTR2# when RESET is activated. It is 0b for the low state of DTR2# when RESET is activated.

10.9.2 KBC (keyboard) Data Base Address MSB Register (Index=60h, Default=00h)

Bit	Description
7-4	**Read only** as "0h" for Base Address [15:12].
3-0	**Read/write**, mapped as Base Address [11:8].

10.9.3 KBC (keyboard) Data Base Address LSB Register (Index=61h, Default=60h)

Bit	Description
7-0	**Read/write**, mapped as Base Address[7:0].

10.9.4 KBC (keyboard) Command Base Address MSB Register (Index=62h, Default=00h)

Bit	Description
7-4	**Read only** as "0h" for Base Address[15:12].
3-0	**Read/write**, mapped as Base Address[11:8].

10.9.5 KBC (keyboard) Command Base Address LSB Register (Index=63h, Default=64h)

Bit	Description
7-0	**Read/write**, mapped as Base Address[7:0].

10.9.6 KBC (keyboard) Interrupt Level Select (Index=70h, Default=01h)

Bit	Description
7-4	Reserved with default “0h”.
3-0	Select the interrupt level [note1] for KBC (keyboard).

10.9.7 KBC (keyboard) Interrupt Type (Index=71h, Default=02h)

This register indicates the type of interrupt set for KBC (keyboard) and is **read only** as “02h” when bit 1 of the KBC (keyboard) Special Configuration Register is cleared. If set, this type of interrupt can be selected as level or edge trigger.

Bit	Description
7-2	Reserved
1	1: High Level. 0: Low Level.
0	1: Level Type. 0: Edge Type.

10.9.8 KBC (keyboard) Special Configuration Register (Index=F0h, Default=00h)

Bit	Description
7	Reserved
6	Reserved
5	Reserved
4	1: IRQ sharing. 0: normal.
3	1:KBC’s clock 8 MHz. 0:KBC’s clock 12 MHz.
2	1: Key lock enabled. 0: Key lock disabled.
1	1: Type of interrupt of KBC (keyboard) can be changed. 0: Type of interrupt of KBC (keyboard) is fixed.
0	1: Enables the External Access ROM of 8042. 0: Internal built-in ROM is used.

10.10 KBC (mouse) Configuration Registers (LDN=06h)

10.10.1 KBC (mouse) Activate (Index=30h, Default=00h)

Bit	Description
7-1	Reserved
0	KBC (mouse) Enable. 1: Enabled. 0: Disabled.

10.10.2 KBC (mouse) Interrupt Level Select (Index=70h, Default=0Ch)

Bit	Description
7-4	Reserved with default “0h”.
3-0	Select the interrupt level [note1] for KBC (mouse).

10.10.3 KBC (mouse) Interrupt Type (Index=71h, Default=02h)

This register indicates the type of interrupt used for KBC (mouse) and is **read only** as "02h" when bit 0 of the KBC (mouse) Special Configuration Register is cleared. When bit 0 is set, the type of interrupt can be selected as level or edge trigger.

Bit	Description
7-2	Reserved
1	1: High Level. 0: Low Level.
0	1: Level Type. 0: Edge Type.

10.10.4 KBC (mouse) Special Configuration Register (Index=F0h, Default=00h)

Bit	Description
7-2	Reserved with default "00h."
1	1: IRQ sharing. 0: Normal.
0	1: Type of interrupt of KBC (mouse) can be changed. 0: Type of interrupt of KBC (mouse) is fixed.

10.11 GPIO Configuration Registers (LDN=07h)

10.11.1 CS0 Base Address MSB Register (Index=60h, Default=00h)

Bit	Description
7-4	**Read only** as "0h" for Base Address [15:12].
3-0	**Read/write**, mapped as Base Address [11:8].

10.11.2 CS0 Base Address LSB Register (Index=61h, Default=00h)

Bit	Description
7-0	**Read/write**, mapped as Base Address[7:0].

10.11.3 CS1 Base Address MSB Register (Index=62h, Default=00h)

Bit	Description
7-4	**Read only** as "0h" for Base Address [15:12].
3-0	**Read/write**, mapped as Base Address [11:8].

10.11.4 CS1 Base Address LSB Register (Index=63h, Default=00h)

Bit	Description
7-0	**Read/write**, mapped as Base Address[7:0].

10.11.5 CS2 Base Address MSB Register (Index=64h, Default=00h)

Bit	Description
7-4	**Read only** as "0h" for Base Address [15:12].
3-0	**Read/write**, mapped as Base Address [11:8].

10.11.6 CS2 Base Address LSB Register (Index=65h, Default=00h)

Bit	Description
7-0	**Read/write**, mapped as Base Address[7:0].

10.11.7 Simple I/O Base Address MSB Register (Index=66h, Default=00h)

Bit	Description
7-4	**Read only** as "0h" for Base Address[15:12].
3-0	**Read/write**, mapped as Base Address[11:8].

10.11.8 Simple I/O Base Address LSB Register (Index=67h, Default=00h)

Bit	Description
7-0	**Read/write**, mapped as Base Address[7:0].

10.11.9 Panel Button De-bounce Base Address MSB Register (Index=68h, Default=00h)

Bit	Description
7-4	**Read only** as "0h" for Base Address[15:12].
3-0	**Read/write**, mapped as Base Address[11:8].

10.11.10 Panel Button De-bounce Base Address LSB Register (Index=69h, Default=00h)

Bit	Description
7-0	**Read/write**, mapped as Base Address[7:0].

10.11.11 GP IRQ Steering 1 Control Register (Index=70h, Default=00h)

Bit	Description
7-4	Reserved
3-0	Select the interrupt level [note1] for GPIO.

10.11.12 GP IRQ Steering 1 Pin Mapping Register (Index=71h, Default=00h)

Bit	Description
7	Reserved
6	GP IRQ Steering 1 IRQ Sharing enable.
5-0	Please see Location mapping table [note3] on page 40.

10.11.13 GP IRQ Steering 2 Control Register (Index=72h, Default=00h)

Bit	Description
7-4	Reserved
3-0	Select the interrupt level [note1] for GPIO.

10.11.14 GP IRQ Steering 2 Pin Mapping Register (Index=73h, Default=00h)

Bit	Description
7	Reserved
6	GP IRQ Steering 1 IRQ Sharing enabled.
5-0	Please see Location mapping table [note3] on page 40.

10.11.15 GP Set Selection Register (Index=F0h, Default=00h)

This register is used to determine which set will be accessed by the later accessing of Index F1h, F2h. If accessing F3h, F4h, F5h, F6h, and F7h, this register should be fixed at 00h. Please refer to the Location mapping table [note3] on page 40.

10.11.16 CSX Pin Mapping Register (Index=F1h, Default=00h)

This register is used to determine CSX output pin mapping. Before accessing this register, the GP set selection register must be determined first (00h for CS0, 01h for CS1 and 02h for CS2).

Bit	Description
7-6	Reserved
5-0	Please see Location mapping table [note3] on page 40.

10.11.17 CSX Control Register (Index=F2h, Default=00h)

Before accessing this register, the GP set selection register must be determined first (00h for CS0, 01h for CS1 and 02h for CS2).

Bit	Description
7-6	Reserved
3-2	Base Address Alignment. 00 : single port 01 : 2 ports 10 : 4 ports 11 : 8 ports
1-0	Chip Select Type. 00 : Pure Address Decode 01 : Address Decode and IOR command 10 : Address Decode and IOW command 11 : Address Decode and (IOR or IOW command)

10.11.18 GPIO Pin Polarity Register (Index=F3h, Default=00h)

This register is used to program the GP pin type as polarity inverting or non-inverting. Before accessing this register, the GP set selection register must be fixed at 00h.

Bit	Description
7-0	For each bit 1: Inverting. 0: Non-inverting.

10.11.19 GPIO Pin Internal Pull-up Enable Register (Index=F4h, Default=00h)

Before accessing this register, the GP set selection register must be fixed at 00h.

Bit	Description
7-0	For each bit 1: Enabled. 0: Disabled.

10.11.20 Simple I/O Enable Register (Index=F5h, Default=00h)

This register is used to select the function as either the Simple I/O or the Alternate function. Before accessing this register, the GP set selection register must be fixed at 00h.

Bit	Description
7-0	For each bit 1: Simple I/O. 0: Alternate function.

10.11.21 Simple I/O Direction Selection Register (Index=F6h, Default=00h)

This register is used to determine the direction of the Simple I/O. Before accessing this register, the GP set selection register must be fixed at 00h.

Bit	Description
7-0	For each bit 1: Input mode. 0: Output mode.

10.11.22 Panel Button De-bounce Enable Register (Index=F7h, Default=00h)

Before accessing this register, the GP set selection register must be fixed at 00h.

Bit	Description
7-0	For each bit 1: Enabled. 0: Disabled.

10.11.23 Panel Button De-bounce Control Register/GP LED Blinking 2 Control Register (Index=F8h, Default=00h)

Bit	Description
7	GP LED 2 short low pulse enable.
6-5	GP LED 2 frequency Control. 00: 4 Hz. 01: 1 Hz. 10: 1/4 Hz. 11: 1/8 Hz.
4	GP LED 2 Output low enable.
3	IRQ output type. 0: Edge mode. 1: Level mode.
2	IRQ output enable. 0: Disabled. 1: Enabled.
1-0	De-bounce time selection. 00: 8 ms (6 ms ignored, 8 ms pass) 01: 16 ms (12 ms ignored, 16 ms pass) 10: 32 ms (24 ms ignored, 21 ms pass) 11: 64 ms (48 ms ignored, 64 ms pass)

10.11.24 Keyboard Lock Pin Mapping Register (Index=F9h, Default=00h)

Bit	Description
7-6	Reserved
5-0	Keyboard Lock Pin Location. Please see Location mapping table [note3] on page 40.

10.11.25 GP LED Blinking 1 Pin Mapping Register (Index=FAh, Default=00h)

Bit	Description
7-6	Reserved
5-0	GP LED Blinking Location. Please see Location mapping table note3 on page 40.

10.11.26 GP LED Blinking Control and RING# Pin Mapping Register (Index=FBh, Default=00h)

Bit	Description
7	Reserved
6-4	Location of RING#. 000 : GPIO10 010 : GPIO11 (Only this pin can work under VCCH power) 011 : GPIO12 100 : GPIO13 101 : GPIO14 110 : GPIO15 001 : GPIO16 111 : GPIO17
3	GP LED 1 short low pulse enable.
2-1	GP LED 1 frequency Control. 00: 4 Hz 01: 1 Hz 10: 1/4 Hz 11: 1/8 Hz
0	GP LED 1 Output low enabled.

10.11.27 GP LED Blinking 2 Pin Mapping Register (Index=FCh, Default=00h)

Bit	Description
7-6	Reserved
5-0	GP LED 2 Pin Location. Please see Location mapping table note3 on page 40.

10.11.28 Reserved Register (Index=FDh, Default=00h)

10.11.29 PCI CLKRUN# Pin Mapping Register (Index=FEh, Default=00h)

Bit	Description
7-6	Reserved
5-0	PCI CLKRUN# Pin Location. Please see Location mapping table note3 on page 40.

10.11.30 SMI# Pin Mapping Register (Index=FFh, Default=00h)

Bit	Description
7-6	Reserved
5-0	SMI# Pin Location. Please see Location mapping table [note3] on page 40.

10.11.31 SMI# Control Register 1 (Index=E0h, Default=00h)

Bit	Description
7	Enables the generation of an SMI# due to GP IRQ Steering 1's IRQ (EN_GPIRQ1).
6	Enables the generation of an SMI# due to KBC(PS/2 Mouse)'s IRQ (EN_MIRQ).
5	Enables the generation of an SMI# due to KBC(Keyboard)'s IRQ (EN_KIRQ).
4	Enables the generation of an SMI# due to FAN Controller's IRQ (EN_ECIRQ).
3	Enables the generation of an SMI# due to Parallel Port's IRQ (EN_PIRQ).
2	Enables the generation of an SMI# due to Serial Port 2's IRQ (EN_S2IRQ).
1	Enables the generation of an SMI# due to Serial Port 1's IRQ (EN_S1IRQ).
0	Enables the generation of an SMI# due to FDC's IRQ (EN_FIRQ).

10.11.32 SMI# Control Register 2 (Index=E1h, Default=00h)

Bit	Description
7	Forces to clear all the SMI# status register bits, non-sticky.
6	0: Edge trigger. 1: Level trigger.
5-2	Reserved
1	Enables the generation of an SMI# due to APC Switch Button(EN_BTN).
0	Enables the generation of an SMI# due to GP IRQ Steering 2's IRQ (EN_GPIRQ2).

10.11.33 SMI# Status Register 1 (Index=E2h, Default=00h)

This register is used to read the status of SMI# inputs.

Bit	Description
7	GP IRQ Steering 1's IRQ.
6	KBC(PS/2 Mouse)'s IRQ.
5	KBC(Keyboard)'s IRQ.
4	FAN Controller's IRQ.
3	Parallel Port's IRQ.
2	Serial Port 2's IRQ.
1	Serial Port 1's IRQ.
0	FDC's IRQ.

10.11.34 SMI# Status Register 2 (Index=E3h, Default=00h)

This register is used to read the status of SMI# inputs.

Bit	Description
7-2	Reserved
1	APC Switch Button.
0	GP IRQ Steering 2's IRQ.

Note1: Interrupt level mapping

Fh-Dh: not valid
Ch : IRQ12
.
.
3h : IRQ3
2h : not valid
1h : IRQ1
0h : no interrupt selected

Note2: DMA channel mapping

7h-5h : not valid
4h : no DMA channel selected
3h : DMA3
2h : DMA2
1h : DMA1
0h : not valid

Note3: The Location mapping

Location	Description
001 000	GPIO10 (pin 66).
001 001	GPIO11 (pin 90). Powered by VCCH.
001 010	GPIO12 (pin 73).
001 011	GPIO13 (pin 72).
001 100	GPIO14 (pin 71).
001 101	GPIO15 (pin 70).
001 110	GPIO16 (pin 69).
001 111	GPIO17 (pin 68).
else	Reserved

11. Functional Description

11.1 General Purpose I/O

IT8673F provides flexible I/O control and special functions for the system designers through a set of General Purpose I/O pins (GPIO). Some of GPIO pins are multi-functional. The GPIO functions will not be performed unless the related enable bits of the GPIO Multi-function Pin Selection register (Index 25h of Global Configuration Register) are set. GPIO function includes the simple I/O function and alternate function, and the function selection is determined by Simple I/O Enable Register (Index=F5h).

The Simple I/O function includes a set of registers, which correspond to the GPIO pins. The accessed I/O ports are programmable. Base Address is programmed on the GPIO Simple I/O Base Address LSB and MSB registers (LDN=07h, Index=66h and 67h).

The Alternate Function provides several special functions for users, including three chip select strobes (CS0, CS1, CS2), SMI# output routing, Interrupt steering, Panel Button De-bounce, Keyboard Lock input routing, LED Blinking, PCI CLKRUN# routing, and RING routing (sub-function of APC). All these functions can be programmed to all GPIO pins, except the RING# function.

The GP set selection register (Index=F0h) is used to determine the set X of the some registers (Index=F1h and F2h). Before these registers can be programmed, this register (Index=F0h) must be determined in first.

IT8673F provides flexible control registers related to each of three chip select strobes. Each chip select strobe can be programmed as 1, 2, 4 or 8 via consecutive I/O ports decoding. Each chip select strobe can also be programmed to qualify with IOR# or IOW# strobe. There are four types of qualifying conditions: pure address decided, asserted on address matching and IOR# asserted, asserted on address matching and IOW# asserted, asserted on address matching and IOR# or IOW# asserted.

The Key Lock function locks the keyboard to invalidate any key stroke. The programming method is to set bit 2 on the KBC (keyboard) Special Configuration Register (Index=F0h, LDN=05h). The Keyboard Lock Pin Mapping Register (Index=F9h) must also be programmed correctly.

The Interrupt steering function provides a useful feature for motherboard designers. Through this mapping method, the interrupt of other on-board devices can be easily modified by programming the registers of Index = 70h, 71h, 72h, and 73h.

The Blinking function provides a low frequency blink output. By connecting to some external components, it can be used to control a power LED. There are several frequencies that can be selected.

The PCI CLKRUN# output is used to resume the PCI CLOCK in system power down mode, when the IT8673F devices (Serial Port 1, Serial Port 2, Parallel Port…) request to generate an interrupt through SIRQ protocol. All the devices will not be resumed unless the related enable bits in SMI# control register 1 and 2 are set.

The SMI# is a non-maskable interrupt dedicated for transparent power management. It consists of different enable interrupts from each of the functional blocks in IT8673F. The interrupts are enabled onto the SMI# output via the SMI# control register 1 and SMI# control register 2. The SMI# status registers 1 and 2 are used to read the status of the SMI input events. All the SMI# status register bits can be cleared when the corresponding sources events become invalidated. These bits can also be cleared by writing 1 to bit 7 of SMI# control register 2, whether the events of the corresponding sources are invalidated or not. The SMI# can be programmed as pulse mode or level mode whenever an SMI# event occurs. The logic equation of the SMI# event is described below:

SMI# event = (EN_FIRQ and FIRQ) or (EN_S1IRQ and S1IRQ) or (EN_S2IRQ and S2IRQ) or (EN_PIRQ and PIRQ) or (EN_KBC(Keyboard) and KIRQ) or (EN_KBC(Mouse) and MIRQ) or (EN_GPIRQ1 and GPIRQ1) or (EN_GPIRQ2 or GPIRQ2).

11.2 Advanced Power Supply Control and PME#

The circuit for advanced power supply control (APC) provides three power-up events, Keyboard, Mouse, and RING#. When any of these three events is true, PWRON# will perform a low state until VCC is switched to ON state. The three events include:

1. Detection of RING# pulse or pulse train on the programmed RING# input pin(LDN=04h, Index=FBh, bits 6-4).
2. Detection of KCLK edge or special pattern of KCLK and KDAT. The special pattern of KCLK means pressing pre-set key string sequentially, and KDAT means pressing pre-set keys simultaneously.
3. Detection of MCLK edge or special pattern of MCLK and MDAT. The special pattern of MCLK and MDAT means double clicking on any mouse buttons.

The PANSWH# and PSON are especially designed for PIIX4. PANSWH# serves as a main power switch input which is wire-AND to the APC output PWRON#. PSON is the ATX Power control output, which is a power-failure gating circuit. The power-failure gating circuit is responsible for gating the SUSC# until PANSWH# becomes active when the VCCH is switched from OFF to ON.

The power-failure gating circuit can be disabled by setting the APC/PME Control Register 2 (LDN=04h, Index=F4h, bit 5). The gating circuit also provides an auto-restore function. When the bit 5 of PCR1 is set, the previous PSON state will be restored when the VCCH is switched from OFF to ON.

The RING# function is used to power on the system from modem, fax, etc. It can be programmed to detect a pulse train with pulse low.

The Mask PWRON# Activation bit (bit 4 of PCR 1) is used to mask all Power-up events except Switch on event when the VCCH state is just switched from FAIL to OFF. In other words, when this bit is set and the power state is switched from FAIL to OFF, the only validated function is PANSWH#.

The PCR2 register is responsible for determining the Keyboard power up events and APC conditions. Bit 7 of PCR2 is used to select the function of pin 93 (APC Power up events or PCI PME# output). Bit 4 is used to mask the PANSWH# power-on event. To enable this bit, the keyboard power-up event should be enabled and set by (1) pressing pre-set key string sequentially or (2) stroking pre-set keys simultaneously. The APC/PME# special code index and data registers are used to specify the special key codes in the special power-up events of (1) pressing pre-set key string sequentially or (2) stroking pre-set keys simultaneously.

When bit 7 of PCR2 is set to 1, PME# function is selected. There are two differences. When any one of the three power-up events is true, the output of pin 115 goes low until the corresponding status bit is written to “1”. PME# function is validated in both VCC ON and OFF states.

All APC registers (Index=F0h, F2h, F4h, F5h and F6h) are powered by back-up power (VBAT) when VCCH is OFF.

11.3 FAN Controller

The FAN Controller, built in the IT8673F, include three FAN Tachometers, and three sets of advanced FAN Controllers. FAN Tachometer inputs are digital inputs with an acceptable input range of 0V to 5V, and are responsible for measuring the FAN’s Tachometer pulse periods. FAN_TAC1 and FAN_TAC2 are included with programmable divisors, and can be used to measure different fan speed ranges. FAN_TAC3 is included with fixed divisor, and can only be used in default range.

11.3.1 Interfaces

ISA Bus: The FAN Controller of IT8673F decodes four addresses on the ISA bus.

Table 11-1. Address Map on the ISA Bus

Register or Port	Address
Address register of the Fan Controller	Base+05h
Data register of the Fan Controller	Base+06h

Note 1. The Base Address is determined by the Logical Device configuration registers of FAN Controller (LDN=04h, registers Index= 60h, 61h).

To access an FAN Controller's register, the address of the register is written to the address port (Base+05h). Read or write data from or to that register via data port (Base+06h).

11.3.2 Registers

11.3.2.1 Address Port (Base+05h, Default=00h)

Bit	Description
7	Outstanding; **Read only** This bit is set when a data write is performed to Address Port via the ISA bus or when a Serial Bus transaction is in progress. This bit can be cleared when the Serial Bus transaction is completed, or when a data write/read is performed to/from Data Port.
6-0	Index: Internal Address of RAM and Registers.

Table 11-2. FAN Controller Registers

Index	Register	Default	Description
28h-2Ah	FAN_TAC1-3 Reading	-	FAN Tachometer 1-3 Reading Register; the counts number of the internal clock per resolution
3Bh-3Dh	FAN_TAC1-3 Limit	-	FAN Tachometer 1-3 Count Limit Register
40h	Configuration	08h	
41h	Interrupt Status 1	00h	Auto increment to the index of Interrupt status 2
42h	Interrupt Status 2	00h	
43h	SMI# Mask 1	00h	Auto increment to the index of SMI# Mask 2
44h	SMI# Mask 2	00h	
45h	Interrupt Mask 1	00h	Auto increment to the index of Interrupt Mask 2
46h	Interrupt Mask 2	0Xh	
47h	FAN Tachometer Divisor	5Xh	The divisor values of the FAN Tachometer.
51h	FAN control	00h	FAN control registers
52h	FAN Set X PWM Control	00h	FAN PWM Control Register
58h	Vendor ID	90h	ITE Vendor ID. **Read Only** Register

Note: X indicates 1 or 2 or 3.

11.3.2.2 Register Description

11.3.2.2.1 Configuration Register (Index=40h, Default=08h)

Bit	R/W	Description
7	R/W	Initialization. A “1” restores all registers to their individual default values, except the Serial Bus Address register. This bit clears itself when the default value is “0”.
6	R/W	ON/OFF control of FAN_CTL1. This bit is used to control FAN_CTL1 when FAN_CTL1 mode (Bit 0 of the register Index=51h) is set to ON_OFF mode. 0: OFF. 1: ON.
5-4		Reserved
3	R/W	INT_Clear. A ”1” disables the SMI# and IRQ outputs with the contents of interrupt status bits remain unchanged.
2	R/W	IRQ enables the IRQ Interrupt output.
1	R/W	SMI# Enable. A “1” enables the SMI# Interrupt output.
0	R/W	Reserved

11.3.2.2.2 Interrupt Status Register 1 (Index=41h, Default=00h)

Reading this register will clear itself following a read access.

Bit	R/W	Description
7	R	A “1” indicates the FAN Count 2 limit has been reached.
6	R	A “1” indicates the FAN Count 1 limit has been reached.
5-0	-	Reserved

11.3.2.2.3 Interrupt Status Register 2 (Index=42h, Default=00h)

Reading this register will clear itself after the read operation is completed.

Bit	R/W	Description
7-5	-	Reserved
4	R	A "1" indicates a Case Open has occurred.
3	R	A "1" indicates the FANM Count 3 limit has been reached.
2-0	-	Reserved

11.3.2.2.4 SMI# Mask Register 1 (Index=43h, Default=00h)

Bit	R/W	Description
7	R/W	A "1" disables the FANM Count 2 interrupt status bit for SMI#.
6	R/W	A "1" disables the FANM Count 1 interrupt status bit for SMI#.
5-0	R/W	Reserved

11.3.2.2.5 SMI# Mask Register 2 (Index=44h, Default=00h)

Bit	R/W	Description
7-5	-	Reserved
4	R/W	A "1" disables the Case Open Intrusion interrupt status bit for SMI#.
3	R/W	A "1" disables the FANM count 3 interrupt status bit for SMI#.
2-0	R/W	Reserved

11.3.2.2.6 Interrupt Mask Register 1 (Index=45h, Default=00h)

Bit	R/W	Description
7	R/W	A "1" disables the FANM Count 2 interrupt status bit for IRQ.
6	R/W	A "1" disables the FANM Count 1 interrupt status bit for IRQ.
5-0	R/W	Reserved

11.3.2.2.7 Interrupt Mask Register 2 (Index=46h, Default=0Xh)

Bit	R/W	Description
7	R/W	A "1" outputs an active high pulse on the Case Open pin (COPEN#).
6-5	-	Reserved
4	R/W	A "1" disables the Case Open interrupt status bit for IRQ.
3	R/W	A "1" disables the FANM count 3 interrupt status bit for IRQ.
2-0	R/W	Reserved

11.3.2.2.8 FAN Tachometer Divisor Register (Index=47h, Default=5Xh)

Bit	R/W	Description
7-6	R/W	FAN Tachometer Count 2 divisor 00: divided by 1 01: divided by 2 10: divided by 4 11: divided by 8
5-4	R/W	FAN Tachometer Count 1 divisor 00: divided by 1 01: divided by 2 10: divided by 4 11: divided by 8
3-0	R	Reserved

11.3.2.2.9 FAN Control Register (Index=51h, Default=00h)

Bit	R/W	Description
7-6	R/W	FAN control registers set selection 00: FAN_CTL1 01: FAN_CTL2 10: FAN_CTL3 11: reserved
5	-	Reserved. Should be fixed at 0.
4	R/W	ON/OFF control of FAN_CTL3. This bit is used to control FAN_CTL3 when FAN_CTL3 mode is set on ON_OFF mode (Bit 2 of this register is set to 0). 0: OFF. 1: ON.
3	R/W	ON/OFF control of FAN_CTL2. This bit is used to control FAN_CTL2 when FAN_CTL2 mode is set on ON_OFF mode (Bit 1 of this register is set to 0). 0: OFF. 1: ON.
2	R/W	FAN_CTL3 mode. 0: ON_OFF mode. 1: PWM mode.
1	R/W	FAN_CTL2 mode. 0: ON_OFF mode. 1: PWM mode.
0	R/W	FAN_CTL1 mode. 0: ON_OFF mode. 1: PWM mode.

11.3.2.2.10 FAN Set X PWM Control Register (Index=52h, Default=00h)

The Sex X is determined in the FAN Control Register bits 7-6.

Bit	R/W	Description
7	R/W	Reserved. Should write a “0”.
6-0	R/W	PWM value. There are 128 steps of the FAN_CTL output pin are provided to control fan speeds.

11.3.3 Operation

11.3.3.1 Power On RESET and Software RESET

When the system power is first applied, the FAN Controller performs a “power on reset” on the registers which are returned to default values (due to system hardware reset).

11.3.3.2 Fan Tachometer

The Fan Tachometer inputs gate a 22.5 kHz clock into an 8-bit counter (maximum count=255) for one period of the input signals. Several divisors, located in FAN Divisor Register, are provided for FAN_TAC1 and FAN_TAC2, and are used to modify the monitoring range. FAN_TAC3 is not adjustable, and its divisor value is always set to 2. Counts are based on 2 pulses per resolution tachometer output.

RPM = 1.35 X 10^6 / (Count X Divisor)

The maximum input signal range is from 0 to VCC. The additional application is needed to clamp the input voltage and current.

11.3.3.3 Fan Controller ON-OFF and SmartGuardian Modes

The IT8673F provides advanced FAN Controllers. Two modes are provided for each controller: ON_OFF and PWM modes. The former is a logical ON or OFF, and the latter is a PWM output. With the addition of external application, the Fan’s voltage values can be varied easily.

11.4 Floppy Disk Controller (FDC)

11.4.1 Introduction

The Floppy Disk Controller provides the interface between a host processor and up to two floppy disk drives. It integrates a controller and a digital data separator with write precompensation, data rate selection logic, microprocessor interface, and a set of registers.

The FDC supports data transfer rates of 250 Kbps, 300 Kbps, 500 Kbps, and 1 Mbps. It operates in PC/AT mode and supports 3-Mode type drives. Additionally, the FDC is software compatible with the 82077.

The FDC configuration is handled by software and a set of Configuration registers. Status, Data, and Control registers facilitate the interface between the host microprocessor and the disk drive, providing information about the condition and/or state of the FDC. These configuration registers can select the data rate, enable interrupts, drives, and DMA modes, and indicate errors in the data or operation of the FDC/FDD.

The controller manages data transfers using a set of data transfer and control commands. These commands are handled in three phases: Command, Execution, and Result. Not all commands utilize all these three phases.

11.4.2 Reset

The IT8673F device implements both software and hardware reset options for the FDC. Either type of the resets will reset the FDC, terminating all operations and placing the FDC into an idle state. A reset during a write to the disk will corrupt the data and the corresponding CRC.

11.4.3 Hardware Reset (RESET Pin)

When the FDC receives a RESET signal, all registers of the FDC core are cleared (except those programmed by the SPECIFY command). To exit the reset state, the host must clear the DOR bit.

11.4.4 Software Reset (DOR Reset and DSR Reset)

When the reset bit in the DOR or the DSR is set, all registers of the FDC core are cleared. A reset performed by setting the reset bit in the DOR has higher priority over a reset performed by setting the reset bit in the DSR. In addition, to exit the reset state, the DSR bit is self-clearing, while the host must clear the DOR bit.

11.4.5 Digital Data Separator

The internal digital data separator is comprised of a digital PLL and associated support circuitry. It is responsible for synchronizing the raw data signal read from the floppy disk drive. The synchronized signal is used to separate the encoded clock from the data pulses.

11.4.6 Write Precompensation

Write precompensation is a method that can be used to adjust the effects of bit shift on data as it is written to the disk. It is harder for the data separator to read data that has been subject to bit shifting. Soft read errors can occur due to such bit shifting. Write precompensation predicts where the bit shifting might occur within a data pattern and shifts the individual data bits back to their nominal positions. The FDC permits the selection of write precompensation via the Data Rate Select Register (DSR) bits 2 through 4.

11.4.7 Data Rate Selection

Selecting one of the four possible data rates for the attached floppy disks is accomplished by setting the Diskette Control Register (DCR) or Data Rate Select Register (DSR) bits to 0 and 1. The data rate is determined by the last value that is written to either the DCR or the DSR. When the data rate is set, the data separator clock is scaled appropriately.

11.4.8 Status, Data and Control Registers

11.4.8.1 Digital Output Register (DOR, FDC Base Address + 02h)

This is a Read/Write register. It controls drive selection and motor enables as well as a software reset bit and DMA enable. The I/O interface reset may be used at any time to clear the DOR's contents.

Table 11-3. Digital Output Register (DOR)

Bit	Symbol	Name	Description
7-6	-	-	Reserved
5	MOTB EN	Drive B Motor Enable	0: Disable Drive B motor. 1: Enable Drive B motor.
4	MOTA EN	Drive A Motor Enable	0: Disable Drive A motor. 1: Enable Drive A motor.
3	DMAEN	Disk Interrupt and DMA Enable	0: Disable disk interrupt and DMA (DRQx, DACKx#, TC and INTx). 1: Enable disk interrupt and DMA.
2	RESET#	FDC Function Reset	0: Reset FDC function. 1: Clear reset of FDC function. This reset does not affect the DSR, DCR or DOR.
1	-	-	Reserved
0	DVSEL	Drive Selection	0: Selects Drive A. 1: Selects Drive B.

11.4.8.2 Tape Drive Register (TDR, FDC Base Address + 03h)

This is a **read/write** register and is included for 82077 software compatibility. The contents of this register are not used internal to the device.

Table 11-4. Tape Drive Register (TDR)

Bit	Symbol	Name	Description
7-2	NU	Not Used	-
1-0	TP_SEL[1:0]	Tape Drive Selection	TP_SEL[1:0] : Drive selected. 00: None 01: 1 10: 2 11: 3

11.4.8.3 Main Status Register (MSR, FDC Base Address + 04h)

This is a **read only** register. It indicates the general status of the FDC, and is able to receive data from the host. The MSR should be read before each byte is sent to or received from the Data register, except when in DMA mode.

Table 11-5. Main Status Register (MSR)

Bit	Symbol	Name	Description
7	RQM	Request for Master	FDC Request for Master. 0: The FDC is busy and cannot receive data from the host. 1: The FDC is ready and the host can transfer data.
6	DIO	Data I/O Direction	Indicates the direction of data transfer once a RQM has been set. 0: Write 1: Read
5	NDM	Non-DMA Mode	This bit selects Non-DMA mode of operation. 0: DMA mode selected. 1: Non-DMA mode selected. This mode is selected via the SPECIFY command during the Execution phase of a command.
4	CB	Diskette Control Busy	Indicates whether a command is in progress (the FDD is busy). 0: A command has been executed and the end of the Result phase has been reached. 1: A command is being executed.
3-2	-	-	Reserved
1	DBB	Drive B Busy	Indicates whether Drive B is in the SEEK portion of a command. 0: Not busy. 1: Busy.
0	DAB	Drive A Busy	Indicates whether Drive A is in the SEEK portion of a command. 0: Not busy. 1: Busy.

11.4.8.4 Data Rate Select Register (DSR, FDC Base Address + 04h)

This is a **write only** register. It is used to determine the data rate, amount of write precompensation, power down mode, and software reset. The data rate of the floppy controller is the most recent write of either the DSR or DCR. The DSR is unaffected by a software reset. The DSR can be set to 02h by a hardware reset, and the “02h” represents the default precompensation, and 250 Kbps indicates the data transfer rate.

Table 11-6. Data Rate Select Register (DSR)

<table>
<tr><th>Bit</th><th>Symbol</th><th>Name</th><th>Description</th></tr>
<tr><td>7</td><td>S/W RESET</td><td>Software Reset</td><td>Software Reset. It is active high and shares the same function with the RESET# of the DOR except that this bit is self-clearing.</td></tr>
<tr><td>6</td><td>POWER DOWN</td><td>Power Down</td><td>When this bit is written with a “1”, the floppy controller is put into manual low power mode. The clocks of the floppy controller and data separator circuits will be turned off until a software reset or the Data Register or Main Status Register is accessed.</td></tr>
<tr><td>5</td><td>NU</td><td>Not Used</td><td>-</td></tr>
<tr><td>4-2</td><td>PRE-COMP 2-0</td><td>Precompensation Select</td><td>These three bits are used to determine the value of write precompensation that will be applied to the WDATA# pin. Track 0 is the default starting track number, which can be changed by the CONFIGURE command for precompensation.
<table>
<tr><th>PRE_COMP</th><th>Precompensation Delay</th></tr>
<tr><td>111</td><td>0.0 ns</td></tr>
<tr><td>001</td><td>41.7 ns</td></tr>
<tr><td>010</td><td>83.3 ns</td></tr>
<tr><td>011</td><td>125.0 ns</td></tr>
<tr><td>100</td><td>166.7 ns</td></tr>
<tr><td>101</td><td>208.3 ns</td></tr>
<tr><td>110</td><td>250.0 ns</td></tr>
<tr><td>000</td><td>Default</td></tr>
</table>
Default Precompensation Delays
<table>
<tr><th>Data Rate</th><th>Precompensation Delay</th></tr>
<tr><td>1Mbps</td><td>41.7 ns</td></tr>
<tr><td>500Kbps</td><td>125.0 ns</td></tr>
<tr><td>300Kbps</td><td>125.0 ns</td></tr>
<tr><td>250Kbps</td><td>125.0 ns</td></tr>
</table></td></tr>
<tr><td>1-0</td><td>DRATE1-0</td><td>Data Rate Select</td><td>Bits 1-0 — Data Transfer Rate
00 — 500 Kbps
01 — 300 Kbps
10 — 250 Kbps (default)
11 — 1 Mbps</td></tr>
</table>

11.4.8.5 Data Register (FIFO, FDC Base Address + 05h)

This is an 8-bit **read/write** register. It transfers command information, diskette drive status information, and the result phase status between the host and the FDC. The FIFO consists of several registers in a stack. Only one register in the stack is permitted to transfer information or status to the data bus at a time.

Table 11-7. Data Register (FIFO)

Bit	Symbol	Name	Description
7-0		Data	Command information, diskette drive status, or result phase status data.

11.4.8.6 Digital Input Register (DIR, FDC Base Address + 07h)

This is a **read only** register and shares this address with the Diskette Control Register (DCR).

Table 11-8. Digital Input Register (DIR)

Bit	Symbol	Name	Description
7	DSKCHG	Diskette Change	Indicates the inverting value of the bit monitored from the input of the Floppy Disk Change pin (DSKCHG#).
6-0	NU	Not Used	-

11.4.8.7 Diskette Control Register (DCR, FDC Base Address + 07h)

This is a **write only** register and shares this address with the Digital Input Register (DIR).

The DCR register controls the data transfer rate for the FDC.

Table 11-9. Diskette Control Register (DCR)

Bit	Symbol	Name	Description
7-2	NU	Not Used	-
1-0	DRATE1-0	Data Rate Select	**Bits 1-0** **Data Transfer Rate** 00 500Kbps 01 300Kbps 10 250Kbps 11 1Mbps

11.4.9 Controller Phases

The FDC handles data transfer and control commands in three phases: Command, Execution and Result. Not all commands utilize all these three phases.

11.4.9.1 Command Phase

Upon reset, the FDC enters the Command phase and is ready to receive commands from the host. The host must verify that MSR bit 7 (RQM) = 1 and MSR bit 6 (DIO) = 0, indicating the FDC is ready to receive data. For each command, a defined set of command code and parameter bytes must be transferred to the FDC in a given order. See 11.4.11 and 11.4.12 for details on the various commands. RQM is set false (0) after each byte-Read cycle, and set true (1) when a new parameter byte is required. The Command phase is completed when this set of bytes has been received by the FDC. The FDC automatically enters the next controller phase and the FIFO is disabled.

11.4.9.2 Execution Phase

Upon the completion of the Command phase, the FDC enters the Execution phase. It is in this phase that all data transfers occur between the host and the FDC. The SPECIFY command indicates whether this data transfer occurs in DMA or non-DMA mode. Each data byte is transferred via an IRQx or DRQx# based upon the DMA mode. On reset, the CONFIGURE command can automatically enable or disable the FIFO. The Execution phase is completed when all data bytes have been received. If the command executed does not require a Result phase, the FDC is ready to receive the next command.

11.4.9.3 Result Phase

For commands that require data written to the FIFO, the FDC enters the Result phase when the IRQ or DRQ is activated. The MSR bit 7 (RQM) and MSR bit 6 (DIO) must equal to 1 to read the data bytes. The Result phase is completed when the host has read each of the defined set of result bytes for the given command. Right after the completion of the phase, RQM is set to 1, DIO is set to 0, and the MSR bit 4 (CB) is cleared, indicating the FDC is ready to receive the next command.

11.4.9.4 Result Phase Status Registers

For commands that contain a Result phase, these Read only registers indicate the status of the most recently executed command.

Table 11-10. Status Register 0 (ST0)

Bit	Symbol	Name	Description
7-6	IC	Interrupt Code	00: Execution of the command has been completed correctly 01: Execution of the command began, but failed to complete successfully 10: INVALID command 11: Execution of the command was not completed correctly, due to a polling error
5	SE	Seek End	The FDC executed a SEEK or RE-CALIBRATE command.
4	EC	Equipment Check	The TK00# pin was not set after a RE-CALIBRATE command was issued.
3	NU	Not Used	-
2	H	Head Address	The current head address.
1	DSB	Drive B Select	Drive B selected.
0	DSA	Drive A Select	Drive A selected.

Table 11-11. Status Register 1 (ST1)

Bit	Symbol	Name	Description
7	EN	End of Cylinder	Indicates the FDC attempted to access a sector beyond the final sector of the track. This bit will be set if the Terminal Count (TC) signal is not issued after a READ DATA or WRITE DATA command.
6	NU	Not Used	-
5	DE	Data Error	A CRC error occurred in either the ID field or the data field of a sector.
4	OR	Overrun/ Underrun	An overrun on a READ operation or underrun on a WRITE operation occurs when the FDC is not serviced by the CPU or DMA within the required time interval.
3	NU	Not Used	-
2	ND	No Data	No data are available to the FDC when either of the following conditions is met: 1. The floppy disk cannot find the indicated sector while the READ DATA or READ DELETED DATA commands are executed, or 2. While executing a READ ID command, an error occurs upon reading the ID field, or 3. While executing a READ A TRACK command, the FDC cannot find the starting sector
1	NW	Not Writeable	Set when a WRITE DATA, WRITE DELETED DATA, or FORMAT A TRACK command is being executed on a write-protected diskette.
0	MA	Missing Address Mark	This flag bit is set when either of the following conditions is met: 1. The FDC cannot find a Data Address Mark or a Deleted Data Address Mark on the specified track, or 2. The FDC cannot find any ID address on the specified track after two index pulses are detected from the INDEX# pin

Table 11-12. Status Register 2 (ST2)

Bit	Symbol	Name	Description
7	NU	Not Used	-
6	CM	Control Mark	This flag bit is set when either of the following conditions is met: 1. The FDC finds a Deleted Data Address Mark during a READ DATA command, or 2. The FDC finds a Data Address Mark during a READ DELETED DATA command
5	DD	Data Error in Data Field	This flag bit is set when a CRC error is found in the data field.
4	WC	Wrong Cylinder	This flag bit is set when the track address in the ID field is different from the track address specified in the FDC.
3	SH	Scan Equal Hit	This flag bit is set when the condition of "equal" is satisfied during a SCAN command.
2	SN	Scan Not Satisfied	This flag bit is set when the FDC cannot find a sector on the cylinder during a SCAN command.
1	BC	Bad Cylinder	This flag bit is set when the track address equals “FFh” and is different from the track address in the FDC.
0	MD	Missing Data Address Mark	This flag bit is set when a Data Address Mark or Deleted Data Address Mark cannot be found by the FDC.

Table 11-13. Status Register 3 (ST3)

Bit	Symbol	Name	Description
7	FT	Fault	Indicates the current status of the Fault signal from the FDD.
6	WP	Write Protect	Indicates the current status of the Write Protect signal from the FDD.
5	RDY	Ready	Indicates the current status of the Ready signal from the FDD.
4	TK0	Track 0	Indicates the current status of the Track 0 signal from the FDD.
3	TS	Two Side	Indicates the current status of the Two Side signal from the FDD.
2	HD	Head Address	Indicates the current status of the Head Select signal to the FDD.
1-0	US1, US0	Unit Select	Indicate the current status of the Unit Select signals to the FDD.

11.4.10 Command Set

The FDC utilizes a defined set of commands to communicate with the host. Each command is comprised of a unique first byte, which contains the op-code, and a series of additional bytes, which contain the required set of parameters and results. The op-code byte indicates to the FDC how many additional bytes should be expected for the command being written. The descriptions use a common set of parameter byte symbols, which are presented in Table 11-14. The FDC commands may be executed whenever the FDC is in the Command phase. The FDC checks to see that the first byte is a valid command and, if so, proceeds. An interrupt is issued if it is not a valid command.

Table 11-14. Command Set Symbol Descriptions

Symbol	Name	Description
C	Cylinder Number	The current/selected cylinder (track) number: 0 – 255.
D	Data	The data pattern to be written into a sector.
DC3–DC0	Drive Configuration Bit3-0	Designate which drives are perpendicular drives on the PERPENDICULAR MODE command.
DIR	Direction Control	Read/Write Head Step Direction Control. 0 = Step Out; 1 = Step In.
DR0, DR1	Disk Drive Select	The selected drive number: 0 or 1.
DTL	Data Length	When N is defined as 00h, DTL designates the number of data bytes which users are going to read out or write into the Sector. When N is not 00h, DTL is undefined.
DFIFO	Disable FIFO	A “1” will disable the FIFO (default). A “0” will enable the FIFO.
EC	Enable Count	If EC=1, DTL of VERIFY command will be SC.
EIS	Enable Implied Seek	If EIS=1, a SEEK operation will be performed before executing any READ or WRITE command that requires the C parameter.
EOT	End of Track	The final sector number on a cylinder. During a READ or WRITE operation, the FDC stops data transfer after the sector number is equal to EOT.
GAP2	Gap 2 Length	By PERPENDICULAR MODE command, this parameter changes Gap 2 length in the format.
GPL	Gap Length	The length of Gap 3. During a FORMAT command, it determines the size of Gap 3.
H	Head Address	The Head number 0 or 1, as specified in the sector ID field. (H = HD in all command words.)
HD	Head	The selected Head number 0 or 1. Also controls the polarity of HDSEL#. (H = HD in all command words.)
HLT	Head Load Time	The Head Load Time in the FDD (2 to 254 ms in 2 ms increments).
HUT	Head Unload Time	The Head Unload Time after a READ or WRITE operation has been executed (16 to 240 ms in 16 ms increments).
LOCK		If LOCK=1, DFIFO, FIFOTHR, and PRETRK parameters of the CONFIGURE command will not be affected by a software reset. If LOCK=0 (default), the above parameters will be set to their default values following a software reset.

Table 11-14. Command Set Symbol Descriptions (cont'd)

Symbol	Name	Description
MFM	FM or MFM Mode	If MFM is low, FM Mode (single density) is selected. If MFM is high, MFM Mode (double density) is selected.
MT	Multi-Track	If MT is high, a Multi-Track operation is to be performed. In this mode, the FDC will automatically start searching for sector 1 on side 1 after finishing a READ/WRITE operation on the last sector on side 0.
N	Number	The number of data bytes written into a sector, where: 00 = 128 bytes (PC standard) 01 = 256 bytes 02 = 512 bytes … 07 = 16 Kbytes
NCN	New Cylinder Number	A new cylinder number, which is to be reached as a result of the SEEK operation. Desired position of Head.
ND	Non-DMA Mode	When ND is high, the FDC operates in the Non-DMA Mode.
OW	Overwrite	If OW=1, DC3-0 of the PERPENDICULAR MODE command can be modified. Otherwise, those bits cannot be changed.
PCN	Present Cylinder Number	The cylinder number at the completion of a SENSE INTERRUPT STATUS command. Position of Head at present time.
POLLD	Polling Disable	If POLLD=1, the internal polling routine is disabled.
PRETRK	Precompensation Starting Track Number	Programmable from track 0 – 255.
R	Record	The sector number, which will be read or written.
RCN	Relative Cylinder Number	To determine the relative cylinder offset from present cylinder as used by the RELATIVE SEEK command.
SC		The number of sectors per cylinder.
SK	Skip	If SK=1, the Read Data operation will skip sectors with a Deleted Data Address Mark. Or, the Read Deleted Data operation only accesses sectors with a Deleted Data Address Mark.
SRT	Step Rate Time	The Stepping Rate for the FDD (1 to 16 ms in 1 ms increments). Stepping Rate applies to all drives (F=1 ms, E=2 ms, etc.).
ST0 ST1 ST2 ST3	Status 0 Status 1 Status 2 Status 3	ST0–3 stand for one of four registers that store the status information after a command has been executed. This information is available during the Result phase after command execution. These registers should not be confused with the Main Status Register (selected by $A_0 = 0$); ST0–3 may be read only after a command has been executed and contain information associated with that particular command.
STP		If STP = 1 during a SCAN operation, the data in contiguous sectors are compared byte by byte with data sent from the processor (or DMA). If STP = 2, alternate sectors are read and compared.

Table 11-15. Command Set Summary

READ DATA										
Phase	**R/W**	**Data Bus**								**Remarks**
		D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	
Command	W	MT	MFM	SK	0	0	1	1	0	Command Codes
	W	0	0	0	0	0	HDS	DR1	DR0	
	W	C								Sector ID information before the command execution
	W	H								
	W	R								
	W	N								
	W	EOT								
	W	GPL								
	W	DTL								
Execution										Data transfer between the FDD and the main system
Result	R	ST0								Status information after command execution
	R	ST1								
	R	ST2								
	R	C								Sector ID information after command execution
	R	H								
	R	R								
	R	N								

READ DELETED DATA										
Phase	**R/W**	**Data Bus**								**Remarks**
		D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	
Command	W	MT	MFM	SK	0	1	1	0	0	Command Codes
	W	0	0	0	0	0	HDS	DR1	DR0	
	W	C								Sector ID information before the command execution
	W	H								
	W	R								
	W	N								
	W	EOT								
	W	GPL								
	W	DTL								
Execution										Data transfer between the FDD and the main system
Result	R	ST0								Status information after command execution
	R	ST1								
	R	ST2								
	R	C								Sector ID information after command execution
	R	H								
	R	R								
	R	N								

READ A TRACK										
Phase	**R/W**	**Data Bus**								**Remarks**
		D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	
Command	W	MT	MFM	0	0	0	0	1	0	Command Codes
	W	0	0	0	0	0	HDS	DR1	DR0	
	W	C								Sector ID information before the command execution
	W	H								
	W	R								
	W	N								
	W	EOT								
	W	GPL								
	W	DTL								
Execution										Data transfer between the FDD and main system cylinder's contents from index hole to EOT
Result	R	ST0								Sector ID information before the command execution
	R	ST1								
	R	ST2								
	R	C								Sector ID information after command execution
	R	H								
	R	R								
	R	N								

WRITE DATA										
Phase	**R/W**	**Data Bus**								**Remarks**
		D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	
Command	W	MT	MFM	0	0	0	1	0	1	Command Codes
	W	0	0	0	0	0	HDS	DR1	DR0	
	W	C								Sector ID information before the command execution
	W	H								
	W	R								
	W	N								
	W	EOT								
	W	GPL								
	W	DTL								
Execution										Data transfer between the FDD and the main system
Result	R	ST0								Status information after command execution
	R	ST1								
	R	ST2								
	R	C								Sector ID information after command execution
	R	H								
	R	R								
	R	N								

WRITE DELETED DATA									
Phase	**R/W**	**Data Bus**							**Remarks**
		D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
Command	W	MT	MFM	0	0	1	0	0	1	Command Codes
	W	0	0	0	0	0	HDS	DR1	DR0	
	W	C								Sector ID information before the command execution
	W	H								
	W	R								
	W	N								
	W	EOT								
	W	GPL								
	W	DTL								
Execution										Data transfer between the FDD and the main system.
Result	R	ST0								Status information after command execution
	R	ST1								
	R	ST2								
	R	C								Sector ID information after command execution
	R	H								
	R	R								
	R	N								

FORMAT A TRACK									
Phase	**R/W**	**Data Bus**							**Remarks**
		D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
Command	W	0	MFM	0	0	1	1	0	1	Command Codes
	W	0	0	0	0	0	HDS	DR1	DR0	
	W	N								Bytes/Sector
	W	SC								Sectors/Cylinder
	W	GPL								Gap 3
	W	D								Filler Byte
Execution	W	C								Input Sector Parameters per-sector
	W	H								
	W	R								
	W	N								
Result	R	ST0								FDC formats an entire cylinder Status information after command execution
	R	ST1								
	R	ST2								
	R	Undefined								
	R	Undefined								
	R	Undefined								
	R	Undefined								

SCAN EQUAL									
Phase	**R/W**	**Data Bus**							**Remarks**
		D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
Command	W	MT	MFM	SK	1	0	0	0	1	Command Codes
	W	0	0	0	0	0	HDS	DR1	DR0	
	W	C								Sector ID information before the command execution
	W	H								
	W	R								
	W	N								
	W	EOT								
	W	GPL								
	W	STP								
Execution										Data transferred from the system to controller is compared to data read from disk
Result	R	ST0								Status information after command execution
	R	ST1								
	R	ST2								
	R	C								Sector ID information after command execution
	R	H								
	R	R								
	R	N								

SCAN LOW OR EQUAL									
Phase	**R/W**	**Data Bus**							**Remarks**
		D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
Command	W	MT	MFM	SK	1	1	0	0	1	Command Codes
	W	0	0	0	0	0	HDS	DR1	DR0	
	W	C								Sector ID information before the command execution
	W	H								
	W	R								
	W	N								
	W	EOT								
	W	GPL								
	W	STP								
Execution										Data transferred from the system to controller is compared to data read from disk
Result	R	ST0								Status information after command execution
	R	ST1								
	R	ST2								
	R	C								Sector ID information after command execution
	R	H								
	R	R								
	R	N								

SCAN HIGH OR EQUAL									
Phase	R/W	Data Bus							Remarks
		D7	D6	D5	D4	D3	D2	D1	D0	
Command	W	MT	MFM	SK	1	1	1	0	1	Command Codes
	W	0	0	0	0	0	HDS	DR1	DR0	
	W	C								Sector ID information before the command execution
	W	H								
	W	R								
	W	N								
	W	EOT								
	W	GPL								
	W	STP								
Execution										Data transferred from the system to controller is compared to data read from disk
Result	R	ST0								Status information after command execution
	R	ST1								
	R	ST2								
	R	C								Sector ID information after command execution
	R	H								
	R	R								
	R	N								

VERIFY									
Phase	R/W	Data Bus							Remarks
		D7	D6	D5	D4	D3	D2	D1	D0	
Command	W	MT	MFM	SK	1	0	1	1	0	Command Codes
	W	EC	0	0	0	0	HDS	DR1	DR0	
	W	C								Sector ID information before the command execution
	W	H								
	W	R								
	W	N								
	W	EOT								
	W	GPL								
	W	DTL/SC								
Execution										No data transfer takes place
Result	R	ST0								Status information after command execution
	R	ST1								
	R	ST2								
	R	C								Sector ID information after command execution
	R	H								
	R	R								
	R	N								

READ ID									
Phase	R/W	Data Bus							Remarks
		D7	D6	D5	D4	D3	D2	D1	D0	
Command	W	0	MFM	0	0	1	0	1	0	Command Codes
	W	0	0	0	0	0	HDS	DR1	DR0	
Execution										The first correct ID information on the Cylinder is stored in the Data Register
Result	R	ST0								Status information after command execution
	R	ST1								
	R	ST2								
	R	C								Sector ID information during execution phase
	R	H								
	R	R								
	R	N								

CONFIGURE									
Phase	R/W	Data Bus							Remarks
		D7	D6	D5	D4	D3	D2	D1	D0	
Command	W	0	0	0	1	0	0	1	1	Configure Information
	W	0	0	0	0	0	0	0	0	
	W	0	EIS	DFIFO	POLLD	FIFOTHR				
		PRETRK								
Execution										

RE-CALIBRATE									
Phase	R/W	Data Bus							Remarks
		D7	D6	D5	D4	D3	D2	D1	D0	
Command	W	0	0	0	0	0	1	1	1	Command Codes
	W	0	0	0	0	0	0	DR1	DR0	
Execution										Head retracted to Track 0

SEEK									
Phase	R/W	Data Bus							Remarks
		D7	D6	D5	D4	D3	D2	D1	D0	
Command	W	0	0	0	0	1	1	1	1	Command Codes
	W	0	0	0	0	0	HDS	DR1	DR0	
	W	NCN								
Execution										Head is positioned over proper cylinder on diskette

RELATIVE SEEK									
Phase	R/W	Data Bus							Remarks
		D7	D6	D5	D4	D3	D2	D1	D0	
Command	W	1	DIR	0	0	1	1	1	1	Command Codes
	W	0	0	0	0	0	HDS	DR1	DR0	
	W	RCN								
Execution										Head is stepped in or out a programmable number of tracks

DUMPREG									
Phase	R/W	Data Bus							Remarks
		D7	D6	D5	D4	D3	D2	D1	D0	
Command	W	0	0	0	0	1	1	1	0	Command Codes
Execution										Registers placed in FIFO
Result	R	PCN-Drive 0								
	R	PCN-Drive 1								
	R	PCN-Drive 2								
	R	PCN-Drive 3								
	R	SRT				HUT				
	R	HLT							ND	
	R									
	R	LOCK	0	DC3	DC2	DC1	DC0	GAP	WG	
	R	0	DIS	DFIFO	POLLD	FIFOTHR				
	R	PRETRK								

LOCK									
Phase	R/W	Data Bus							Remarks
		D7	D6	D5	D4	D3	D2	D1	D0	
Command	W	LOCK	0	0	1	0	1	0	0	Command Codes
Result	R	0	0	0	LOCK	0	0	0	0	

VERSION									
Phase	R/W	Data Bus							Remarks
		D7	D6	D5	D4	D3	D2	D1	D0	
Command	W	0	0	0	1	0	0	0	0	Command Codes
Result	R	1	0	0	1	0	0	0	0	Enhanced Controller

SENSE INTERRUPT STATUS									
Phase	R/W	Data Bus							Remarks
		D7	D6	D5	D4	D3	D2	D1	D0	
Command	W	0	0	0	0	1	0	0	0	Command Codes
Result	R	ST0								Status information at the end of each SEEK operation
	R	PCN								

SENSE DRIVE STATUS									
Phase	R/W	Data Bus							Remarks
		D7	D6	D5	D4	D3	D2	D1	D0	
Command	W	0	0	0	0	0	1	0	0	Command Codes
	W	0	0	0	0	0	HDS	DR1	DR0	
Result	R	ST3								Status information about FDD

SPECIFY									
Phase	R/W	Data Bus							Remarks
		D7	D6	D5	D4	D3	D2	D1	D0	
Command	W	0	0	0	0	0	0	1	1	Command Codes
	W	SRT				HUT				
	W	HLT							ND	

PERPENDICULAR MODE									
Phase	R/W	Data Bus							Remarks
		D7	D6	D5	D4	D3	D2	D1	D0	
Command	W	0	0	0	1	0	0	1	0	Command Codes
	W	OW	0	DC3	DC2	DC1	DC0	GAP	WG	

INVALID									
Phase	R/W	Data Bus							Remarks
		D7	D6	D5	D4	D3	D2	D1	D0	
Command	W	Invalid codes								INVALID Command Codes (NO-OP: FDC goes into standby state)
Result	R	ST0								ST0 = 80h

11.4.11 Data Transfer Commands

All data transfer commands utilize the same parameter bytes (except for FORMAT A TRACK command) and return the same result data bytes. The only difference between them is the five bits (0–4) of the first byte.

11.4.11.1 READ DATA

The READ DATA command contains nine command bytes that place the FDC into the Read Data mode. Each READ operation is initialized by a READ DATA command. The FDC locates the sector to be read by matching ID Address Marks and ID fields from the command with the information on the diskette. The FDC then transfers the data to the FIFO. When the data from the given sector has been read, the READ DATA command is completed and the sector address is automatically incremented by “1”. The data from the next sector is read and transferred to the FIFO in the same manner. Such a continuous Read function is called a "Multi-Sector Read Operation".

If a TC or an implied TC (FIFO overrun/underrun) is received, the FDC stops sending data, but continues to read data from the current sector and checks the CRC bytes until the end of the sector is reached and the READ operation is completed.

The sector size is determined by the N parameter value as calculated in the equation below:

Sector Size = $2^{(7+N\ value)}$ bytes.

The DTL parameter determines the number of bytes to be transferred. Therefore, if N = 00h, setting the sector size to 128 and the DTL parameter value is less than this, the remaining bytes will be read and checked for CRC errors by the FDC. If this occurs in a WRITE operation, the remaining bytes will be filled with 0. If the sector size is not 128 (N > 00h), DTL should be set to FFh.

In addition to performing Multi-Sector Read operations, the FDC can perform Multi-Track Read operations. When the MT parameter is set, the FDC can read both sides of a disk automatically.

The combination of N and MT parameter values determines the amount of data that can be transferred during either type of READ operation. Table 11-16 shows the maximum data transfer capacity and the final sector the FDC reads based on these parameters.

Table 11-16. Effects of MT and N Bits

MT	N	Maximum Transfer Capacity	Final Sector Read from Disk
0	1	256 X 26 = 6656	26 on side 0 or side 1
1	1	256 X 52 = 13312	26 on side 1
0	2	512 X 15 = 7680	15 on side 0 or side 1
1	2	512 X 30 = 15360	15 on side 1
0	3	1024 X 8 = 8192	8 on side 0 or side 1
1	3	1024 X16 =16384	16 on side 1

11.4.11.2 READ DELETED DATA

The READ DELETED DATA command is the same as the READ DATA command, except that a Deleted Data Address Mark (as opposed to a Data Address Mark) is read at the beginning of the Data Field. This command is typically used to mark a bad sector on a diskette.

11.4.11.3 READ A TRACK

After receiving a pulse from the INDEX# pin, the READ A TRACK command reads the entire data field from each sector of the track as a continuous block. If any ID or Data Field CRC error is found, the FDC continues to read data from the track and indicates the error at the end. Because the Multi-Track [and Skip] operation[s] is[are] not allowed under this command, the MT and SK bits should be low (0) during the command execution.

This command terminates normally when the number of sectors specified by EOT has not been read. If, however, no ID Address Mark has been found by the second occurrence of the INDEX pulse, the FDC will set the IC code in the ST0 to 01, indicating an abnormal termination, and then finish the command.

11.4.11.4 WRITE DATA

The WRITE DATA command contains nine command bytes that place the FDC into the Write Data mode. Each WRITE operation is initialized by a WRITE DATA command. The FDC locates the sector to be written by reading ID fields and matching the sector address from the command with the information on the diskette. Then the FDC reads the data from the host via the FIFO and writes the data into the sector's data field. Finally, the FDC computes the CRC value, storing it in the CRC field, and increments the sector number (stored in the R parameter) by "1". The next data field is written into the next sector in the same manner. Such a continuous write function is called a "Multi-Sector Write Operation".

If a TC or an implied TC (FIFO overrun/underrun) is received, the FDC stops writing data and fills the remaining data field with 0s. If a check of the CRC value indicates an error in the sector ID Field, the FDC will set the IC code in the ST0 to 01 and the DE bit in the ST1 to 1, indicating an abnormal termination, and then terminate the WRITE DATA command. The maximum data transfer capacity and the DTL, N, and MT parameters are the same as in the READ DATA command.

11.4.11.5 WRITE DELETED DATA

The WRITE DELETED DATA command is the same as the WRITE DATA command, except that a Deleted Data Address Mark (instead of a Data Address Mark) is written at the beginning of the Data Field. This command is typically used to mark a bad sector on a diskette.

11.4.11.6 FORMAT A TRACK

The FORMAT A TRACK command is used to format an entire track. Initialized by an INDEX pulse, it writes data to the Gaps, Address Marks, ID fields and Data fields according to the density mode selected (FM or MFM). The Gap and Data field values are controlled by the host-specified values programmed into N, SC, GPL, and D during the Command phase. The Data field is filled with the data byte specified by D. The four data bytes per sector (C, H, R, and N) needed to fill the ID field are supplied by the host. The C, R, H, and N values must be renewed for each new sector of a track. Only the R parameter value must be changed when a sector is formatted, allowing the disk to be formatted with non-sequential sector addresses. These steps are repeated until a new INDEX pulse is received, at which point the FORMAT A TRACK command is terminated.

11.4.11.7 SCAN

The SCAN command allows the data read from the disk to be compared with the data sent from the system. There are three SCAN commands:

SCAN EQUAL Disk Data = System Data

SCAN HIGH OR EQUAL Disk Data ≥ System Data

SCAN LOW OR EQUAL Disk Data ≤ System Data

The SCAN command execution continues until the scan condition has been met, or the EOT has been reached, or if TC is asserted. Read errors on the disk have the same error condition as the READ DATA command. If the SK bit is set, sectors with deleted data address marks are ignored. If all sectors read are skipped, the command terminates with the D3 bit of the ST2 being set. The Result phase of the command is shown below:

Table 11-17. SCAN Command Result

Command	Status Register		Condition
	D2	D3	
SCAN EQUAL	0	1	Disk = System
	1	0	Disk ≠ System
SCAN HIGH OR EQUAL	0	1	Disk = System
	0	0	Disk > System
	1	0	Disk < System
SCAN LOW OR EQUAL	0	1	Disk = System
	0	0	Disk < System
	1	0	Disk > System

11.4.11.8 VERIFY

The VERIFY command is used to read logical sectors containing a Normal Data AM from the selected drive without transferring the data to the host. This command acts like a READ DATA command except that no data is transferred to the host. This command is designed for post-format or post write verification. Data is read from the disk, as the controller checks for valid Address Marks in the Address and Data Fields. The CRC is computed and checked against the previously stored value. Because no data is transferred to the host, the TC (Terminal Count of DMA) cannot be used to terminate this command. An implicit TC will be issued to the FDC by setting the EC bit. This implicit TC will occur when the SC value has decremented to 0. This command can also be terminated by clearing the EC bit and when the EOT value equals to the final sector to be checked.

Table 11-18. VERIFY Command Result

MT	EC	SC/EOT	Termination Result
0	0	SC = DTL EOT ≤ # Sectors per side	No Error
0	0	SC = DTL EOT > # Sectors per side	Abnormal Termination
0	1	SC ≤ # Sectors Remaining AND EOT ≤ # Sectors per side	No Error
0	1	SC > # Sectors Remaining OR EOT > # Sectors per side	Abnormal Termination
1	0	SC = DTL EOT > # Sectors per side	No Error
1	0	SC = DTL EOT > # Sectors per side	Abnormal Termination
1	1	SC ≤ # Sectors Remaining AND EOT ≤ # Sectors per side	No Error
1	1	SC > # Sectors Remaining OR EOT > # Sectors per side	Abnormal Termination

11.4.12 Control Commands

The control commands do not transfer any data. Instead, these commands are used to monitor and manage the data transfer. Three of the Control commands generate an interrupt when finished — READ ID, RE-CALIBRATE and SEEK. It is strongly recommended that a SENSE INTERRUPT STATUS command be issued after these commands to capture their valuable interrupt information. The RE-CALIBRATE, SEEK, and SPECIFY commands do not return any result bytes.

11.4.12.1 READ ID

The READ ID command is used to find the actual recording head position. It stores the first readable ID field value into the FDC registers. If the FDC cannot find an ID Address Mark by the time a second INDEX pulse is received, an abnormal termination will be generated by setting the IC code in the ST0 to 01.

11.4.12.2 CONFIGURE

The CONFIGURE command determines some special operation modes of the controller. It needs not to be issued if the default values of the controller meet the system requirements.
EIS: Enable Implied Seeks. A SEEK operation is performed before a READ, WRITE, SCAN, or VERIFY commands.
0 = Disabled (default).
1 = Enabled.
DFIFO: Disable FIFO.
0 = Enabled.
1 = Disabled (default).
POLLD: Disable polling of the drives.

0 = Enabled (default). When enabled, a single interrupt is generated after a reset.
1 = Disabled.
FIFOTHR: The FIFO threshold in the execution phase of data transfer commands. They are programmable from 00 to 0F hex (1 bytes to 16 bytes). Defaults to one byte.
PRETRK: The Pre-compensation Start Track Number. They are programmable from track 0 to FF hex (track 0 to track 255). Defaults to track 0.

11.4.12.3 RE-CALIBRATE

The RE-CALIBRATE command retracts the FDC read/write head to the track 0 position, resetting the value of the PCN counter and checking the TK00# status. If TK00# is low, the DIR# pin remains low and step pulses are issued. If TK00# is high, SE [and EC bits] of ST0 are set high, and the command is terminated. When TK00# remains low for 79 step pulses, the RE-CALIBRATE command is terminated by setting SE and EC bits of ST0 high. Consequently, for disks that can accommodate more than 80 tracks, more than one RE-CALIBRATE command is required to retract the head to the physical track 0.

The FDC is in a non-busy state during the Execution phase of this command, making it possible to issue another RE-CALIBRATE command in parallel with the current command.

On power-up, software must issue a RE-CALIBRATE command to properly initialize the FDC and the drives attached.

11.4.12.4 SEEK

The SEEK command controls movement of the FDC read/write head movement from one track to another. The FDC compares the current head position, stored in PCN, with NCN values after each step pulse to determine what direction to move the head, if required. The direction of movement is determined below:

PCN < NCN — Step In: Sets DIR# signal to 1 and issues step pulses,
PCN > NCN — Step Out: Sets DIR# signal to 0 and issues step pulses, and
PCN = NCN — Terminate the command by setting the ST0 SE bit to 1.

The impulse rate of step pulse is controlled by Stepping Rate Time (SRT) bit in the SPECIFY command. The FDC is in a non-busy state during the Execution phase of this command, making it possible to issue another SEEK command in parallel with the current command.

11.4.12.5 RELATIVE SEEK

The RELATIVE SEEK command steps the selected drive in or out in a given number of steps. The DIR bit is used to determine to step in or out. RCN (Relative Cylinder Number) is used to determine how many tracks to step the head in or out from the current track. After the step operation is completed, the controller generates an interrupt, but the command has no Result phase. No other command except the SENSE INTERRUPT STATUS command should be issued while a RELATIVE SEEK command is in progress.

11.4.12.6 DUMPREG

The DUMPREG command is designed for system run-time diagnostics, and application software development, and debug. This command has one byte of Command phase and 10 bytes of Result phase, which return the values of parameters set in other commands.

11.4.12.7 LOCK

The LOCK command allows the programmer to fully control the FIFO parameters after a hardware reset. If the LOCK bit is set to 1, the parameters DFIFO, FIFOTHR, and PRETRK in the CONFIGURE command are not affected by a software reset. If the bit is set to 0, those parameters are set to default values after a software reset.

11.4.12.8 VERSION

The VERSION command is used to determine the controller being used. In Result phase, a value of 90 hex is returned in order to be compatible with the 82077.

11.4.12.9 SENSE INTERRUPT STATUS

The SENSE INTERRUPT STATUS command resets the interrupt signal (IRQ) generated by the FDC, and identifies the cause of the interrupt via the IC code and SE bit of the ST0, as shown in Table 11-19.

It may be necessary to generate an interrupt when any of the following conditions occur:

1. Before any Data Transfer or READ ID command
2. After SEEK or RE-CALIBRATE commands (no result phase exists)
3. When a data transfer is required during an Execution phase in the non-DMA mode

Table 11-19. Interrupt Identification

SE	IC Code	Cause of Interrupt
0	11	Polling.
1	00	Normal termination of SEEK or RE-CALIBRATE command.
1	01	Abnormal termination of SEEK or RE-CALIBRATE command.

11.4.12.10 SENSE DRIVE STATUS

The SENSE DRIVE STATUS command acquires drive status information. It has no Execution phase.

11.4.12.11 SPECIFY

The SPECIFY command sets the initial values for the HUT (Head Unload Time), HLT (Head Load Time), SRT (Step Rate Time), and ND (Non-DMA mode) parameters. The possible values for HUT, SRT, and HLT are shown in Table 11-20, Table 11-21 and Table 11-22 respectively. The FDC is operated in DMA or non-DMA mode based on the value specified by the ND parameters.

Table 11-20. HUT Values

Parameter	1 Mbps	500 Kbps	300 Kbps	250 Kbps
0	128	256	426	512
1	8	16	26.7	32
…	…	…	…	…
E	112	224	373	448
F	120	240	400	480

Table 11-21. SRT Values

Parameter	1 Mbps	500 Kbps	300 Kbps	250 Kbps
0	8	16	26.7	32
1	7.5	15	25	30
…	…	…	…	…
E	1	2	3.33	4
F	0.5	1	1.67	2

Table 11-22. HLT Values

Parameter	1 Mbps	500 Kbps	300 Kbps	250 Kbps
00	128	256	426	512
01	1	2	3.33	4
02	2	4	6.7	8
…	…	…	…	…
7E	126	252	420	504
7F	127	254	423	508

11.4.12.12 PERPENDICULAR MODE

The PERPENDICULAR MODE command is used to support the unique READ/WRITE/FORMAT commands of Perpendicular Recording disk drives (4 Mbytes unformatted capacity). This command configures each of the four logical drives as a perpendicular or conventional disk drive via the DC3-DC0 bits, or with the GAP and WG control bits. Perpendicular Recording drives operate in “Extra High Density” mode at 1Mbps, and are downward compatible with 1.44 Mbyte and 720 kbyte drives at 500 Kbps (High Density) and 250 Kbps (Double Density) respectively. This command should be issued during the initialization of the floppy disk controller. Then, when a drive is accessed for a FORMAT A TRACK or WRITE DATA command, the controller adjusts the format or Write Data parameters based on the data rate. If WG and GAP are used (not set to 00), the operation of the FDC is based on the values of GAP and WG. If WG and GAP are set to 00, setting DCn to 1 will set drive n to Perpendicular mode. DC3-DC0 are unaffected by a software reset, but WG and GAP are both cleared to 0 after a software reset.

Table 11-23. Effects of GAP and WG on FORMAT A TRACK and WRITE DATA Commands

GAP	WG	Mode	Length of GAP2 FORMAT FIELD	Portion of GAP2 Re-Written by WRITE DATA Command
0	0	Conventional	22 bytes	0 bytes
0	1	Perpendicular (500 Kbps)	22 bytes	19 bytes
1	0	Reserved (Conventional)	22 bytes	0 bytes
1	1	Perpendicular (1 Mbps)	41 bytes	38 bytes

Table 11-24. Effects of Drive Mode and Data Rate on FORMAT A TRACK and WRITE DATA Commands

Data Rate	Drive Mode	Length of GAP2 FORMAT FIELD	Portion of GAP2 Re-Written by WRITE DATA Command
250/300/500 Kbps	Conventional Perpendicular	22 bytes 22 bytes	0 bytes 19 bytes
1 Mbps	Conventional Perpendicular	22 bytes 41 bytes	0 bytes 38 bytes

11.4.12.13 INVALID

The INVALID command indicates when an undefined command has been sent to FDC. The FDC will set the bit 6 and the bit 7 in the Main Status Register to 1 and terminate the command without issuing an interrupt.

11.4.13 DMA Transfers

DMA transfers are enabled by the SPECIFY command and are initiated by the FDC by activating the DRQ cycle during a DATA TRANSFER command. The FIFO is enabled directly by asserting the DMA cycles.

11.4.14 Low Power Mode

When writing a 1 to the bit 6 of the DSR, the controller is set to low power mode immediately. All the clock sources including Data Separator, Microcontroller, and Write precompensation unit will be gated. The FDC can be resumed from the low-power state in two ways. One is a software reset via the DOR or DSR; and the other is a read or write to either the Data Register or Main Status Register. The second method is more preferred since all internal register values are retained.

11.5 Serial Port (UART) Description

The IT8673F incorporates two enhanced serial ports that perform serial to parallel conversion on received data, and parallel to serial conversion on transmitted data. Each of the serial channels individually contains a programmable baud rate generator which is capable of dividing the input clock by a number ranging from 1 to 65535. The data rate of each serial port can also be programmed from 115.2K baud down to 50 baud. The character options are programmable for 1 start bit; 1, 1.5 or 2 stop bits; even, odd, stick or no parity; and privileged interrupts.

Table 11-25. Serial Channel Registers

Register	DLAB*	Address	READ	WRITE
Data	0	Base + 0h	RBR (Receiver Buffer Register)	TBR (Transmitter Buffer Register)
Control	0	Base + 1h	IER (Interrupt Enable Register)	IER
	x	Base + 2h	IIR (Interrupt Identification Register)	FCR (FIFO Control Register)
	x	Base + 3h	LCR (Line Control Register)	LCR
	x	Base + 4h	MCR (Modem Control Register)	MCR
	1	Base + 0h	DLL (Divisor Latch LSB)	DLL
	1	Base + 1h	DLM (Divisor Latch MSB)	DLM
Status	x	Base + 5h	LSR (Line Status Register)	LSR
	x	Base + 6h	MSR (Modem Status Register)	MSR
	x	Base + 7h	SCR (Scratch Pad Register)	SCR

* DLAB is bit 7 of the Line Control Register.

11.5.1 Data Registers

The TBR and RBR individually hold from five to eight data bits. If the transmitted data is less than eight bits, it aligns to the LSB. Either received or transmitted data is buffered by a shift register, and is latched first by a holding register. The bit 0 of any word is first received and transmitted.

(1) Receiver Buffer Register (RBR) (Read only, Address offset=0, DLAB=0)

This register receives and holds the incoming data. It contains a non-accessible shift register which converts the incoming serial data stream into a parallel 8-bit word.

(2) Transmitter Buffer Register (TBR) (Write only, Address offset=0, DLAB=0)

This register holds and transmits the data via a non-accessible shift register, and converts the outgoing parallel data into a serial stream before transmission.

11.5.2 Control Registers: IER, IIR, FCR, DLL, DLM, LCR and MCR

(1) Interrupt Enable Register (IER) (Read/Write, Address offset=1, DLAB=0)

The IER is used to enable (or disable) four active high interrupts which activate the interrupt outputs with its lower four bits: IER(0), IER(1), IER(2), and IER(3).

Table 11-26. Interrupt Enable Register Description

Bit	Default	Description
7-4	-	**Reserved**
3	0	**Enable MODEM Status Interrupt** Sets this bit high to enable the Modem Status Interrupt when one of the Modem Status Registers changes its bit status.
2	0	**Enable Receiver Line Status Interrupt** Sets this bit high to enable the Receiver Line Status Interrupt which is caused when Overrun, Parity, Framing or Break occurs.
1	0	**Enable Transmitter Holding Register Empty Interrupt** Sets this bit high to enable the Transmitter Holding Register Empty Interrupt.
0	0	**Enable Received Data Available Interrupt** Sets this bit high to enable the Received Data Available Interrupt and Time-out interrupt in the FIFO mode.

(2) Interrupt Identification Register (IIR) (Read only, Address offset=2)

This register facilitates the host CPU to determine interrupt priority and its source. The priority of four existing interrupt levels is listed below:

1. Received Line Status (highest priority)
2. Received Data Ready
3. Transmitter Holding Register Empty
4. Modem Status (lowest priority)

When a privileged interrupt is pending and the type of interrupt is stored in the IIR which is accessed by the Host, the serial channel holds back all interrupts and indicates the pending interrupts with the highest priority to the Host. Any new interrupts will not be acknowledged until the Host access is completed. The contents of the IIR are described in the table on the next page:

Table 11-27. Interrupt Identification Register

FIFO Mode	Interrupt Identification Register			Interrupt Set and Reset Functions			
Bit 3	Bit 2	Bit 1	Bit 0	Priority Level	Interrupt Type	Interrupt Source	Interrupt Reset Control
0	X	X	1	-	None	None	-
0	1	1	0	First	Receiver Line Status	OE, PE, FE, or BI	Read LSR
0	1	0	0	Second	Received Data Available	Received Data Available	Read RBR or FIFO drops below the trigger level
1	1	0	0	Second	Character Time-out Indication	No characters have been removed from or input to the RCVR FIFO during the last 4 character times and there is at least 1 character in it during this time	Read RBR
0	0	1	0	Third	Transmitter Holding Register Empty	Transmitter Holding Register Empty	Read IIR if THRE is the Interrupt Source Write THR
0	0	0	0	Fourth	Modem Status	CTS#, DSR#, RI#, DCD#	Read MSR

Note: X = Not defined

IIR(7), IIR(6): Are set when FCR(0) = 1.
IIR(5), IIR(4): Always logic 0.
IIR(3): In non-FIFO mode, this bit is a logic 0. In the FIFO mode, this bit is set along with bit 2 when a time-out interrupt is pending.
IIR(2), IIR(1): Used to identify the highest priority interrupt pending.
IIR(0): Used to indicate a pending interrupt in either a hard-wired prioritized or polled FAN with a logic 0 state. In such a case, IIR contents may be used as a pointer to the appropriate interrupt service routine.

(3) FIFO Control Register (FCR) (Write Only, Address offset=2)

This register is used to enable/clear the FIFO, and set the RCVR FIFO trigger level.

Table 11-28. FIFO Control Register Description

Bit	Default	Description
7-6	-	**Receiver Trigger Level Select** These bits set the trigger levels for the RCVR FIFO interrupt.
5-4	0	**Reserved**
3	0	This bit doesn't affect the Serial Channel operation. RXRDY and TXRDY functions are not available on this chip.
2	0	**Transmitter FIFO Reset** This self-clearing bit clears all contents of the XMIT FIFO and resets its related counter to 0 via a logic "1."
1	0	**Receiver FIFO Reset** Setting this self-clearing bit to a logic “1” clears all contents of the RCVR FIFO and resets its related counter to 0 (except the shift register).
0	0	**FIFO Enable** XMIT and RCVR FIFO are enabled when this bit is set high. XMIT and RCVR FIFOs are disabled and cleared respectively when this bit is cleared to low. This bit must be a logic 1 if the other bits of the FCR are written to, or they will not be properly programmed. When this register is switched to non-FIFO mode, all its contents are cleared.

Table 11-29. Receiver FIFO Trigger Level Encoding

FCR (7)	FCR (6)	RCVR FIFO Trigger Level
0	0	1 byte
0	1	4 bytes
1	0	8 bytes
1	1	14 bytes

(4) Divisor Latches (DLL, DLM) (Read/Write, Address offset=0,1, DLAB=0)

Two 8-bit Divisor Latches (DLL and DLM) store the divisor values in a 16-bit binary format. They are loaded during the initialization to generate a desired baud rate.

(5) Baud Rate Generator (BRG)

Each serial channel contains a programmable BRG which can take any clock input (from DC to 3 MHz) to generate standard ANSI/CCITT bit rates for the channel clocking with an external clock oscillator. The DLL or DLM is a number of 16-bit format, providing the divisor range from 1 to 2^{16} to obtain the desired baud rate. The output frequency is 16X data rate.

Table 11-30. Baud Rates Using (24 MHz ÷ 13) Clock

Desired Baud Rate	Divisor Used
50	2304
75	1536
110	1047
134.5	857
150	768
300	384
600	192
1200	96
1800	64
2000	58
2400	48
3600	32
4800	24
7200	16
9600	12
19200	6
38400	3
57600	2
115200	1

(6) Scratch Pad Register (Read/Write, Address offset=7)

This 8-bit register does not control the UART operation in any way. It is intended as a scratch pad register to be used by programmers to temporarily hold general purpose data.

(7) Line Control Register (LCR) (Read/Write, Address offset=3)

LCR controls the format of the data character and supplies the information of the serial line. Its contents are described on the next page:

Table 11-31. Line Control Register Description

Bit	Default	Description
7	0	**Divisor Latch Access Bit (DLAB)** Must be set to high to access the Divisor Latches of the baud rate generator during READ or WRITE operations. It must be set low to access the Data Register (RBR and TBR) or the Interrupt Enable Register.
6	0	**Set Break** Forces the Serial Output (SOUT) to the spacing state (logic 0) by a logic 1, and this state will be preserved until a low level resetting LCR(6), enabling the serial port to alert the terminal in a communication system.
5	0	**Stick Parity** When this bit and LCR(3) are high at the same time, the parity bit is transmitted, and then detected by receiver, in opposite state by LCR(4) to force the parity bit into a known state and to check the parity bit in a known state.
4	0	**Even Parity Select** When parity is enabled (LCR(3) = 1), LCR(4) = 0 selects odd parity, and LCR(4) = 1 selects even parity.
3	0	**Parity Enable** A parity bit, located between the last data word bit and stop bit, will be generated or checked (transmit or receive data) when LCR(3) is high.
2	0	**Number of Stop Bits** Specifies the number of stop bits in each serial character, as summarized in table 11-32.
1-0	00	**Word Length Select [1:0]** 11: 8 bits 10: 7 bits 01: 6 bits 00: 5 bits

Table 11-32. Stop Bits Number Encoding

LCR (2)	Word Length	No. of Stop Bits
0	-	1
1	5 bits	1.5
1	6 bits	2
1	7 bits	2
1	8 bits	2

Note: The receiver will ignore all stop bits beyond the first, regardless of the number used in transmission.

(8) MODEM Control Register (MCR) (Read/Write, Address offset=4)

Controls the interface by the modem or data set (or device emulating a modem).

Table 11-33. Modem Control Register Description

Bit	Default	Description
7-5	-	**Reserved**
4	0	**Internal Loop Back** Provides a loopback feature for diagnostic test of the serial channel when it is set high. Serial Output (SOUT) is set to the Marking State Shift Register output loops back into the Receiver Shift Register. All Modem Control inputs (CTS#, DSR#, RI# and DCD#) are disconnected. The four Modem Control outputs (DTR#, RTS#, OUT1 and OUT2) are internally connected to the four Modem Control inputs and forced to inactive high. The transmitted data are then immediately received, allowing the processor to verify the transmit and receive data path of the serial channel.
3	0	**OUT2** This bit is the Output 2 bit and enables the serial port interrupt output by a logic 1.
2	0	**Out1** This bit does not have an output pin and can only be read or written by the CPU.
1	0	**Request to Send (RTS)** Controls the Request to Send (RTS#) which is in an inverse logic state with MCR(1).
0	0	**Data Terminal Ready (DTR)** Controls the Data Terminal ready (DTR#) which is in an inverse logic state with the MCR(0).

11.5.3 Status Registers: LSR and MSR

(1) Line Status Register (LSR) (Read/Write, Address offset=5)

This register provides status indications and is usually the first register read by the CPU to determine the cause of an interrupt or to poll the status of each serial channel. The contents of the LSR are described below:

Table 11-34. Line Status Register Description

Bit	Default	Description
7	0	**Error in Receiver FIFO** In 16450 mode, this bit is always 0. In the FIFO mode, it sets high when there is at least one parity error, framing or break interrupt in the FIFO. This bit is cleared when the CPU reads the LSR, if there are no subsequent errors in the FIFO.
6	1	**Transmitter Empty** This **read only** bit indicates that the Transmitter Holding Register and Transmitter Shift Register are both empty. Otherwise, this bit is "0," and has the same function in the FIFO mode.
5	1	**Transmitter Holding Register Empty** Transmitter Holding Register Empty (THRE). This **read only** bit indicates that the TBR is empty and is ready to accept a new character for transmission. It is set high when a character is transferred from the THR into the Transmitter Shift Register, causing a priority 3 IIR interrupt which is cleared by a read of IIR. In the FIFO mode, it is set when the XMIT FIFO is empty and is cleared when at least one byte is written to the XMIT FIFO.
4	0	**Line Break** Break Interrupt (BI) status bit indicates that the last character received was a break character, (invalid but entire character), including parity and stop bits. This occurs when the received data input is held in the spacing (logic 0) for longer than a full word transmission time (start bit + data bits + parity + stop bit). When any of these error conditions is detected (LSR(1) to LSR(4)), a Receiver Line Status interrupt (priority 1) will be generated in the IIR with the IER(2) enabled previously.
3	0	**Framing Error** Framing Error (FE) bit, a logic 1, indicates that the stop bit in the received character was not valid. It resets low when the CPU reads the contents of the LSR.
2	0	**Parity Error** The parity error (PE) indicates by with a logic 1 that the received data character does not have the correct even or odd parity, as selected by LCR(4). It will be reset to "0" whenever the LSR is read by the CPU.
1	0	**Overrun Error** Overrun Error (OE) bit indicates by a logic 1 that the RBR has been overwritten by the next character before it had been read by the CPU. In the FIFO mode, the OE occurs when the FIFO is full and the next character has been completely received by the Shift Register. It will be reset when the LSR is read by the CPU.
0	0	**Data Ready** A "1" indicates a character has been received by the RBR. And a logic "0" indicates all the data in the RBR or the RCVR FIFO have been read.

(2) MODEM Status Register (MSR) (Read/Write, Address offset=6)

This 8-bit register indicates the current state of the control lines with modems or peripheral devices in addition to this current state information. Four of these eight bits MSR(4) - MSR(7) can provide the state change information when a modem control input changes state. It is reset low when the Host reads the MSR.

Table 11-35. Modem Status Register Descriptiopn

Bit	Default	Description
7	0	**Data Carrier Detect** Data Carrier Detect - Indicates the complement status of Data Carrier Detect (DCD#) input. If MCR(4) = 1, MSR(7) is equivalent to OUT2 of the MCR.
6	0	**Ring Indicator** Ring Indicator (RI#) - Indicates the complement status to the RI# input. If MCR(4)=1, MSR(6) is equivalent to OUT1 in the MCR.
5	0	**Data Set Ready** Data Set Ready (DSR#) - Indicates that the modem is ready to provide received data to the serial channel receiver circuitry. If the serial channel is in the loop mode (MCR(4) = 1), MSR(5) is equivalent to DTR# in the MCR.
4	0	**Clear to Send** Clear to Send (CTS#) - Indicates the complement of CTS# input. When the serial channel is in the loop mode (MCR(4)=1), MSR(5) is equivalent to RTS# in the MCR.
3	0	**Delta Data Carrier Detect** Indicates that the DCD# input state has been changed since the last time read by the Host.
2	0	**Trailing Edge Ring Indicator** Indicates that the RI input state to the serial channel has been changed from a low to high since the last time read by the Host. The change to logic 1 does not activate the TERI.
1	0	**Delta Data Set Ready** Delta Data Set Ready (DDSR) - A logic "1" indicates that the DSR# input state to the serial channel has been changed since the last time read by the Host.
0	0	**Delta Clear to Send** This bit indicates the CTS# input to the chip has changed state since the last time the MSR was read.

11.5.4 Reset

The reset of the IT8673F should be held to an idle mode reset high for 500 ns until initialization, and this causes the initialization of the transmitter and receiver internal clock counters.

Table 11-36. Reset Control of Registers and Pinout Signals

Register/Signal	Reset Control	Reset Status
Interrupt Enable Register	Reset	All bits Low
Interrupt Identification Register	Reset	Bit 0 is high and bits 1-7 are low
FIFO Control Register	Reset	All bits Low
Line Control Register	Reset	All bits Low
Modem Control Register	Reset	All bits Low
Line Status Register	Reset	Bits 5 and 6 are high, others are low
Modem Status Register	Reset	Bits 0-3 low, bits 4-7 input signals
SOUT1, SOUT2	Reset	High
RTS0#, RTS1#, DTR0#, DTR1#	Reset	High
IRQ of Serial Port	Reset	High Impedance

11.5.5 Programming

Each serial channel of the IT8673F is programmed by control registers, whose contents define the character length, number of stop bits, parity, baud rate and modem interface. Even though the control register can be written in any given order, the IER should be the last register written because it controls the interrupt enables. After the port has been programmed, these registers can still be updated whenever the port is not transferring data.

11.5.6 Software Reset

This approach allows the serial port returning to a completely known state without a system reset. This is achieved by writing the required data to the LCR, DLL, DLM and MCR. The LSR and RBR must be read before enabling interrupts to clear out any residual data or status bits that may be invalid for subsequent operations.

11.5.7 Clock Input Operation

The input frequency of the Serial Channel is 24 MHz ÷ 13, not exactly 1.8432 MHz.

11.5.8 FIFO Interrupt Mode Operation

(1) RCVR Interrupt

When setting FCR(0)=1 and IER(0)=1, the RCVR FIFO and receiver interrupts are enabled. The RCVR interrupt occurs under the following conditions:

a. The receive data available interrupt and the IIR, receive data available indication, will be issued only if the FIFO has reached its programmed trigger level. They will be cleared as soon as the FIFO drops below its trigger level

b. The receiver line status interrupt has higher priority over the received data available interrupt

c. The time-out timer will be reset after receiving a new character or after the Host reads the RCVR FIFO whenever a time-out interrupt occurs. The timer will be reset when the Host reads one character from the RCVR FIFO

RCVR FIFO time-out Interrupt: By enabling the RCVR FIFO and receiver interrupts, the RCVR FIFO time-out interrupt will occur under the following conditions:

a. The RCVR FIFO time-out interrupt will occur only if there is at least one character in the FIFO whenever the interval between the most recent received serial character and the most recent Host READ from the FIFO is longer than four consecutive character times

b. The RLCK clock signal input is used to calculate character times

c. The time-out timer will be reset after receiving a new character or after the Host reads the RCVR FIFO whenever any time-out interrupt occurs. The timer will be reset when the Host reads one character from the RCVR FIFO

(2) XMIT Interrupt

By setting FCR(0) and IER(1) to high, the XMIT FIFO and transmitter interrupts are enabled, and the XMIT interrupt occurs under the conditions described below:

a. The transmitter interrupt occurs when the XMIT FIFO is empty, and it will be reset if the THR is written or the IIR is read.

b. The transmitter FIFO empty indications will be delayed one character time minus the last stop bit time whenever the following condition occurs: THRE = 1 and there have not been at least two bytes in the transmitter FIFO at the same time since the last THRE = 1. The transmitter interrupt after changing FCR(0) will be immediate, if it is enabled. Once the first transmitter interrupt is enabled, the THRE indication is delayed one character time minus the last stop bit time.

The character time-out and RCVR FIFO trigger level interrupts are in the same priority order as the received data available interrupt. The XMIT FIFO empty is in the same priority as the transmitter holding register empty interrupt.

FIFO Polled Mode Operation [FCR(0)=1, and IER(0), IER(1), IER(2), IER(3) or all are “0”]

Either or both XMIT and RCVR can be in this operation mode. The operation mode can be programmed by users and is responsible for checking the RCVR and XMIT status via the LSR described below:

LSR(7): RCVR FIFO error indication
LSR(6): XMIT FIFO and Shift register empty
LSR(5): The XMIT FIFO empty indication
LSR(4) - LSR(1): Specify that errors have occurred. Character error status is handled in the same way as in the interrupt mode. The IIR is not affected since IER(2)=0.
LSR(0): This bit is high whenever the RCVR FIFO contains at least one byte.

No trigger level is reached or time-out condition indicated in the FIFO Polled Mode.

11.6 Parallel Port

The IT8673F supports the IBM AT, PS/2 compatible bi-directional standard parallel port (SPP), the Enhanced Parallel Port (EPP) and the Extended Capabilities Port (ECP). Refer to the IT8673F Configuration registers and Hardware Configuration Description for information on the following: enabling/disabling, changing the base address of the parallel port, and operation mode selection.

Table 11-37. Parallel Port Connector in Different Modes

Host Connector	Pin No.	SPP	EPP	ECP
1	96	STB#	WRITE#	nStrobe
2-9	91-84	PD0 - 7	PD0 - 7	PD0 - 7
10	82	ACK#	INTR	nAck
11	81	BUSY	WAIT#	Busy PeriphAck(2)
12	80	PE	(NU) (1)	PError nAckReverse(2)
13	79	SLCT	(NU) (1)	Select
14	95	AFD#	DSTB#	nAutoFd HostAck(2)
15	94	ERR#	(NU) (1)	nFault nPeriphRequest(2)
16	93	INIT#	(NU) (1)	nInit nReverseRequest(2)
17	92	SLIN#	ASTB#	nSelectIn

Notes : 1. NU : Not used
2. Fast mode
3. For more information, please refer to the IEEE 1284 standard.

11.6.1 SPP and EPP Modes

Table 11-38. Address Map and Bit Map for SPP and EPP Modes

Register	Address	I/O	D0	D1	D2	D3	D4	D5	D6	D7	Mode
Data Port	Base+0h	R/W	PD0	PD1	PD2	PD3	PD4	PD5	PD6	PD7	SPP/EPP
Status Port	Base+1h	R	TMOUT	1	1	ERR#	SLCT	PE	ACK#	BUSY#	SPP/EPP
Control Port	Base+2h	R/W	STB	AFD	INIT	SLIN	IRQE	PDDIR	1	1	SPP/EPP
EPP Address Port	Base+3h	R/W	PD0	PD1	PD2	PD3	PD4	PD5	PD6	PD7	EPP
EPP Data Port0	Base+5h	R/W	PD0	PD1	PD2	PD3	PD4	PD5	PD6	PD7	EPP
EPP Data Port1	Base+5h	R/W	PD0	PD1	PD2	PD3	PD4	PD5	PD6	PD7	EPP
EPP Data Port2	Base+6h	R/W	PD0	PD1	PD2	PD3	PD4	PD5	PD6	PD7	EPP
EPP Data Port3	Base+7h	R/W	PD0	PD1	PD2	PD3	PD4	PD5	PD6	PD7	EPP

Note 1. The Base Address depends on the Logical Device configuration registers of Parallel Port (0X60, 0X61).

(1) Data Port (Primary Base Address + 00h)

This is a bi-directional 8-bit data port. The direction of data flow is determined by the bit 5 of the logic state of the control port register. It forwards directions when the bit is low and reverses directions when the bit is high.

(2) Status Port (Primary Base Address + 01h)

This is a **read only** register. Writing to this register has no effects. The contents of this register are latched during an IOR cycle.

Bit 7 - BUSY#: Inverse of printer BUSY signal, a logic "0" means that the printer is busy and cannot accept another character. A logic "1" means that it is ready to accept the next character.
Bit 6 - ACK#: Printer acknowledge, a logic "0" means that the printer has received a character and is ready to accept another. A logic "1" means that it is still processing the last character.
Bit 5 - PE: Paper end, a logic "1" indicates the paper end.
Bit 4 - SLCT: Printer selected, a logic "1" means that the printer is on line.
Bit 3 - ERR#: Printer error signal, a logic "0" means an error has been detected.
Bits 1, 2: Reserved, these bits are always "1" when read.
Bit 0 - TMOUT: This bit is valid only in EPP mode and indicates that a 10-msec time-out has occurred in EPP operation. A logic "0" means no time-out occurred and a logic “1” means that a time-out error has been detected. This bit is cleared by a RESET or by writing a logic “1” to it. When the IT8673F are selected to non-EPP mode (SPP or ECP), this bit is always logic "1" when read.

(3) Control Port (Primary Base Address +02h)

This port provides all output signals to control the printer. The register can be read and written.

Bits 7, 6 : Reserved, these two bits are always "1" when read.
Bit 5 PDDIR: Data port direction control, this bit determines the direction of the data port. Set this bit "0" to output the data port to PD bus and "1" to input from PD bus.
Bit 4 IRQE: Interrupt request enable, setting this bit "1" enables the interrupt requests from the parallel port to the Host. An interrupt request is generated by a "0" to "1" transition of the ACK# signal.
Bit 3 SLIN: Inverse of SLIN# pin, setting this bit to "1" selects the printer.
Bit 2 INIT: Initiate printer, setting this bit to "0" initializes the printer.

Bit 1 AFD: Inverse of the AFD# pin, setting this bit to "1" causes the printer to automatically feed after each

line is printed.
Bit 0 STB: Inverse of the STB# pin, this pin controls the data strobe signal to the printer.

(4) EPP Address Port (Primary Base Address + 03h)

The EPP Address Port is only available in the EPP mode. When the Host writes to this port, the contents of D0 -D7 are buffered and output to PD0 - PD7. The leading edge of IOW causes an EPP ADDRESS WRITE cycle. When the Host reads from this port, the contents of PD0 - PD7 are read. The leading edge of IOR causes an EPP ADDRESS READ cycle.

(5) EPP Data Ports 0-3 (Primary Base Address + 04h - 07h)

The EPP Data Ports are only available in the EPP mode. When the Host writes to these ports, the contents of D0 - D7 are buffered and output to PD0 - PD7. The leading edge of IOW causes an EPP DATA WRITE cycles. When the Host reads from these ports, the contents of PD0 - PD7 are read. The leading edge of IOR causes an EPP DATA READ cycle.

11.6.2 EPP Operation

When the parallel port of the IT8673F is selected to be in the EPP mode, the SPP mode is also available.

Address/Data Port address is decoded (Base address + 03h- 07h), the PD bus is in the SPP mode, and the output signals such as STB#, AFD#, INIT#, and SLIN# are set by SPP control port. The direction of the data port is controlled by the bit 5 of the control port register. A 10-msec time is required to prevent the system from lockup. The time has elapsed from the beginning of the IOCHRDY high (EPP READ/WRITE cycle) to WAIT# being deasserted. If a time-out occurs, the current EPP READ/WRITE cycle is aborted and a logic "1" will be read in the bit 0 of the status port register. The Host must write 0 to bits 0, 1, 3 of the control port register before any EPP READ/WRITE cycle (EPP spec.) The pins STB#, AFD# and SLIN# are controlled by hardware for the hardware handshaking during EPP READ/WRITE cycle.

(1) EPP ADDRESS WRITE

1. The Host writes a byte to the EPP Address Port (Base address + 03h). The chip drives D0 - D7 onto PD0 - PD7.

2. The chip drives IOCHRDY low and asserts WRITE (STB#) and ASTB# (SLIN#) after IOW is active.

3. Peripheral deasserts WAIT#, indicating that the chip may begin the termination of this cycle. The chip then deasserts ASTB#, latches the address from D0 - D7 to PD bus and releases IOCHRDY, allowing the Host to complete the I/O WRITE cycle.

4. Peripheral asserts WAIT#, indicating that it acknowledges the termination of the cycle. The chip then deasserts WRITE to terminate the cycle.

(2) EPP ADDRESS READ

1. The Host reads a byte from the EPP Address Port. The chip drives the PD bus to tri-state for the peripheral to drive.

2. The chip drives IOCHRDY low and asserts ASTB# after IOR is active.

3. Peripheral drives the PD bus valid and deasserts WAIT#, indicating that the chip may begin to terminate this cycle. The chip then deasserts ASTB#, latches the address from PD bus to D0 -D7 and releases IOCHRDY, allowing the Host to complete the I/O READ cycle.

4. Peripheral drives the PD bus to tri-state and then asserts WAIT#, indicating that it acknowledges the termination of the cycle.

(3) EPP DATA WRITE

1. The host writes a byte to the EPP Data Port (Base address +04H - 07H). The chip drives D0- D7 onto PD0 -PD7.

2. The chip drives IOCHRDY low and asserts WRITE# (STB#) and DSTB#(AFD#) after IOW becomes active.

3. The peripheral deasserts WAIT#, indicating that the chip may begin the termination of this cycle. The chip then deasserts DSTB#, latches the data from D0 - D7 to the PD bus and releases IOCHRDY, allowing the Host to complete the I/O WRITE cycle.

4. The peripheral asserts WAIT#, indicating that it acknowledges the termination of the cycle. The chip then deasserts WRITE to terminate the cycle.

(4) EPP DATA READ

1. The Host reads a byte from the EPP DATA Port. The chip drives PD bus to tri-state for peripheral to drive.

2. The chip drives IOCHRDY low and asserts DSTB# after IOR is active.

3. The peripheral drives PD bus valid and deasserts WAIT#, indicating that the chip may begin the termination of this cycle. The chip then deasserts DSTB#, latches the data from PD bus to D0 - D7 and releases IOCHRDY allowing the host to complete the I/O READ cycle.

4. The peripheral tri-states the PD bus and then asserts WAIT#, indicating that it acknowledges the termination of the cycle.

11.6.3 ECP Mode

This mode is both software and hardware compatible with the existing parallel ports, allowing ECP to be used as a standard LPT port when ECP is not required. It provides an automatic high-burst-bandwidth channel that supports DMA or ECP mode in both forward and reverse directions. A 16-byte FIFO is implemented in both forward and reverse directions to smooth data flow and enhance the maximum bandwidth allowed. The port supports an automatic handshaking for the standard parallel port to improve compatibility and increase the speed of mode transfer. It also supports run-length encoded (RLE) decompression in hardware. Compression is accomplished by counting identical bytes and transmitting an RLE byte that indicates how many times a byte has been repeated. The IT8673F does not support hardware RLE compression. Please refer to "Extended Capabilities Port Protocol and ISA Interface Standard" for a detailed description.

Table 11-39. Bit Map of the ECP Registers

Register	D7	D6	D5	D4	D3	D2	D1	D0
data	PD7	PD6	PD5	PD4	PD3	PD2	PD1	PD0
ecpAFifo	Addr/RLE	Address or RLE field						
dsr	nBusy	nAck	PError	Select	nFault	1	1	1
dcr	1	1	PPDIR	IRQE	SelectIn	nInit	AutoFd	Strobe
cFifo	Parallel Port Data FIFO							
ecpDFifo	ECP Data FIFO							
tFifo	Test FIFO							
cnfgA	0	0	0	1	0	0	0	0
cnfgB	0	intrValue	0	0	0	0	0	0
ecr	mode			nErrIntrEn	dmaEn	ServiceIntr	full	empty

(1) ECP Register Definitions

Table 11-40. ECP Register Definitions

Name	Address	I/O	ECP Mode	Function
data	Primary Base +0H	R/W	000-001	Data Register
ecpAFIFO	Primary Base +0H	R/W	011	ECP FIFO (Address)
dsr	Primary Base +1H	R/W	All	Status Register
dcr	Primary Base +2H	R/W	All	Control Register
cFifo	Secondary Base +0H	R/W	010	Parallel Port Data FIFO
ecpDFIFO	Secondary Base +0H	R/W	011	ECP FIFO (DATA)
tFifo	Secondary Base +0H	R/W	110	Test FIFO
cnfgA	Secondary Base +0H	R	111	Configuration Register A
cnfgB	Secondary Base +1H	R/W	111	Configuration Register B
ecr	Secondary Base +2H	R/W	All	Extended Control Register

Note 1: The Primary base address is selected by configuration registers (0X60, 0X61). The Secondary base address is selected by configuration registers (0X62, 0X63).

(2) ECP Mode Descriptions

Table 11-41. ECP Mode Descriptions

Mode	Description
000	Standard Parallel Port Mode
001	PS/2 Parallel Port Mode
010	Parallel Port FIFO Mode
011	ECP Parallel Port Mode
110	Test Mode
111	Configuration Mode

Note: Please refer to the ECP Register Description from page 106 to 107 for detailed descriptions of the mode selection.

(3) ECP Pin Descriptions

Table 11-42. ECP Pin Descriptions

Name	Type	Description
nStrobe (HostClk)	O	Used for handshaking with Busy to write data and addresses into the peripheral device.
PD0-PD7	I/O	Address or data or RLE data.
nAck (PeriphClk)	I	Used for handshaking with nAutoFd to transfer data from the peripheral device to the Host.
Busy (PeriphACK)	I	The peripheral uses this signal for flow control in the forward direction (hand-shaking with nStrobe). In the reverse direction, this signal is used to determine whether a command or data information is present on PD0-PD7.
PError (nAckReverse)	I	Used to acknowledge nInit from the peripheral which drives this signal low, allowing the host to drive the PD bus.
Select	I	Printer On-Line indication.
nAutoFd (HostAck)	O	In the reverse direction, it is used for handshaking between the nAck and the Host. When it is asserted, a peripheral data byte is requested. In the forward direction, this signal is used to determine whether a command or data information is present on PD0-PD7.
nFault (nPeriphRequest)	I	In the forward direction (only), the peripheral is allowed (but not required) to assert this signal (low) to request a reverse transfer while in ECP mode. The signal provides a mechanism for peer-to-peer communication. It is typically used to generate an interrupt to the host, which has the ultimate control over the transfer direction.
nInit (nReverseRequest)	O	The host may drive this signal low to place the PD bus in the reverse direction. In the ECP mode, the peripheral is permitted to drive the PD bus when nInit is low and nSelectIn is high.
nSelectIn (1284 Active)	O	Always inactive (high) in the ECP mode.

(4) Data Port (Primary Base+0h, Modes 000 and 001)

Its contents will be cleared by a RESET. In a write operation, the contents of the data bus are latched by Data Register at the rising edge of the IOW# input. The contents are then sent without being inverted to PD0-PD7. The contents of data ports are read and sent to the host in a read operation.

(5) ecpAFifo PORT (Address/RLE) (Primary Base+0h, Mode 011)

Any data byte written to this port are placed in the FIFO and tagged as an ECP Address/RLE. The hardware then sends this data automatically to the peripheral. The operation of this port is only valid in forward direction (dcr(5)=0).

(6) Device Status Register (dsr) (Primary Base+1h, Mode All)

Bits 0, 1 and 2 of this register are not implemented. These bit states remain at high in a read operation of Printer Status Register.
dsr(7):This bit is the inverted level of the Busy input.
dsr(6): This bit is the state of the nAck input.
dsr(5): This bit is the state of the PError input.
dsr(4): This bit is the state of the Select input.
dsr(3): This bit is the state of the nFault input.
dsr(2)-dsr(0): These bits are always 1.

(7) Device Control Register (dcr) (Primary Base+2h, Mode All)

Bits 6 and 7 of this register supply no function. They are set high during the read operation, and cannot be written. Contents in bits 0-5 are initialized to 0 when the RESET pin is active.

dcr(7)-dcr(6) : These two bits are always high.
dcr(5) : Except in modes 000 and 010, setting this bit low means that the PD bus is in output operation; setting it high, in input operation. This bit will be forced low in mode 000.
dcr(4): Setting this bit high enables the interrupt request from the peripheral to the host due to a rising edge of the nAck input.
dcr(3): It is inverted and output to the pin nSelectIn.
dcr(2): It is output to the pin nInit without inversion.
dcr(1): It is inverted and output to the pin nAutoFd.
dcr(0): It is inverted and output to the pin nStrobe.

(8) Parallel Port Data FIFO (cFifo) (Secondary Base+0h, Mode 010)

Bytes written or DMA transferred from the Host to this FIFO are sent by a hardware handshaking to the peripheral according to the standard parallel port protocol. This operation is only defined for the forward direction.

(9) ECP Data FIFO (ecpDFifo) (Secondary Base+0h, Mode 011)

When the direction bit dcr(5) is 0, bytes written or DMA transferred from the Host to this FIFO are sent by a hardware handshaking to the peripheral according to the ECP parallel port protocol. When the dcr(5) is 1, data bytes from the peripheral to this FIFO are read in an automatic hardware handshaking. The Host can acquire these bytes by performing read operations or DMA transfers from this FIFO.

(10) Test FIFO Mode (tFifo) (Secondary Base+0h, Mode 110)

The Host may operate **read/write** or DMA transfers to this FIFO in any direction. Data in this FIFO will be displayed on the PD bus without using hardware protocol handshaking. The tFifo will not accept new data after it is full. Performing a read operation from an empty tFifo causes the last data byte to return.

(11) Configuration Register A (cnfgA) (Secondary Base+0h, Mode 111)

This **read only** register indicates to the system that interrupts are ISA-Pulses. This is an 8-bit implementation by returning a 10h.

(12) Configuration Register B (cnfgB) (Secondary Base+1h, Mode 111)

This register is **read only**.

cnfgB(7): A logic “0” read indicates that the chip does not support hardware RLE compression.
cnfgB(6):Returns the value on the ISA IRQ line to warn possible conflicts.
cnfgB(5)-cnfgB(3): A value 000 read indicates that the interrupt must be selected with jumpers.
cnfgB(2)-cnfgB(0): A value 000 read indicates that the DMA channel is a jumpered 8-bit DMA.

(13) Extended Control Register (ECR) (Secondary Base+2h, Mode All)

Table 11-43. Extended Control Register (ECR) Mode and Description

ECR	Mode and Description
000	Standard Parallel Port Mode. The FIFO is reset and the direction bit dcr(5) is always “0” (forward direction) in this mode.
001	PS/2 Parallel Port Mode. It is similar to the SPP mode except that the dcr(5) is **read/write**. When dcr(5) is “1”, the PD bus is tri-state. Reading the data port returns the value on the PD bus instead of the value of the data register.
010	Parallel Port Data FIFO Mode. This mode is similar to the 000 mode, except that the Host writes or DMA transfers the data bytes to the FIFO. The FIFO data is then automatically sent to the peripheral using the standard parallel port protocol. This mode is only valid in the forward direction (dcr(5)=0)
011	ECP Parallel Port Mode. In the forward direction, bytes placed into the ecpDFifo and ecpAFifo are stored in a single FIFO and automatically sent to the peripheral under the ECP protocol. In the reverse direction, bytes are sent to the ecpDFifo from ECP port.
100, 101	Reserved, not defined.
110	Test mode. In this mode, the FIFO may be read from or written to, but it cannot be sent to the peripheral.
111	Configuration mode. In this mode, the cnfgA and cnfgB registers are accessible at 0x400 and 0x401.

ECP function control register.

ecr(7)-ecr(5): These bits are used for **read/write** and Mode selection.

ecr(4): nErrIntrEn, **read/write**, Valid in ECP(011) Mode

1: Disables the interrupt generated on the asserting edge of the nFault input.
0: Enables the interrupt pulse on the asserting edge of the nFault. An interrupt pulse will be generated if nFault is asserted, or if this bit is written from "1" to "0" in the low level nFault.

ecr(3): dmaEn, **read/write**

1: Enables DMA. DMA starts when serviceIntr (ecr(2)) is 0.
0: Disables DMA unconditionally.

ecr(2): serviceIntr, **read/write**

1: Disables DMA and all service interrupts.
0: Enables the service interrupts. This bit will be set to 1 by hardware when one of the three service interrupts has occurred. Writing "1" to this bit will not generate an interrupt.

Case 1: dmaEn=1

During DMA, this bit is set to "1" (a service interrupt generated) if the terminal count is reached.

Case 2: dmaEn=0, dcr(5)=0

This bit is set to "1" (a service interrupt generated) whenever there is writeiIntrThreshold or more space-free bytes in the FIFO.

Case 3: dmaEn=0, dcr(5)=1

This bit is set to 1 (a service interrupt generated) whenever there is READIntrThreshold or more valid bytes to be read from the FIFO.

ecr(1): full, **read only**

1: The FIFO is full and cannot accept another byte.
0: The FIFO has at least one free data byte space.

ecr(0): empty, **read only**

1: The FIFO is empty.
0: The FIFO contains at least one data byte.

(14) Mode Switching Operation

In programmed I/O control (mode 000 or 001), P1284 negotiation and all other tasks happening before data are transferred, and are controlled by software. Setting mode to 011 or 010 will cause the hardware to perform an automatic control-line handshaking and transferring information between the FIFO and the ECP port.

From mode 000 or 001, any other mode may be immediately switched to or any other mode. To change directions, the mode must first be set to 001.

In extended forward mode, the FIFO must be cleared and all signals deasserted before returning to mode 000 or 001. In the ECP reverse mode, all data must be read from the FIFO before returning to mode 000 or 001. Unneeded data are usually accumulated during ECP reverse handshaking, as when the mode is changed during a data transfer. If the above condition is satisfied, nAutoFd will be deasserted regardless

of the transfer state. To avoid bugs during handshaking, these guidelines must be followed.

(15) Software Operation (ECP)

Before the ECP operation can begin, it is first necessary for the Host to switch the mode to 000 to negotiate with the parallel port. Host determines whether the peripheral supports the ECP protocol during the process.

After the negotiation is completed, the mode is set to 011 (ECP). To enable the drivers, the direction must be set to 0. Both strobe and autoFd are set to 0, causing the nStrobe and nAutoFd signals to be deasserted.

All FIFO data transfers are PWord wide and PWord aligned. Permitted only in the forward direction, Address/RLE transfers are byte-wide. ECP address/RLE bytes may be automatically transmitted by writing to the ecpAFifo. Similarly, data PWords may be sent automatically via the ecpDFifo.

To change directions, the Host switches mode to 001. It then negotiates either the forward or reverse channel, sets direction to “1” or “0”, and finally switches mode to 001. If the direction is set to 1, the hardware performs a handshaking for each ECP data byte READ, and tries to fill the FIFO. At this time, PWords may be read from the ecpDFifo while it retains data. It is also possible for the hardware to perform the ECP transfers by handshaking with individual bytes under programmed control in mode = 001, or 000, even though this is a comparatively time-consuming approach.

(16) Hardware Operation (DMA)

The Standard PC DMA protocol is followed. As in the programmed I/O case, the software sets direction and state. Next, the desired count and memory address are programmed into DMA controller. The dmaEn is set to 1, and the serviceIntr is set to “0”. To complete the process, the DMA channel with the DMA controller is unmasked. The contents in the FIFO are emptied or filled by DMA using the right mode and direction.

DMA is always transferred to or from the FIFO located at 0 x 400. By generating an interrupt and asserting a serviceIntr, DMA is disabled when the DMA controller reaches the terminal count. By not asserting LDRQ# for more than 32 consecutive DMA cycles, blocking of refresh requests is eliminated.

When it is necessary to disable a DMA while this is performing a data transfer, the host DMA controller is disabled serviceIntr is then set to”1”, and dmaEn is next set to 0. The DMA will start again whether or not the contents in FIFO are empty or full. This is done first by enabling the host DMA controller, then setting dmaEn to “1”. The procedure is completed with serviceIntr set to 0. Upon the completion of a DMA transfer in the forward direction, the software program must wait until the contents in FIFO are empty and the busy line is low to ensure that all data reach the peripheral device successfully.

(17) Interrupts

When any of the following states are reached, it is necessary to generate an interrupt.

1. serviceIntr = 0, dmaEn = 0, direction = 0, and the number of PWords in the FIFO is greater than or equal to writeIntrThreshold.

2. serviceIntr = 0, dmaEn = 0, direction = 1, and the number of PWords in the FIFO is greater than or equal to readIntrThreshold.

3. serviceIntr = 0, dmaEn = 1, and DMA reaches the terminal count.

4. nErrIntrEn = 0 and nFault goes from high to low or when nErrIntrEn is set from “1” to “0” and nFault is asserted.

5. ackIntEn = 1. In current implementations of using existing parallel ports, the generated interrupt may be either edge trigger or level trigger type, making it "ISA-friendly".

(18) Interrupt Driven Programmed I/O

It is also possible to use an interrupt-driven programmed I/O to execute either ECP or parallel port FIFOs. An interrupt will occur in the forward direction when serviceIntr is 0 and the number of free PWords in the FIFO is equal to or greater than writeIntrThreshold. If either of these conditions is not met, it may be filled with writeIntrThreshold PWords. An interrupt will occur in the reverse direction when serviceIntr is “0” and the number of available PWords in the FIFO is equal to READIntrThreshold. If it is full, the FIFO can be emptied completely in a single burst. If it is not full, only a number of PWords equal to READIntrThreshold may be read from the FIFO in a single burst. In the Test mode, software can determine the values of writeIntrThreshold, READIntrThreshold, and FIFO depth while accessing the FIFO.

Any PC ISA implementation that is adjusted to expedite DMA or I/O transfer must ensure that the bandwidth on the ISA is maintained on the interface. Although the PC ISA bus cannot be directly controlled, the interface bandwidth of the ECP port can be constrained to perform at the optimum speed.

(19) Standard Parallel Port

In the forward direction with DMA, the standard parallel port is run at or close to the permitted peak bandwidth of 500 Kbytes/sec. The state machine does not examine nAck, but just begins the next DMA based on the Busy signal.

11.7 Keyboard Controller (KBC)

The keyboard controller is implemented using an 8-bit microcontroller which is capable of executing the 8042 instruction set. For general information, please refer to the description of the 8042 in the 8-bit controller handbook. In addition, the microcontroller can enter power-down mode by executing two kinds of power-down instructions. The 8-bit microcontroller has 256 bytes of RAM for data memory and 2 Kbytes of ROM for the program storage.

The ROM codes may come from various vendors (or users), and are programmed during the manufacturing process. To assist in developing ROM codes, the keyboard controller has an external access mode. In the external access mode, the internal ROM is disabled and the instructions executed by the microcontroller come from an externally connected ROM.

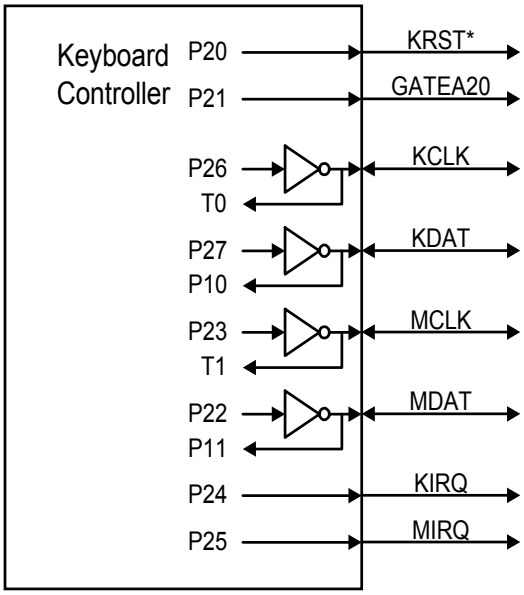


Figure 11-1. Keyboard and Mouse Interface

11.7.1 Host Interface

The keyboard controller interfaces with the system through the 8042 style host interface. The table below shows how the interface decodes the control signals.

Table 11-44. Data Register READ/WRITE Controls

Host Address(Note)	R/W*	Function
60h	R	READ DATA
60h	W	WRITE DATA, (Clear F1)
64h	R	READ Status
64h	W	WRITE Command, (set F1)

Note: These are the default values of the LDN5, 60h and 61h (DATA); LDN5, 62h and 63h (Command). All these registers are programmable.

READ DATA: This is an 8-bit **read only** register. When read, the KIRQ output is cleared and OBF flag in the status register is cleared.
WRITE DATA: This is an 8-bit **write only** register. When written, the F1 flag of the Status register is cleared and the IBF bit is set.
READ Status: This is an 8-bit **read only** register. Refer to the description of the Status register for more information.
WRITE Command: This is an 8-bit **write only** register. When written, both F1 and IBF flags of the Status register are set.

11.7.2 Data Registers and Status Register

The keyboard controller provides two data registers, one is DBIN for data input, the other is DBOUT for data output. Each of the data registers are 8-bit wide. A write (microcontroller) to the DBOUT will load Keyboard Data Read Buffer, set OBF flag and set the KIRQ output. A read (microcontroller) of the DBIN will read the data from the Keyboard Data or Command Write Buffer and clear the IBF flag.

The status register holds information concerning the status of the data registers, the internal flags, and some user-defined status bits. Please refer to Table 11-45. The bit 0 OBF is set to "1" when the microcontroller writes a data into DBOUT, and is cleared when the system initiates a DATA READ operation. The bit 1 IBF is set to "1" when the system initiates a WRITE operation, and is cleared when the microcontroller executes an "IN A, DBB" instruction. The F0 and F1 flags can be set or reset when the microcontroller executes the clear and complement flag instructions. F1 also holds system WRITE information when the system performs WRITE operations.

Table 11-45. Status Register

7	6	5	4	3	2	1	0
ST7	ST6	ST5	ST4	F1	F0	IBF	OBF

11.7.3 Keyboard and Mouse Interface

KCLK is the keyboard clock pin; its output is the inversion of pin P26 of the microcontroller, and the input of KCLK is connected to the T0 pin of the microcontroller. KDAT is the keyboard data pin; its output is the inversion of pin P27 of the microcontroller, and the input of KDAT is connected to the P10 of the microcontroller. MCLK is the mouse clock pin; its output is the inversion of pin P23 of the microcontroller, and the input of MCLK is connected to the T1 pin of the microcontroller. MDAT is the Mouse data pin; its output is the inversion of pin P22 of the microcontroller, and the input of MDAT is connected to the P11 of the microcontroller. KRST# is pin P20 of the microcontroller. GATEA20 is the pin P21 of the microcontroller. These two pins are used as a software controlled or user defined outputs. External pull-ups may be required for these pins.

11.7.4 KIRQ and MIRQ

KIRQ is the interrupt request for keyboard (Default IRQ1), and MIRQ is the interrupt request for mouse (Default IRQ12). KIRQ is internally connected to P24 pin of the microcontroller, and MIRQ is internally connected to pin P25 of the microcontroller.

11.8 Consumer Remote Control (TV Remote) IR (CIR)

11.8.1 Overview

The CIR is used in Consumer Remote Control equipment, and is a programmable amplitude shift keyed (ASK) serial communication protocol. By adjusting frequencies, baud rate divisor values and sensitivity ranges, the CIR registers are able to support the popular protocols such as RC-5, NEC, and RECS-80. Software driver programming can support new protocols.

11.8.2 Features

- Supports 30 kHz-57 kHz (low frequency) or 400 kHz-500 kHz (high frequency) carrier transmission
- Baud rates up to 115200 BPS (high frequency)
- Demodulation optional
- Supports transmission run-length encoding and deferral functions
- 32-byte FIFO for data transmission or data reception

11.8.3 Block Diagram

The CIR consists of the Transmitter and Receiver parts. The Transmitter part is responsible for transmitting data to the FIFO, processing the FIFO data by serialization, modulation and sending out the data through the LED device. The Receiver part is responsible for receiving data, processing data by demodulation, deserialization and storing data in the Receiver FIFO.

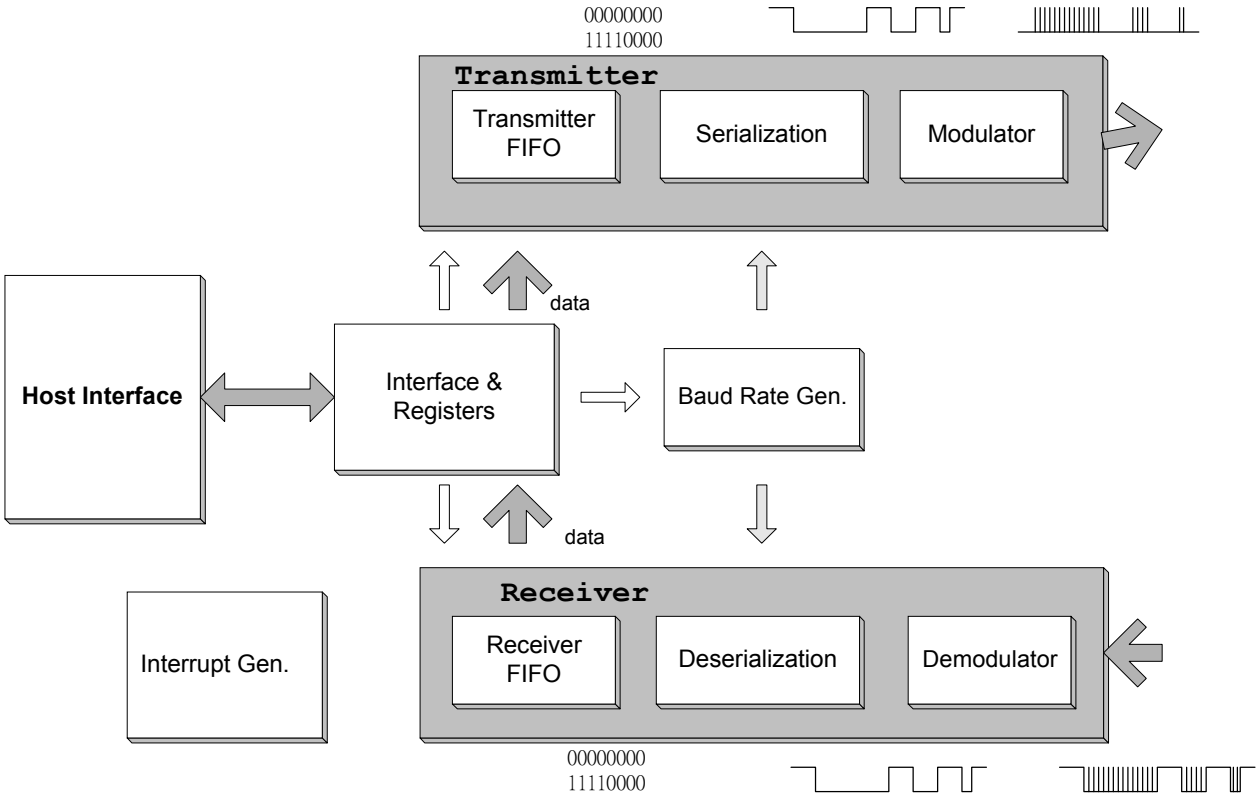


Figure 11-2. CIR Block Diagram

11.8.4 Transmit Operation

The data written to the Transmitter FIFO will be exactly serialized from LSB to MSB, modulated with carrier frequency and sent to the CIRTX output. The data are either in bit-string format or run-length decode.

Before the data transmission can begin, code byte write operations must be performed to the Transmitter FIFO DR. The bit TXRLE in the TCR1 should be set to "1" before the run-length decode data can be written into the Transmitter FIFO. Setting TXENDF in the TCR1 will enable the data transmission deferral, and avoid the transmitter FIFO underrun. The bit width of the serialized bit string is determined by the value programmed in the baud rate divisor registers BDLR and BDHR. When the bits HCFS and CFQ[4:0] are set, either the high-speed or low-speed carrier range is selected, and the corresponding carrier frequency will also be determined. Bits TXMPM[1:0] and TXMPW[2:0] specify the pulse numbers in a bit width and the required duty cycles of the carrier pulse according to the communication protocol. Only a logic "0" can activate the Transmitter LED in the format of a series of modulating pulses.

11.8.5 Receive Operation

The Receiver function is enabled if the bit RXEN in the RCR is set to "1". Either demodulated or modulated RX# signal is loaded into the Receiver FIFO, and the bit RXEND in the RCR determines the demodulation logic should be used or not. Determine the baud rate by programming the baud rate divisor registers BDLR and BDHR, and the carrier frequencies by programming the bits HCFS and CFQ[4:0]. Set RDWOS to "0" to sync. The bit RXACT in the RCR is set to "1" when the serial data or the selected carrier are incoming, and the sampled data will then be kept in the Receiver FIFO. Write "1" to the bit RXACT to stop the Receiver operation; "0" to the bit RXEN to disable the Receiver.

11.8.6 Register Descriptions and Address

Table 11-46. List of CIR Registers

Address	R/W	Default	Name
Base + 0h	R/W	FFh	CIR Data Register (DR)
Base + 1h	R/W	00h	CIR Interrupt Enable Register (IER)
Base + 2h	R/W	01h	CIR Receiver Control Register (RCR)
Base + 3h	R/W	00h	CIR Transmitter Control Register 1 (TCR1)
Base + 4h	R/W	5Ch	CIR Transmitter Control Register 2 (TCR2)
Base + 5h	R	00h	CIR Transmitter Status Register (TSR)
Base + 6h	R	00h	CIR Receiver Status Register (RSR)
Base + 5h	R/W	00h	CIR Baud Rate Divisor Low Byte Register (BDLR)
Base + 6h	R/W	00h	CIR Baud Rate Divisor High Byte Register (BDHR)
Base + 7h	R/W	01h	CIR Interrupt Identification Register (IIR)

11.8.6.1 CIR Data Register (DR)

The DR, an 8-bit **read/write** register, is the data port for CIR. Data are transmitted and received through this register.

Address: Base address + 0h

Bit	R/W	Default	Description
7 – 0	R/W	FFh	**CIR Data Register (DR[7:0])** Writing data to this register causes data to be written to the Transmitter FIFO. Reading data from this register causes data to be received from the Receiver FIFO.

11.8.6.2 CIR Interrupt Enable Register (IER)

The IER, an 8-bit **read/write** register, is used to enable the CIR interrupt request.

Address: Base address + 1h

Bit	R/W	Default	Description
7 – 6	-	-	**Reserved for ITE use.**
5	R/W	0b	**RESET (RESET)** This bit is a software reset function. Writing a "1" to this bit resets the registers of DR, IER, TCR1, BDLR, BDHR and IIR. This bit is then cleared to initial value automatically.
4	R/W	0b	**Baud Rate Register Enable Function Control (BR)** This bit is used to control the baud rate registers enable read/write function. Set this bit to "1" to enable the baud rate registers for CIR. Set this bit to "0" to disabdle the baud rate registers for CIR.
3	R/W	0b	**Interrupt Enable Function Control (IEC)** This bit is used to control the interrupt enable function. Set this bit to "1" to enable the interrupt request for CIR. Set this bit to "0" to disable the interrupt request for CIR.
2	R/W	0b	**Receiver FIFO Overrun Interrupt Enable (RFOIE)** This bit is used to control Receiver FIFO Overrun Interrupt request. Set this bit to "1" to enable Receiver FIFO Overrun Interrupt request. Set this bit to "0" to disable Receiver FIFO Overrun Interrupt request.
1	R/W	0b	**Receiver Data Available Interrupt Enable (RDAIE)** This bit is used to enable Receiver Data Available Interrupt request. The Receiver will generate this interrupt when the data available in the FIFO exceed the FIFO Threshold Level. Set this bit to "1" to enable Receiver Data Available Interrupt request. Set this bit to "0" to disable Receiver Data Available Interrupt request.
0	R/W	0b	**Transmitter Low Data Level Interrupt Enable (TLDLIE)** This bit is used to enable Transmitter Low Data Level Interrupt request. The Transmitter will generate this interrupt when the data available in the FIFO are less than the FIFO threshold Level. Set this bit to "1" to enable Transmitter Low Data Level Interrupt request. Set this bit to "0" to disable Transmitter Low Data Level Interrupt request.

11.8.6.3 CIR Receiver Control Register (RCR)

The RCR, an 8-bit **read/write** register, is used to control the CIR Receiver.

Address: Base address + 2h

Bit	R/W	Default	Description
7	R/W	0b	**Receiver Data Without Sync. (RDWOS)** This bit is used to control the sync. logic for Receiving data. Set this bit to "1" to obtain the receiving data without sync. logic. Set this bit to "0" to obtain the receiving data in sync. logic.
6	R/W	0b	**High-Speed Carrier Frequency Select (HCFS)** This bit is used to select Carrier Frequency between high-speed and low-speed. **0 30-58 kHz (Default)** 1 400-500 kHz
5	R/W	0b	**Receiver Enable (RXEN)** This bit is used to enable Receiver function. Enable Receiver and the RXACT will be active if the selected carrier frequency is received. Set this bit to "1" to enable the Receiver function. Set this bit to "0" to disable the Receiver function.
4	R/W	0b	**Receiver Demodulation Enable (RXEND)** This bit is used to control the Receiver Demodulation logic. If the Receiver device can not demodulate the correct carrier, set this bit to "1". Set this bit to "1" to enable Receiver Demodulation logic. Set this bit to "0" to disable Receiver Demodulation logic.
3	R/W	0b	**Receiver Active (RXACT)** This bit is used to control the Receiver operation. This bit is set to "0" when the Receiver is inactive. This bit will be set to "1" when the Receiver detects a pulse (RXEND=0) or pulse-train (RXEND=1) with correct carrier frequency. The Receiver then starts to sample the input data when Receiver Active is set. Write a "1" to this bit to clear the Receiver Active condition and make the Receiver enter the inactive mode.
2-0	R/W	001b	**Receiver Demodulation Carrier Range (RXDCR[2:0])** These three bits are used to set the tolerance of the Receiver Demodulation carrier frequency. See Table 11-48 and Table 11-49.

11.8.6.4 CIR Transmitter Control Register 1 (TCR1)

The TCR1, an 8-bit **read/write** register, is used to control the Transmitter.

Address: Base address + 3h

Bit	R/W	Default	Description
7	R/W	0b	**FIFO Clear (FIFOCLR)** Writing a "1" to this bit clears the FIFO. This bit is then cleared to 0 automatically.
6	R/W	0b	**Internal Loopback Enable (ILE)** This bit is used to execute internal loopback for test and must be "0" in normal operation. Set this bit to "0" to disable the Internal Loopback mode. Set this bit to "1" to enable the Internal Loopback mode.
5 - 4	R/W	0b	**FIFO Threshold Level (FIFOTL)** These two bits are used to set the FIFO Threshold Level. The FIFO length is 32 bytes for TX or RX function (ILE = 0) in normal operation and 16 bytes for both TX and RX in internal loopback mode (ILE = 1). **16-Byte Mode** / **32-Byte Mode** **00** / **1** / **1(Default)** 01 / 3 / 7 10 / 7 / 17 11 / 13 / 25
3	R/W	0b	**Transmitter Run Length Enable (TXRLE)** This bit controls the Transmitter Run Length encoding/decoding mode, which condenses a series of "1" or "0" into one byte with the bit value stored in bit 7 and number of bits minus 1 in bits 6 – 0. Set this bit to "1" to enable the Transmitter Run Length encoding/decoding mode. Set this bit to "0" to disable the Transmitter Run Length encoding/decoding mode.
2	R/W	0b	**Transmitter Deferral (TXENDF)** This bit is used to avoid Transmitter underrun condition. When this bit is set to "1", the Transmitter FIFO data will be retained until the transmitter time-out condition occurs or the FIFO reaches full.
1 – 0	R/W	0b	**Transmitter Modulation Pulse Mode (TXMPM[1:0])** These two bits are used to define the Transmitter modulation pulse mode. **TXMPM[1:0] Modulation Pulse Mode** C_pls mode (Default): Pulses are generated continuously for the entire logic 0 bit time. 8_pls mode: 8 pulses are generated for each logic 0 bit. 6_pls mode: 6 pulses are generated for each logic 0 bit. 11: Reserved

11.8.6.5 CIR Transmitter Control Register (TCR2)

The TCR2, an 8-bit **read/write** register, is used to determine the carrier frequency.

Address: Base address + 4h

Bit	R/W	Default	Description
7 – 3	R/W	01011b	**Carrier Frequency (CFQ[4:0])** These five bits are used to determine the modulation carrier frequency. See Table 11-47 on the next page.
2 – 0	R/W	100b	**Transmitter Modulation Pulse Width (TXMPW[2:0])** These three bits are used to set the Transmitter Modulation pulse width. The duty cycle of the carrier will be determined according to the settings of Carrier Frequency and the selection of Transmitter Modulation Pulse Width. **TXMPW[2:0] / HCFS = 0 / HCFS = 1** 000 / Reserved / Reserved 001 / Reserved / Reserved 010 / 6 μs / 0.7us 011 / 7 μs / 0.8us **100 / 8.7 μs / 0.9us(Default)** 101 / 10.6 μs / 1.0us 110 / 13.3 μs / 1.16us 111 / Reserved / Reserved

Table 11-47. Modulation Carrier Frequency

CFQ	Low Frequency (HCFS =0)	High Frequency (HCFS = 1)
00000	27 kHz	-
00010	29 kHz	-
00011	30 kHz	400 kHz
00100	31 kHz	-
00101	32 kHz	-
00110	33 kHz	-
00111	34 kHz	-
01000	35 kHz	450 kHz
01001	36 kHz	-
01010	37 kHz	-
01011	**38 kHz (default)**	**480 kHz (default)**
01100	39 kHz	-
01101	40 kHz	500 kHz
01110	41 kHz	-
01111	42 kHz	-
10000	43 kHz	-
10001	44 kHz	-
10010	45 kHz	-
10011	46 kHz	-
10100	47 kHz	-
10101	48 kHz	-
10110	49 kHz	-
10111	50 kHz	-
11000	51 kHz	-
11001	52 kHz	-
11010	53 kHz	-
11011	54 kHz	-
11100	55 kHz	-
11101	56 kHz	-
11110	57 kHz	-
11111	58 kHz	-

Table 11-48. Receiver Demodulation Low Frequency (HCFS = 0)

RXDCR	001		010		011		100		101		110		
CFQ	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	(Hz)
00001	26.25	29.75	24.5	31.5	22.75	33.25	21	35	19.25	36.75	17.5	38.5	28k
00010	27.19	30.81	25.38	32.63	23.56	34.44	21.75	36.25	19.94	38.06	18.13	39.88	29k
00011	28.13	31.88	26.25	33.75	24.38	35.63	22.5	37.5	20.63	39.38	18.75	41.25	30k
00100	29.06	32.94	27.13	34.88	25.19	36.81	23.25	38.75	21.31	40.69	19.38	42.63	31k
00101	30	34	28	36	26	38	24	40	22	42	20	44	32k
00110	30.94	35.06	28.88	37.13	26.81	39.19	24.75	41.25	22.69	43.31	20.63	45.38	33k
00111	31.88	36.13	29.75	38.25	27.63	40.38	25.5	42.5	23.38	44.63	21.25	46.75	34k
01000	32.81	37.19	30.63	39.38	28.44	41.56	26.25	43.75	24.06	45.94	21.88	48.13	35k
01001	33.75	38.25	31.5	40.5	29.25	42.75	27	45	24.75	47.25	22.5	49.5	36k
01010	34.69	39.31	32.38	41.63	30.06	43.94	27.75	46.25	25.44	48.56	23.13	50.88	37k
01011	**35.63**	**40.38**	**33.25**	**42.75**	**30.88**	**45.13**	**28.5**	**47.5**	**26.13**	**49.88**	**23.75**	**52.25**	**38k**
01100	36.56	41.44	34.13	43.88	31.69	46.31	29.25	48.75	26.81	51.19	24.38	53.63	39k
01101	37.5	42.5	35	45	32.5	47.5	30	50	27.5	52.5	25	55	40k
01110	38.44	43.56	35.88	46.13	33.31	48.69	30.75	51.25	28.19	53.81	25.63	56.38	41k
01111	39.38	44.63	36.75	47.25	34.13	49.88	31.5	52.5	28.88	55.13	26.25	57.75	42k
10000	40.31	45.69	37.63	48.38	34.94	51.06	32.25	53.75	29.56	56.44	26.88	59.13	43k
10001	41.25	46.75	38.5	49.5	35.75	52.25	33	55	30.25	57.75	27.5	60.5	44k
10010	42.19	47.81	39.38	50.63	36.56	53.44	33.75	56.25	30.94	59.06	28.13	61.88	45k
10011	43.13	48.88	40.25	51.75	37.38	54.63	34.5	57.5	31.63	60.38	28.75	63.25	46k
10100	44.06	49.94	41.13	52.88	38.19	55.81	35.25	58.75	32.31	61.69	29.38	64.63	47k
10101	45	51	42	54	39	57	36	60	33	63	30	66	48k
10110	45.94	52.06	42.88	55.13	39.81	58.19	36.75	61.25	33.69	64.31	30.63	67.38	49k
10111	46.88	53.13	43.75	56.25	40.63	59.38	37.5	62.5	34.38	65.63	31.25	68.75	50k
11000	47.81	54.19	44.63	57.38	41.44	60.56	38.25	63.75	35.06	66.94	31.88	70.13	51k
11001	49.18	54.55	46.88	57.69	44.78	61.22	42.86	65.22	41.1	69.77	39.47	75	52k
11010	49.69	56.31	46.38	59.63	43.06	62.94	39.75	66.25	36.44	69.56	33.13	72.88	53k
11011	50.63	57.38	47.25	60.75	43.88	64.13	40.5	67.5	37.13	70.88	33.75	74.25	54k
11100	51.56	58.44	48.13	61.88	44.69	65.31	41.25	68.75	37.81	72.19	34.38	75.63	55k
11101	52.5	59.5	49	63	45.5	66.5	42	70	38.5	73.5	35	77	56k
11110	53.44	60.56	49.88	64.13	46.31	67.69	42.75	71.25	39.19	74.81	35.63	78.38	57k

Table 11-49. Receiver Demodulation High Frequency (HCFS = 1)

RXDCR	001		010		011		100		101		110		
CFQ	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	(Hz)
00011	375	425	350	450	325	475	300	500	275	525	250	550	400k
01000	421.9	478.1	393.8	506.3	365.6	534.4	337.5	562.5	309.4	590.6	281.3	618.8	450k
01011	450	510	420	540	390	570	360	600	330	630	300	660	**480k**
01011	468.8	531.3	437.5	562.5	406.3	593.8	375	625	343.8	656.3	312.5	687.5	500k

11.8.6.6 CIR Baud Rate Divisor Low Byte Register (BDLR)

The BDLR, an 8-bit **read/write** register, is used to program the CIR Baud Rate clock.

Address: Base address + 5h (when BR = 1)

Bit	R/W	Default	Description
7-0	R/W	00h	**Baud Rate Divisor Low Byte (BDLR[7:0])** These bits are the low byte of the register used to divide the Baud Rate clock.

11.8.6.7 CIR Baud Rate Divisor High Byte Register (BDHR)

The BDHR, an 8-bit **read/write** register, is used to program the CIR Baud Rate clock.

Address: Base address + 6h (when BR = 1)

Bit	R/W	Default	Description
7-0	R/W	00h	**Baud Rate Divisor High Byte (BDHR[7:0])** These bits are the high byte of the register used to divide the Baud Rate clock.

Baud rate divisor = 115200 / baud rate
Ex1: 2400bps → 115200 /2400 = 48 → 48(d) = 0030 (h)
BDHR = 00(h), BDLR = 30(h)
Ex2: bit width = 0.565 ms → 1770 bps → 115200 / 1770 = 65(d) = 0041(h)
BDHR = 00(h), BDLR = 0041(h)

11.8.6.8 CIR Transmitter Status Register (TSR)

The TSR, an 8-bit **read only** register, provides the Transmitter FIFO status.

Address: Base address + 5h

Bit	R/W	Default	Description
7-6	R	-	**Reserved**
5-0	R	000000b	**Transmitter FIFO Byte Count (TXFBC[5:0])** Return the number of bytes left in the Transmitter FIFO.

11.8.6.9 CIR Receiver FIFO Status Register (RSR)

The RSR, an 8-bit **read only** register, provides the Receiver FIFO status.

Address: Base address + 6h

Bit	R/W	Default	Description
7	R	0b	**Receiver FIFO Time-out (RXFTO)** This bit will be set to "1" when a Receiver FIFO time-out condition occurs. The conditions that must exist for a Receiver FIFO time-out condition to occur include the followings: a. At least one byte has been in the Receiver FIFO is not empty for 64 ms or more, and b. The receiver has been inactive (RXACT=0) for over 64 ms or more, and c. More than 64 ms have elapsed since the last byte was read from the Receiver FIFO by the CPU
6	-	-	**Reserved**
5 – 0	R	000000b	**Receiver FIFO Byte Count (RXFBC)** Return the number of bytes left in the Receiver FIFO.

11.8.6.10 CIR Interrupt Identification Register (IIR)

The IIR, an 8-bit **read only** register, is used to identify the pending interrupts.

Address: Base address + 7h

Bit	R/W	Default	Description
7 - 3	-	-	**Reserved**
2 – 1	R	00b	**Interrupt Identification** These two bits are used to identify the source of the pending interrupts. **IID[1:0] Interrupt Source** 00 No interrupt 01 Transmitter Low Data Level Interrupt 10 Receiver Data Stored Interrupt 11 Receiver FIFO Overrun Interrupt
0	R	1b	**Interrupt Pending** This bit will be set to "1" while an interrupt is pending.

12. DC Electrical Characteristics

Absolute Maximum Ratings*

Applied Voltage..... -0.5V to 7.0V

Input Voltage (Vi)..... -0.5V to VCC+0.5V

Output Voltage (Vo)..... -0.5V to VCC + 0.3V

Operation Temperature (Topt)..... 0°C to +70°C

Storage Temperature ..... -55°C to +125°C

Power Dissipation 300mW

***Comments**

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to this device. These are stress ratings only. Functional operation of this device at these or any other conditions above those indicated in the operational sections of this specification is not implied or intended. Exposure to the absolute maximum rating conditions for extended periods may affect device reliability.

DC Electrical Characteristics (VCC = 5V ± 5%, Ta = 0°C to + 70°C)

Symbol	Parameter	Min.	Typ.	Max.	Unit	Conditions
DO8 Buffer						
V_{OL}	Low Output Voltage			0.4	V	I_{OL} = 8 mA
V_{OH}	High Output Voltage	2.4			V	I_{OH} = -8 mA
DOD8 Buffer						
V_{OL}	Low Output Voltage			0.4	V	I_{OL} = 8 mA
DOD24 Buffer						
V_{OL}	Low Output Voltage			0.4	V	I_{OL} = 24 mA
DO16 Buffer						
V_{OL}	Low Output Voltage			0.4	V	I_{OL} = 16 mA
V_{OH}	High Output Voltage	2.4			V	I_{OH} = -16 mA
DO40 Buffer						
V_{OL}	Low Output Voltage			0.5	V	I_{OL} = 48 mA
V_{OH}	High Output Voltage	2.4			V	I_{OH} = -6 mA
DIOD8 Type Buffer						
V_{OL}	Low Output Voltage			0.4	V	I_{OL} = 8 mA
V_{IL}	Low Input Voltage			0.8	V	
V_{IH}	High Input Voltage	2.2			V	
I_{IL}	Low Input Leakage		10		μA	V_{IN} = 0
I_{IH}	High Input Leakage			-10	μA	V_{IN} = VCC
I_{OZ}	3-state Leakage			20	μA	
DIOD16 Type Buffer						
V_{OL}	Low Output Voltage			0.4	V	I_{OL} = 16 mA
V_{IL}	Low Input Voltage			0.8	V	
V_{IH}	High Input Voltage	2.2			V	
I_{IL}	Low Input Leakage		10		μA	V_{IN} = 0
I_{IH}	High Input Leakage			-10	μA	V_{IN} = VCC
I_{OZ}	3-state Leakage			20	μA	

DC Electrical Characteristics (VCC = 5V ± 5%, Ta = 0°C to + 70°C) [cont'd]

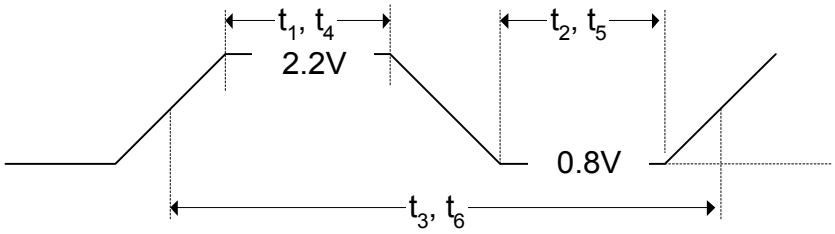
Symbol	Parameter	Min.	Typ.	Max.	Unit	Conditions
DIO24 Type Buffer						
V_{OL}	Low Output Voltage			0.4	V	I_{OL} = 24 mA
V_{OH}	High Output Voltage	2.4			V	I_{OH} = -24 mA
V_{IL}	Low Input Voltage			0.8	V	
V_{IH}	High Input Voltage	2.2			V	
I_{IL}	Low Input Leakage		10		μA	V_{IN} = 0
I_{IH}	High Input Leakage			-10	μA	V_{IN} = VCC
I_{OZ}	3-state Leakage			20	μA	
DI Type Buffer						
V_{IL}	Low Input Voltage			0.8	V	
V_{IH}	High Input Voltage	2.2			V	
I_{IL}	Low Input Leakage		10		μA	V_{IN} = 0
I_{IH}	High Input Leakage			-10	μA	V_{IN} = VCC

13. AC Characteristics (VCC = 5V ± 5%, Ta = 0°C to + 70°C)

13.1 Clock Input Timings

Symbol	Parameter	Min.	Typ.	Max.	Unit
t_1	Clock High Pulse Width when CLKIN=48 MHz[1]	8			nsec
t_2	Clock Low Pulse Width when CLKIN=48 MHz [1]	8			nsec
t_3	Clock Period when CLKIN=48 MHz [1]	20	21	22	nsec
t_4	Clock High Pulse Width when CLKIN=24 MHz [1]	18			nsec
t_5	Clock Low Pulse Width when CLKIN=24 MHz [1]	18			nsec
t_6	Clock Period when CLKIN=24 MHz [1]	40	42	44	nsec

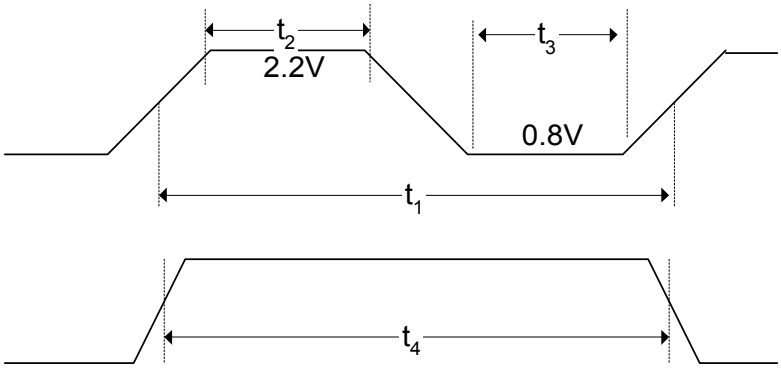
1. Not tested in mass-production. Guaranteed by design.



13.2 PCICLK and RESET Timings

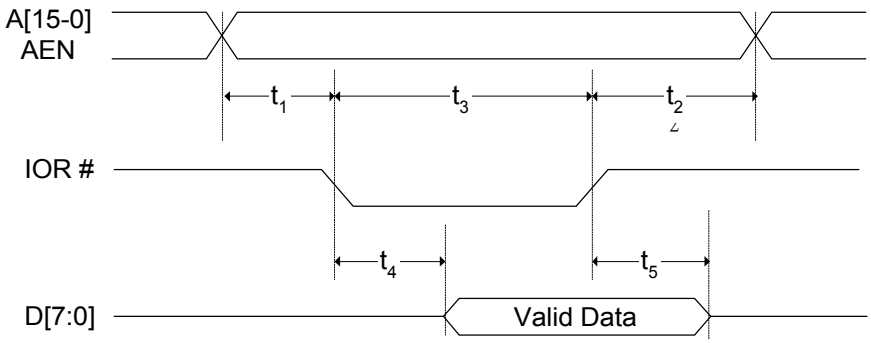
Symbol	Parameter	Min.	Typ.	Max.	Unit
t_1	PCICLK Cycle Time[1]	28			nsec
t_2	PCICLK High Time[1]	11			nsec
t_3	PCICLK Low Time[1]	11			nsec
t_4	RESET High Pulse Width	1.5			μsec

1. Not tested in mass-production. Guaranteed by design.



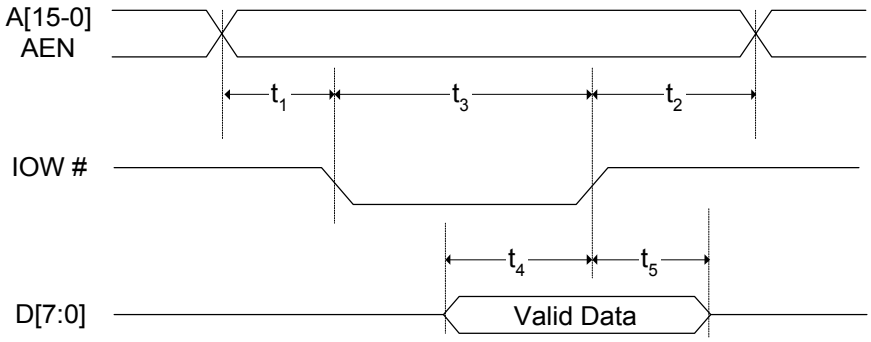
13.3 CPU Read Cycle Timings

Symbol	Parameter	Min.	Typ.	Max.	Unit
t_1	Address setup to IOR# ↓	10			nsec
t_2	Address hold from IOR# ↑	10			nsec
t_3	IOR# pulse width	100			nsec
t_4	Data valid to IOR# ↓	25		65	nsec
t_5	Output floating delay from IOR# ↑	25		50	nsec



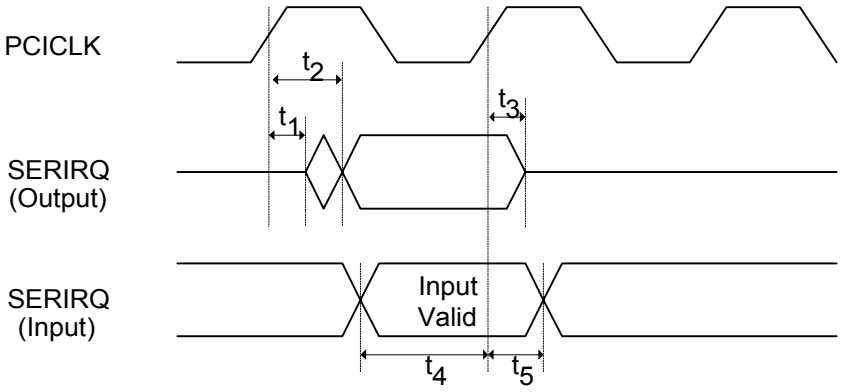
13.4 CPU Write Cycle Timings

Symbol	Parameter	Min.	Typ.	Max.	Unit
t_1	Address setup to IOW# ↓	10			nsec
t_2	Address hold from IOW# ↑	10			nsec
t_3	IOW# pulse width	100			nsec
t_4	Data setup to IOW# ↑	25			nsec
t_5	Data hold from IOR# ↑	15			nsec



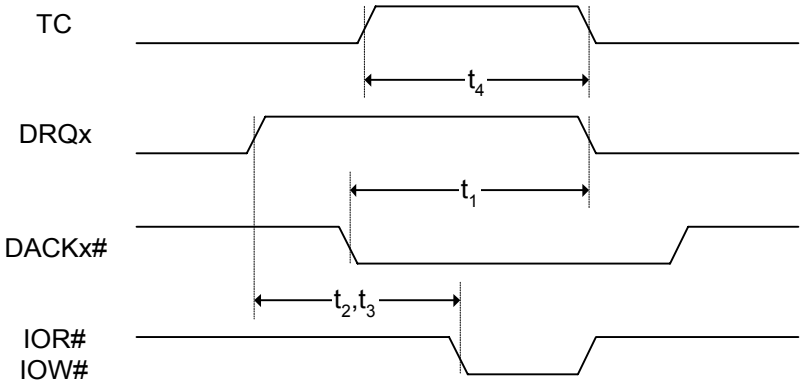
13.5 SERIRQ Timings

Symbol	Parameter	Min.	Typ.	Max.	Unit
t_1	Float to Active Delay	3			nsec
t_2	Output Valid Delay			12	nsec
t_3	Active to Float Delay			6	nsec
t_4	Input Setup Time	9			nsec
t_5	Input Hold Time	3			nsec



13.6 DMA Timings

Symbol	Parameter	Min.	Typ.	Max.	Unit
t_1	Float to Active Delay	3			nsec
t_2	Output Valid Delay			12	nsec
t_3	Active to Float Delay			6	nsec
t_4	Input Setup Time	9			nsec
t_5	Input Hold Time	3			nsec

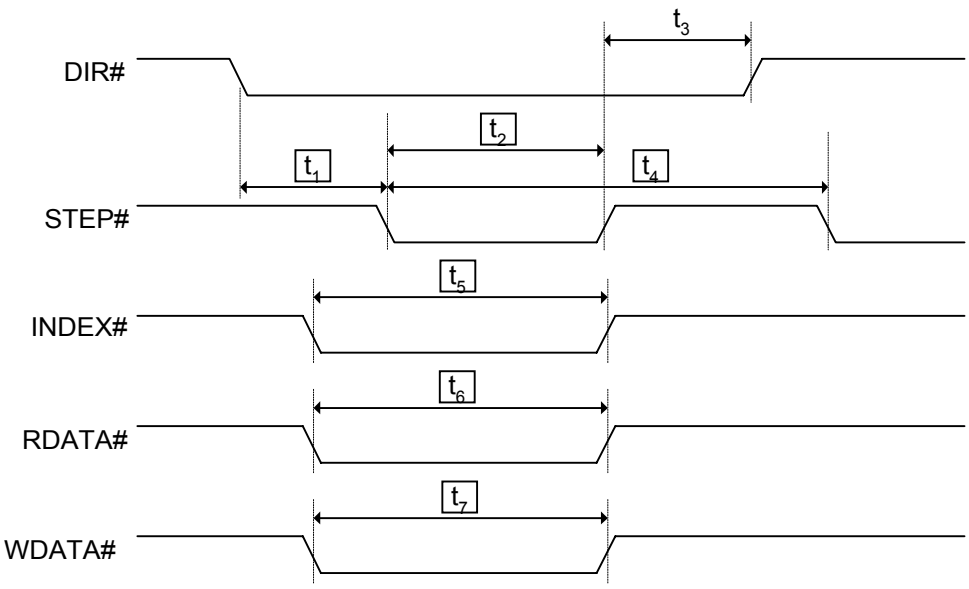


13.7 Floppy Disk Drive Timings

Symbol	Parameter	Min.	Typ.	Max.	Unit
t_1	DIR# active to STEP# low		4X t_{mclk} Note1		nsec
t_2	STEP# active time (low)		24X t_{mclk}		nsec
t_3	DIR# hold time after STEP#		t_{SRT} Note2		msec
t_4	STEP# cycle time		t_{SRT}		msec
t_5	INDEX# low pulse width	2X t_{mclk}			nsec
t_6	RDATA# low pulse width	40			nsec
t_7	WDATA# low pulse width		1X t_{mclk}		nsec

Note 1: t_{mclk} is the cycle of main clock for the microcontroller of FDC. 1/ t_{mclk} =8M/ 4M/ 2.4M/ 2M hz for 1M/ 500K/ 300K/ 250 Kbps transfer rates respectively.

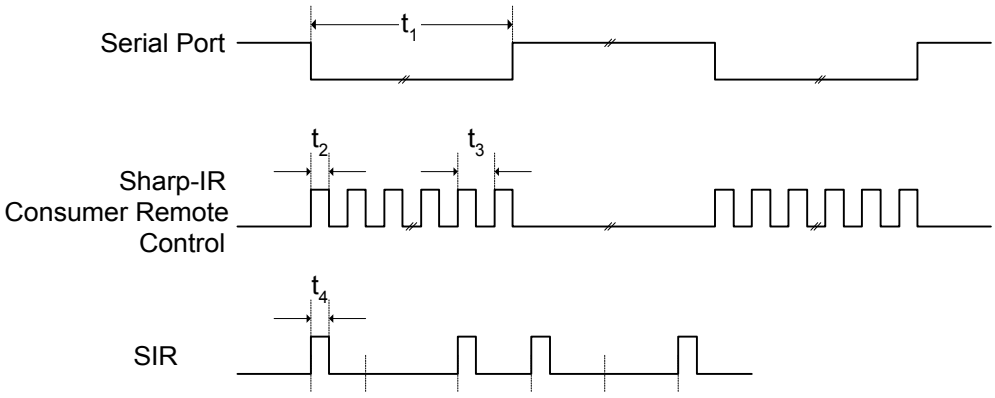
Note 2: t_{SRT} is the cycle of the Step Rate Time. Please refer to the functional description of the SPECIFY command of the FDC.



13.8 Serial Port, ASKIR, SIR and Consumer Remote Control Timings

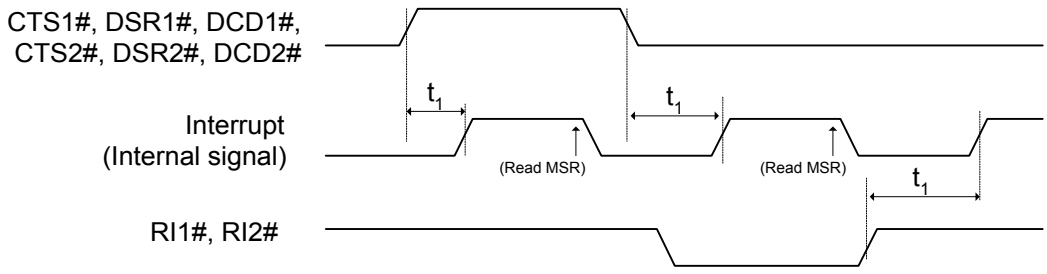
Symbol	Parameter	Conditions	Min.	Max.	Unit
t_1	Single Bit Time in Serial Port and ASKIR	Transmitter	t_{BTN} – 25 Note1	t_{BTN} + 25	nsec
		Receiver	t_{BTN} – 2%	t_{BTN} + 2%	nsec
t_2	Modulation Signal Pulse Width in ASKIR	Transmitter	950	1050	nsec
		Receiver	500		nsec
t_3	Modulation Signal Period in ASKIR	Transmitter	1975	2025	nsec
		Receiver	2000X(23/24)	2000X(25/24)	nsec
t_4	SIR Signal Pulse Width	Transmitter, Variable	(3/16) x t_{BTN} – 25	(3/16) x t_{BTN} + 25	nsec
		Transmitter, Fixed	1.48	1.78	μsec
		Receiver	1		μsec

Note 1: t_{BTN} is the nominal bit time in Serial Port, ASKIR, and SIR. It is determined by the setting on the Baud Rate Divisor registers.



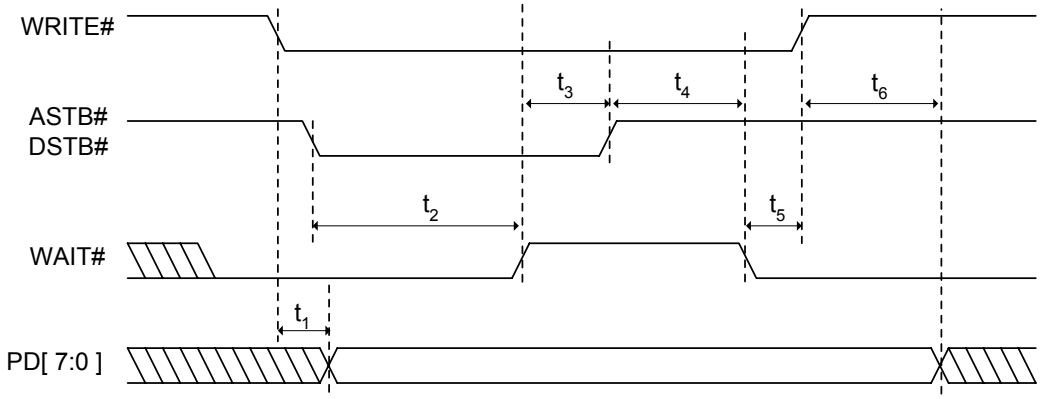
13.9 Modem Control Timings

Symbol	Parameter	Min.	Typ.	Max.	Unit
t_1	Float to active delay			40	nsec



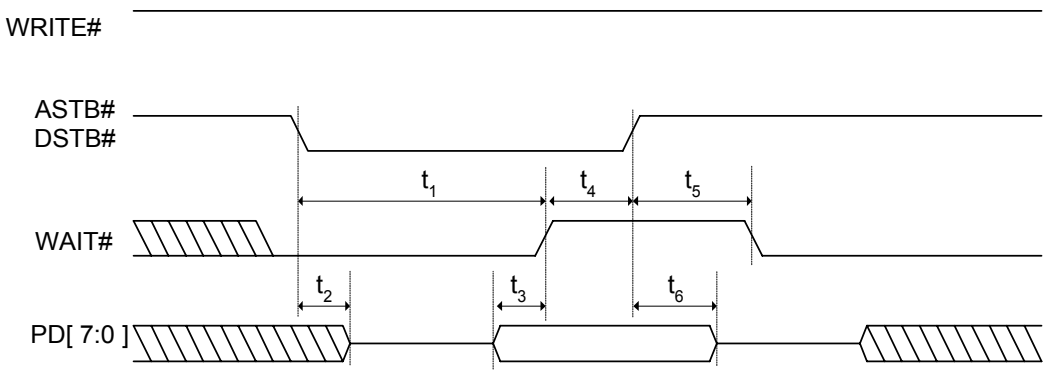
13.10 EPP Address or Data Write Cycle Timings

Symbol	Parameter	Min.	Typ.	Max.	Unit
t_1	WRITE# asserted to PD[7:0] valid			50	nsec
t_2	ASTB# or DSTB# asserted to WAIT# de-asserted	0		10	nsec
t_3	WAIT# de-asserted to ASTB# or DSTB# de-asserted	65		135	nsec
t_4	ASTB# or DSTB# de-asserted to WAIT# asserted	0			nsec
t_5	WAIT# asserted to WRITE# de-asserted	65			nsec
t_6	PD[7:0] invalid after WRITE# de-asserted	0			nsec



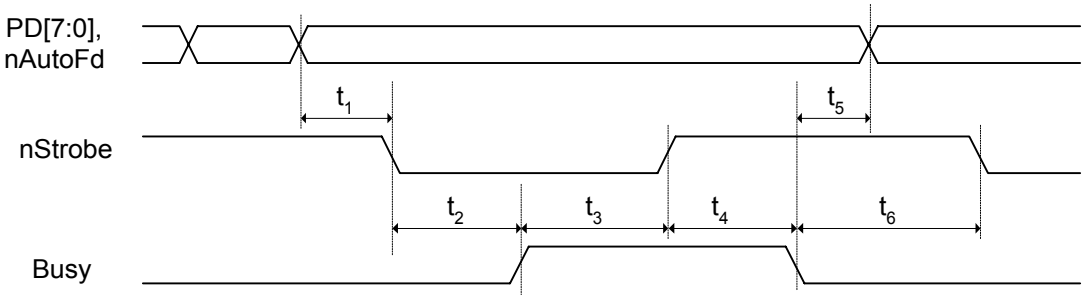
13.11 EPP Address or Data Read Cycle Timings

Symbol	Parameter	Min.	Typ.	Max.	Unit
t_1	ASTB# or DSTB# asserted to WAIT# de-asserted			10	nsec
t_2	ASTB# or DSTB# asserted to PD[7:0] Hi-Z	0			nsec
t_3	PD[7:0] valid to WAIT# de-asserted	0			nsec
t_4	WAIT# de-asserted to ASTB# or DSTB# de-asserted	65		135	nsec
t_5	ASTB# or DSTB# de-asserted to WAIT# asserted	0			nsec
t_6	PD[7:0] invalid after ASTB# or DSTB# de-asserted	20			nsec



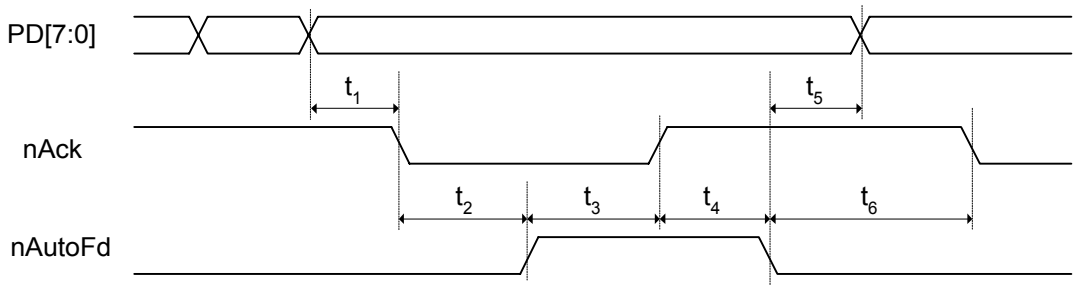
13.12 ECP Parallel Port Forward Timings

Symbol	Parameter	Min.	Typ.	Max.	Unit
t_1	PD[7:0] and nAutoFd valid to nStrobe asserted			50	nsec
t_2	nStrobe asserted to Busy asserted	0			nsec
t_3	Busy asserted to nStrobe de-asserted	70		170	nsec
t_4	nStrobe de-asserted to Busy de-asserted	0			nsec
t_5	Busy de-asserted to PD[7:0] and nAutoFd changed	80		180	nsec
t_6	Busy de-asserted to nStrobe asserted	70		170	nsec



13.13 ECP Parallel Port Backward Timings

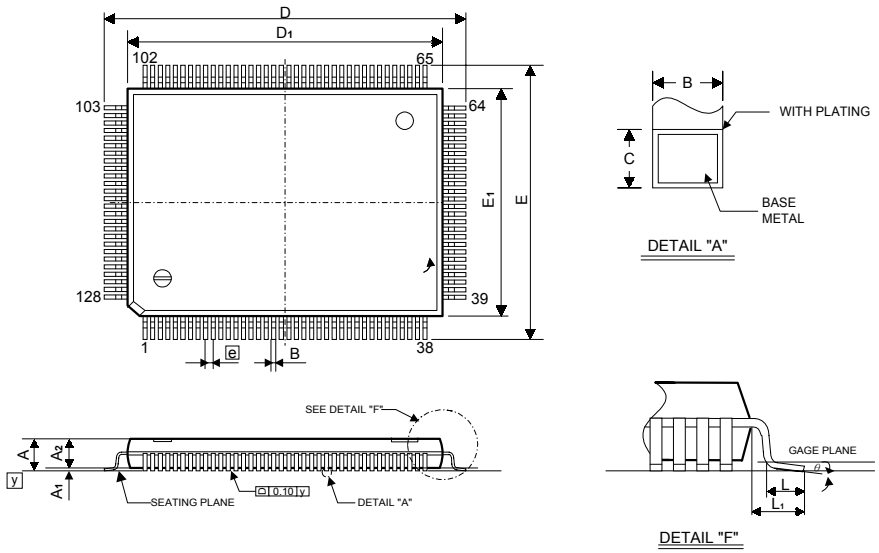
Symbol	Parameter	Min.	Typ.	Max.	Unit
t_1	PD[7:0] valid to nAck asserted	0			nsec
t_2	nAck asserted to nAutoFd asserted	70		170	nsec
t_3	nAutoFd asserted to nAck de-asserted	0			nsec
t_4	nAck de-asserted to nAutoFd de-asserted	70		170	nsec
t_5	nAutoFd de-asserted to PD[7:0] changed	0			nsec
t_6	nAutoFd de-asserted to nAck asserted	0			nsec



14. Package Information

QFP 128L Outline Dimensions

unit: inches/mm



Symbol	Dimension in inch			Dimension in mm		
	Min.	Nom.	Max.	Min.	Nom.	Max.
A	-	-	0.134	-	-	3.40
A_1	0.010	-	-	0.25	-	-
A_2	0.107	0.112	0.117	2.73	2.85	2.97
B	0.007	0.009	0.011	0.17	0.22	0.27
C	0.004	-	0.008	0.09	-	0.20
D	0.906	0.913	0.921	23.00	23.20	23.40
D_1	0.783	0.787	0.791	19.90	20.00	20.10
E	0.669	0.677	0.685	17.00	17.20	17.40
E_1	0.547	0.551	0.555	13.90	14.00	14.10
e	0.020 BSC			0.5 BSC		
L	0.029	0.035	0.041	0.73	0.88	1.03
L_1	0.063 BSC			1.60 BSC		
y	-	-	0.004	-	-	0.10
θ	0°	-	7°	0°	-	7°

Notes:

1. DIMENSIONS D_1 AND E_1 DO NOT INCLUDE MOLD PROTRUSION. BUT MOLD MISMATCH IS INCLUDED.
2. DIMENSIONS B DOES NOT INCLUDE DAMBAR PROTRUSION.
3. CONTROLLING DIMENSION: MILLIMETER

15. Ordering Information

Part No.	Package
IT8673F	128L QFP