FAIRCHILD SEMICONDUCTOR®

March 2013

FCD900N60Z

N-Channel SuperFET® II MOSFET

600 V, 4.5 A, 900 mΩ

Features

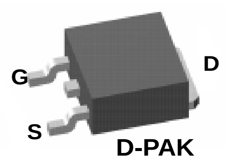
- 650 V @ T_J = 150°C
- Max. $R_{DS(on)}$ = 900 mΩ
- Ultra Low Gate Charge (Typ. Q_g = 13 nC)
- Low Effective Output Capacitance (Typ. C_{oss}.eff = 49 pF)
- 100% Avalanche Tested
- ESD Improved Capacity

Applications

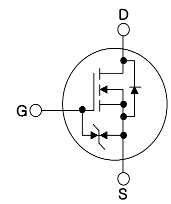
- LCD / LED / PDP TV and Monitor Lighting
- Solar Inverter
- Charger

Description

SuperFET®II MOSFET is Fairchild Semiconductor®'s first generation of high voltage super-junction (SJ) MOSFET family that is utilizing charge balance technology for outstanding low on-resistance and lower gate charge performance.This advanced technology is tailored to minimize conduction loss, provide superior switching performance, and withstand extreme dv/dt rate and higher avalanche energy. Consequently, SuperFETII MOSFET is suitable for various AC/DC power conversion for system miniaturization and higher efficiency.



D-PAK



Absolute Maximum Ratings T_C = 25°C unless otherwise noted

Symbol	Parameter		FCD900N60Z	Unit
V_{DSS}	Drain to Source Voltage		600	V
V_{GSS}	Gate to Source Voltage	-DC	±20	V
		-AC (f > 1Hz)	±30	V
I_D	Drain Current	-Continuous (T_C = 25°C)	4.5	A
		-Continuous (T_C = 100°C)	3.5	
I_{DM}	Drain Current	- Pulsed (Note 1)	13.5	A
E_{AS}	Single Pulsed Avalanche Energy (Note 2)		47.5	mJ
I_{AR}	Avalanche Current (Note 1)		1	A
E_{AR}	Repetitive Avalanche Energy (Note 1)		0.52	mJ
dv/dt	Peak Diode Recovery dv/dt (Note 3)		20	V/ns
	MOSFET dv/dt		100	V/ns
P_D	Power Dissipation	(T_C = 25°C)	52	W
		- Derate above 25°C	0.42	W/°C
T_J, T_{STG}	Operating and Storage Temperature Range		-55 to +150	°C
T_L	Maximum Lead Temperature for Soldering Purpose, 1/8" from Case for 5 Seconds		300	°C

Thermal Characteristics

Symbol	Parameter	FCD900N60Z	Unit
$R_{\theta JC}$	Thermal Resistance, Junction to Case	2.4	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient	100	°C/W

Package Marking and Ordering Information

Device Marking	Device	Package	Reel Size	Tape Width	Quantity
FCD900N60Z	FCD900N60Z	D-PAK	380 mm	16 mm	2500

Electrical Characteristics $T_C = 25^oC$ unless otherwise noted

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit

Off Characteristics

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
BV_{DSS}	Drain to Source Breakdown Voltage	V_{GS} = 0 V, I_D = 10 mA, T_J = 25°C	600	-	-	V
		V_{GS} = 0 V, I_D = 10 mA, T_J = 150°C	650	-	-	V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	I_D = 10 mA, Referenced to 25°C	-	0.72	-	V/°C
BV_{DS}	Drain-Source Avalanche Breakdown Voltage	V_{GS} = 0 V, I_D = 4.5 A	-	700	-	V
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = 480 V, V_{GS} = 0 V	-	-	5	μA
		V_{DS} = 480 V, T_C = 125°C	-	-	20	
I_{GSSF}	Gate-Body Leakage Current, Forward	V_{GS} = 20 V, V_{DS} = 0 V	-	-	10	uA
I_{GSSR}	Gate-Body Leakage Current, Reverse	V_{GS} = -20 V, V_{DS} = 0 V	-	-	-10	uA

On Characteristics

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$V_{GS(th)}$	Gate Threshold Voltage	$V_{GS} = V_{DS}$, I_D = 250 μA	2.5	-	3.5	V
$R_{DS(on)}$	Static Drain to Source On Resistance	V_{GS} = 10 V, I_D = 2.3 A	-	0.82	0.90	Ω
g_{FS}	Forward Transconductance	V_{DS} = 20 V, I_D = 2.3 A (Note 4)	-	4.6	-	S

Dynamic Characteristics

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
C_{iss}	Input Capacitance	V_{DS} = 25 V, V_{GS} = 0 V f = 1 MHz	-	543	720	pF
C_{oss}	Output Capacitance		-	400	530	pF
C_{rss}	Reverse Transfer Capacitance		-	20	30	pF
C_{oss}	Output Capacitance	V_{DS} = 380 V, V_{GS} = 0 V, f = 1.0 MHz	-	11	-	pF
C_{oss} eff.	Effective Output Capacitance	V_{DS} = 0 V to 480 V, V_{GS} = 0 V	-	49	-	pF
$Q_{g(tot)}$	Total Gate Charge at 10V	V_{DS} = 380 V, I_D = 2.3 A V_{GS} = 10 V (Note 4)	-	13	17	nC
Q_{gs}	Gate to Source Gate Charge		-	2.3	-	nC
Q_{gd}	Gate to Drain “Miller” Charge		-	4.8	-	nC
ESR	Equivalent Series Resistance	Drain open	-	2.4	-	Ω

Switching Characteristics

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-On Delay Time	V_{DD} = 380 V, I_D = 2.3 A V_{GS} = 10 V, R_G = 4.7 Ω (Note 4)	-	10.9	32	ns
t_r	Turn-On Rise Time		-	5.3	21	ns
$t_{d(off)}$	Turn-Off Delay Time		-	33.6	77	ns
t_f	Turn-Off Fall Time		-	11.9	34	ns

Drain-Source Diode Characteristics

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
I_S	Maximum Continuous Drain to Source Diode Forward Current		-	-	4.5	A
I_{SM}	Maximum Pulsed Drain to Source Diode Forward Current		-	-	13.5	A
V_{SD}	Drain to Source Diode Forward Voltage	V_{GS} = 0 V, I_{SD} = 2.3 A	-	-	1.2	V
t_{rr}	Reverse Recovery Time	V_{GS} = 0 V, I_{SD} = 2.3 A dI_F/dt = 100 A/μs	-	156	-	ns
Q_{rr}	Reverse Recovery Charge		-	1.3	-	μC

Notes:

1. Repetitive Rating: Pulse width limited by maximum junction temperature
2. I_{AS} = 1 A, V_{DD} = 50 V, R_G = 25 Ω, Starting T_J = 25°C
3. I_{SD} ≤ 2.3 A, di/dt ≤ 200 A/μs, $V_{DD} \leq BV_{DSS}$, Starting T_J = 25°C
4. Essentially Independent of Operating Temperature Typical Characteristics

Typical Performance Characteristics

Figure 1. On-Region Characteristics

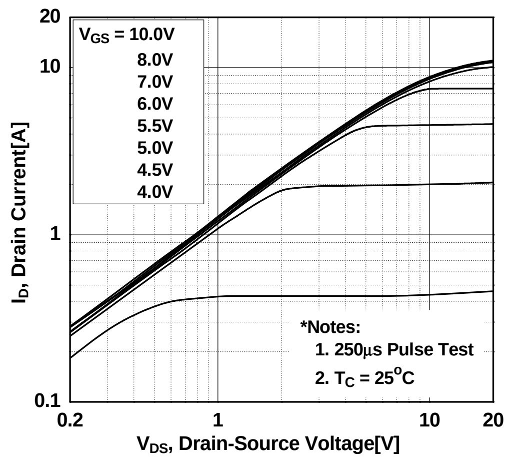


Figure 2. Transfer Characteristics

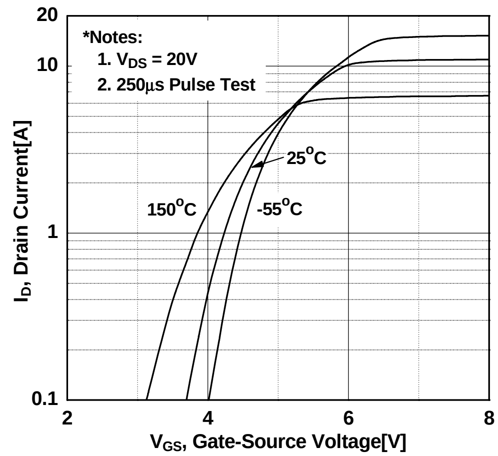


Figure 3. On-Resistance Variation vs. Drain Current and Gate Voltage

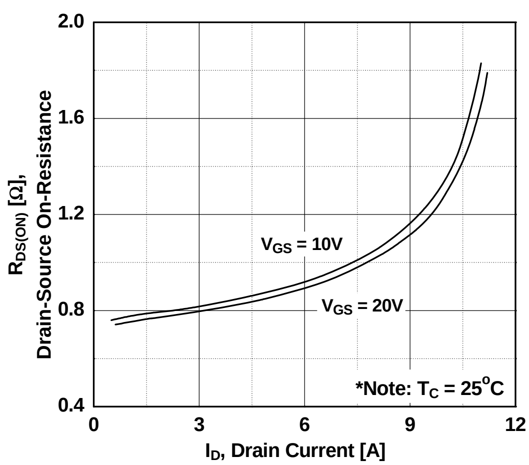


Figure 4. Body Diode Forward Voltage Variation vs. Source Current and Temperature

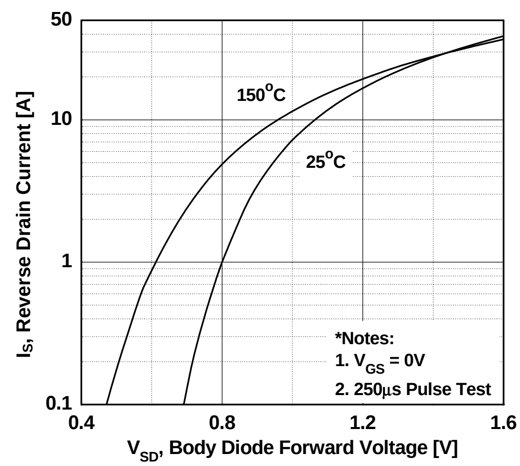


Figure 5. Capacitance Characteristics

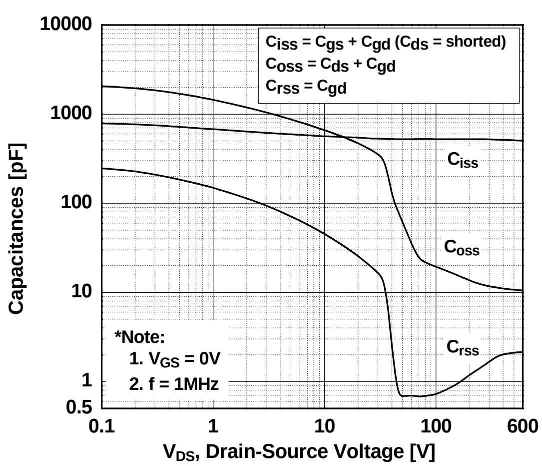
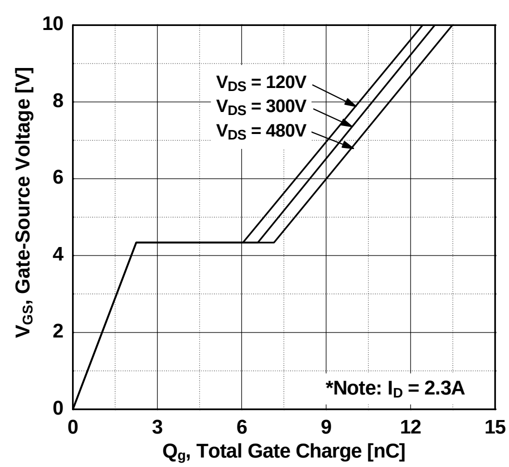


Figure 6. Gate Charge Characteristics



Typical Performance Characteristics (Continued)

Figure 7. Breakdown Voltage Variation vs. Temperature

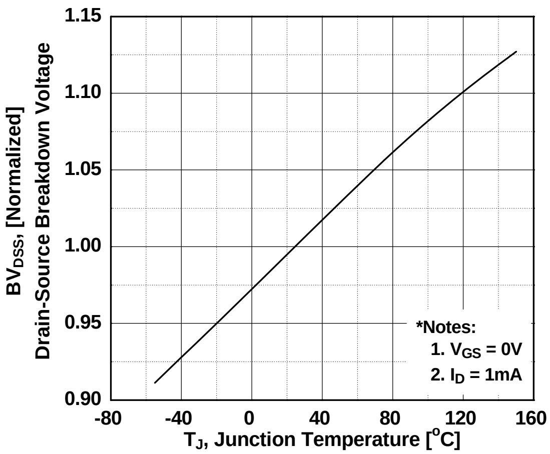


Figure 8. On-Resistance Variation vs. Temperature

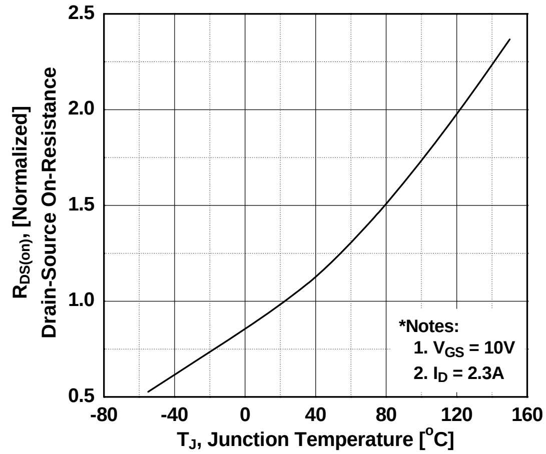


Figure 9. Maximum Safe Operating Area vs. Case Temperature

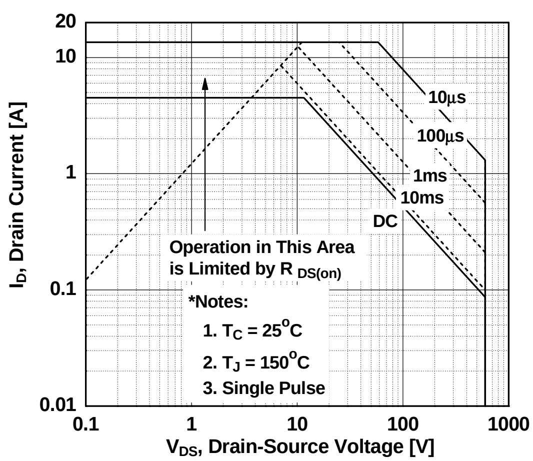


Figure 10. Maximum Drain Current

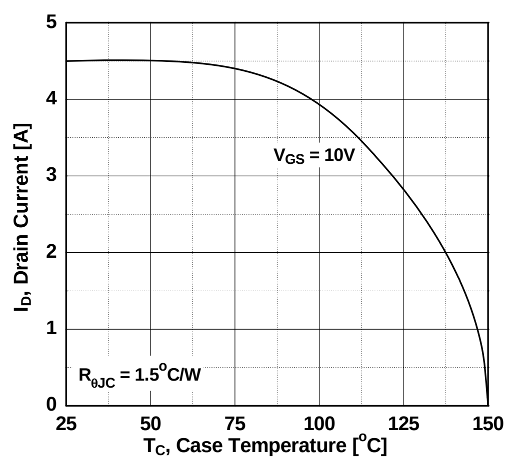
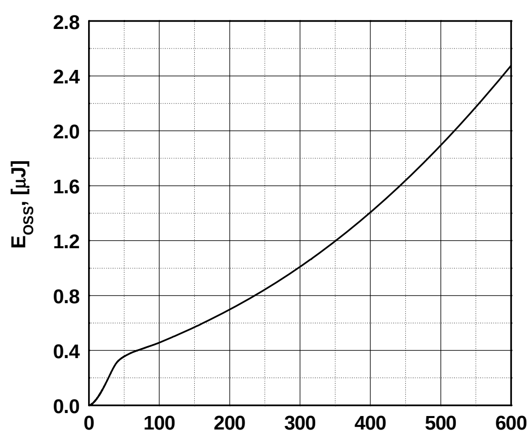
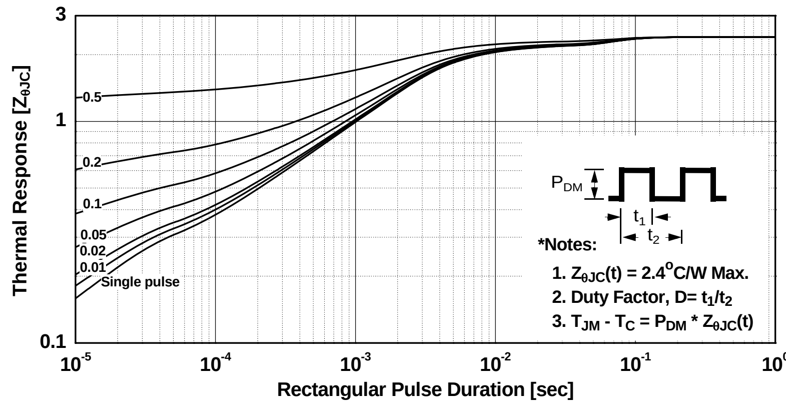


Figure 11. Eoss vs. Drain to Source Voltage

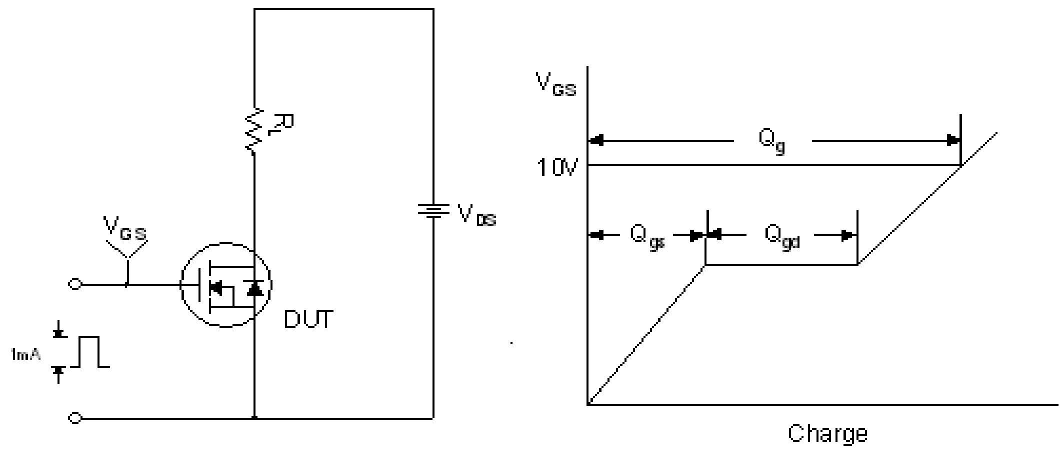


Typical Performance Characteristics (Continued)

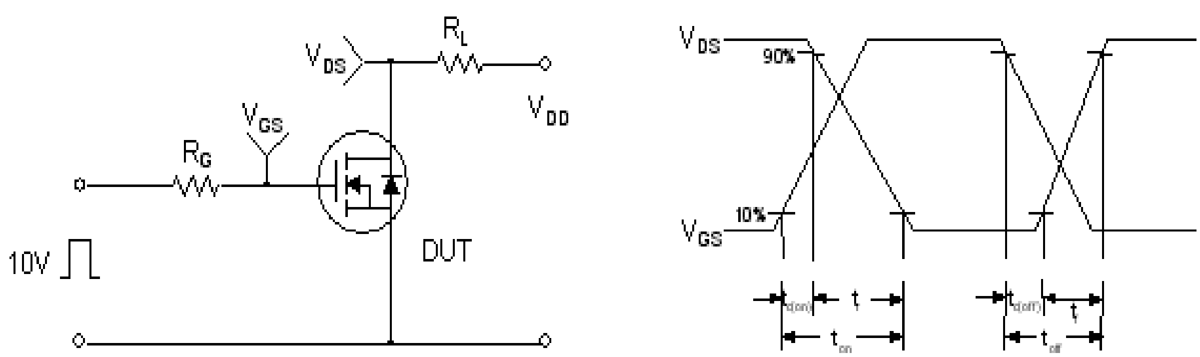
Figure 12. Transient Thermal Response Curve



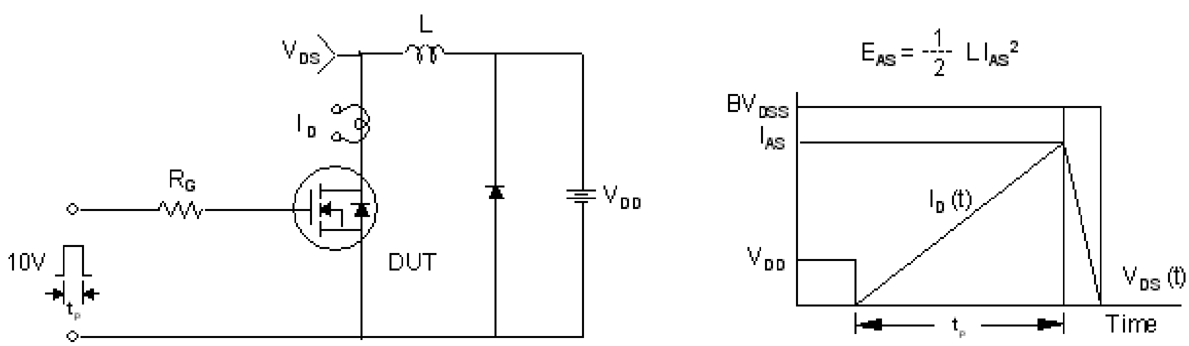
Gate Charge Test Circuit & Waveform



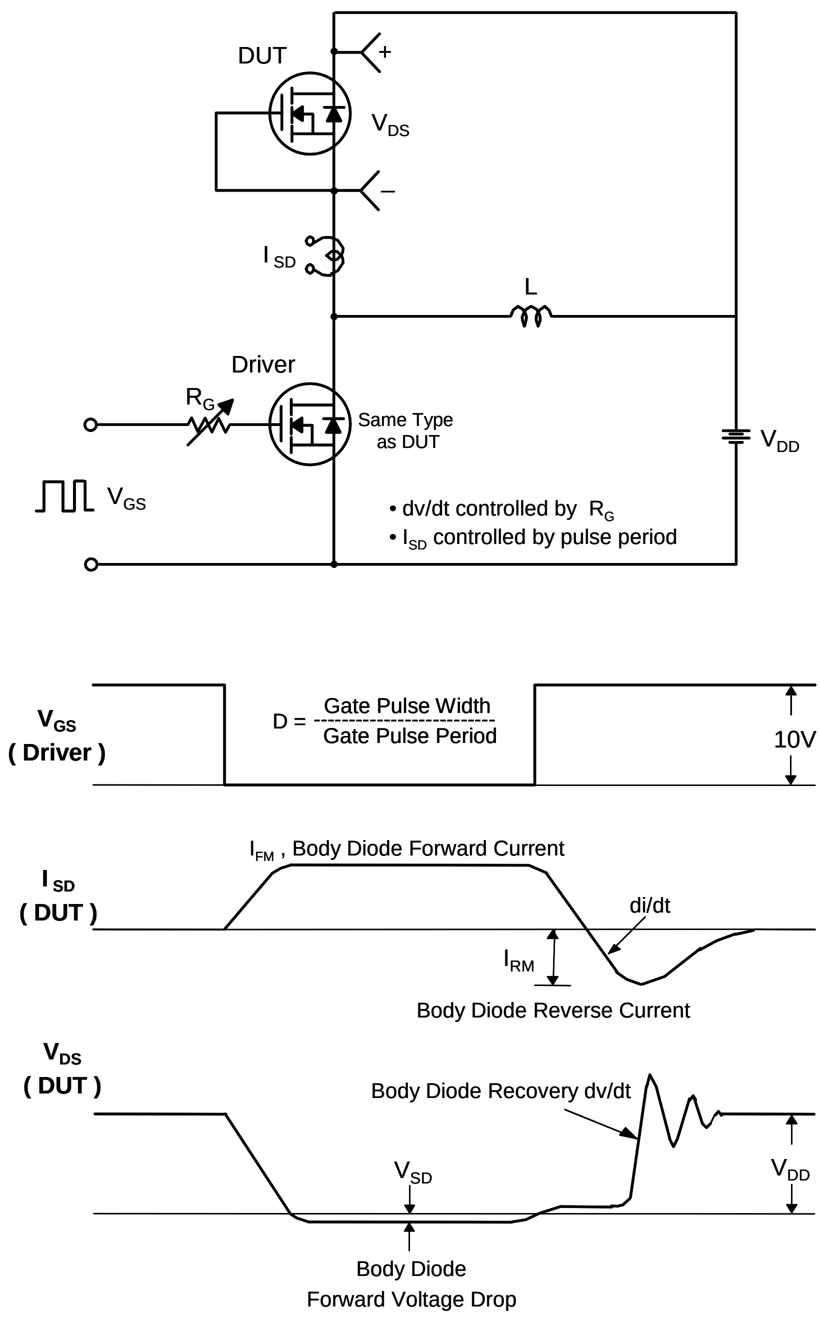
Resistive Switching Test Circuit & Waveforms



Unclamped Inductive Switching Test Circuit & Waveforms

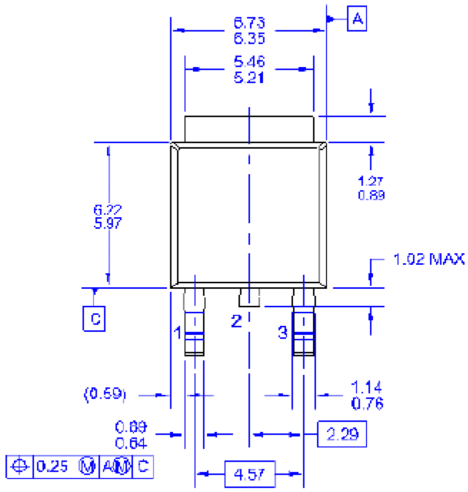


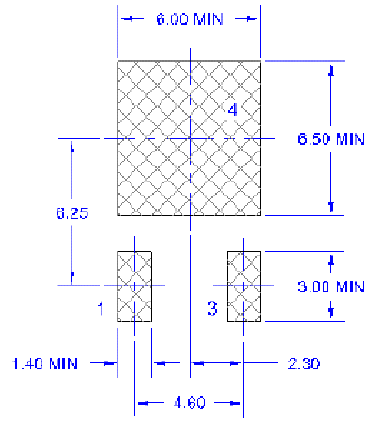
Peak Diode Recovery dv/dt Test Circuit & Waveforms



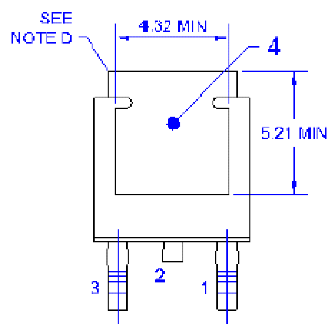
Mechanical Dimensions

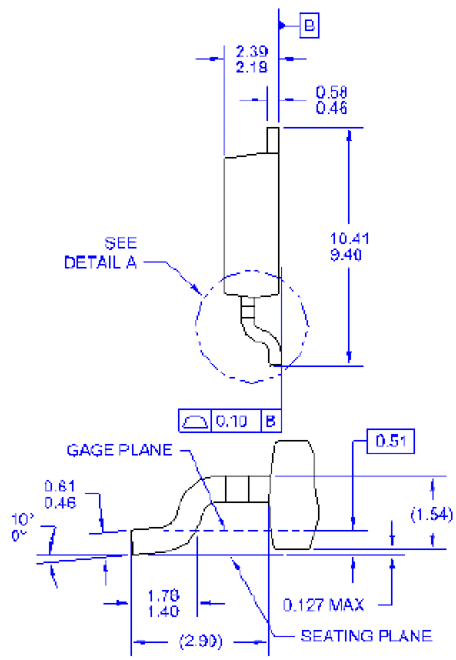
D-PAK





LAND PATTERN RECOMMENDATION





NOTES: UNLESS OTHERWISE SPECIFIED
- A) THIS PACKAGE CONFORMS TO JEDEC, TO-252, ISSUE C, VARIATION AA.
- B) ALL DIMENSIONS ARE IN MILLIMETERS.
- C) DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994.
- D) HEAT SINK TOP EDGE COULD BE IN CHAMFERED CORNERS OR EDGE PROTRUSION.
- E) PRESENCE OF TRIMMED CENTER LEAD IS OPTIONAL.
- F) DIMENSIONS ARE EXCLUSIVE OF BURSS, MOLD FLASH AND TIE BAR EXTRUSIONS.
- G) LAND PATTERN RECOMENDATION IS BASED ON IPC7351A STD TO220P1003X238-3N.
- H) DRAWING NUMBER AND REVISION: MKT-TO252A03REVB

Dimensions in Millimeters

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