

NCE N-Channel Enhancement Mode Power MOSFET

Description

The NCE7580T uses advanced trench technology and design to provide excellent $R_{DS(ON)}$ with low gate charge. This device is suitable for use in PWM, load switching and general purpose applications.

General Features

- $V_{DS} = 75V, I_D = 80A$
 $R_{DS(ON)} < 8m\Omega @ V_{GS} = 10V$ (Typ: $6.5m\Omega$)
- Special process technology for high ESD capability
- Special designed for Convertors and power controls
- High density cell design for ultra low R_{dson}
- Fully characterized Avalanche voltage and current
- Good stability and uniformity with high E_{AS}
- Excellent package for good heat dissipation

Application

- Power switching application
- Hard Switched and High Frequency Circuits
- Uninterruptible Power Supply

100% UIS TESTED!
100% ΔV_{ds} TESTED!



Schematic diagram



Marking and pin assignment



TO-247 top view

Package Marking and Ordering Information

Device Marking	Device	Device Package	Reel Size	Tape width	Quantity
NCE7580T	NCE7580T	TO-247	-	-	-

Absolute Maximum Ratings ($T_A = 25^\circ C$ unless otherwise noted)

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	V_{DS}	75	V
Gate-Source Voltage	V_{GS}	± 25	V
Drain Current-Continuous	I_D	80	A
Drain Current-Continuous ($T_C = 100^\circ C$)	$I_D (100^\circ C)$	60	A
Pulsed Drain Current	I_{DM}	320	A
Maximum Power Dissipation	P_D	180	W
Peak diode recovery voltage	dv/dt	30	V/ns
Derating factor		1.2	W/ $^\circ C$
Single pulse avalanche energy ^(Note 5)	E_{AS}	600	mJ
Operating Junction and Storage Temperature Range	T_J, T_{STG}	-55 To 175	$^\circ C$

Thermal Characteristic

Thermal Resistance, Junction-to- Case ^(Note 2)	$R_{\theta jc}$	0.83	°C/W
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Electrical Characteristics ($T_A=25^\circ\text{C}$ unless otherwise noted)

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Off Characteristics						
Drain-Source Breakdown Voltage	BV_{DSS}	$V_{GS}=0V, I_D=250\mu A$	75	84	-	V
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS}=100V, V_{GS}=0V$	-	-	1	μA
Gate-Body Leakage Current	I_{GSS}	$V_{GS}=\pm 25V, V_{DS}=0V$	-	-	± 100	nA
On Characteristics ^(Note 3)						
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS}=V_{GS}, I_D=250\mu A$	2	2.85	4	V
Drain-Source On-State Resistance	$R_{DS(ON)}$	$V_{GS}=10V, I_D=30A$	-	6.5	8	m Ω
Forward Transconductance	g_{FS}	$V_{DS}=5V, I_D=30A$	-	66	-	S
Dynamic Characteristics ^(Note 4)						
Input Capacitance	C_{iss}	$V_{DS}=25V, V_{GS}=0V,$ $F=1.0\text{MHz}$	-	4400	-	PF
Output Capacitance	C_{oss}		-	340	-	PF
Reverse Transfer Capacitance	C_{rss}		-	260	-	PF
Switching Characteristics ^(Note 4)						
Turn-on Delay Time	$t_{d(on)}$	$V_{DD}=30V, I_D=2A, R_L=15\Omega$ $V_{GS}=10V, R_G=2.5\Omega$	-	17.8	-	nS
Turn-on Rise Time	t_r		-	11.8	-	nS
Turn-Off Delay Time	$t_{d(off)}$		-	56	-	nS
Turn-Off Fall Time	t_f		-	14.6	-	nS
Total Gate Charge	Q_g	$V_{DS}=24V, I_D=40A,$ $V_{GS}=10V$	-	100	-	nC
Gate-Source Charge	Q_{gs}		-	20	-	nC
Gate-Drain Charge	Q_{gd}		-	30	-	nC
Drain-Source Diode Characteristics						
Diode Forward Voltage ^(Note 3)	V_{SD}	$V_{GS}=0V, I_S=40A$	-	-	1.2	V
Diode Forward Current ^(Note 2)	I_S		-	-	80	A
Reverse Recovery Time	t_{rr}	$T_J = 25^\circ\text{C}, I_F = 75A$ $di/dt = 100A/\mu\text{s}$ ^(Note 3)	-	35.6	50	nS
Reverse Recovery Charge	Q_{rr}		-	-	56	nC
Forward Turn-On Time	t_{on}	Intrinsic turn-on time is negligible (turn-on is dominated by LS+LD)				

Notes:

1. Repetitive Rating: Pulse width limited by maximum junction temperature.
2. Surface Mounted on FR4 Board, $t \leq 10$ sec.
3. Pulse Test: Pulse Width $\leq 300\mu\text{s}$, Duty Cycle $\leq 2\%$.
4. Guaranteed by design, not subject to production
5. EAS condition: $T_J=25^\circ\text{C}, V_{DD}=50V, V_G=10V, L=0.3\text{mH}, I_D=62A$

Test circuit

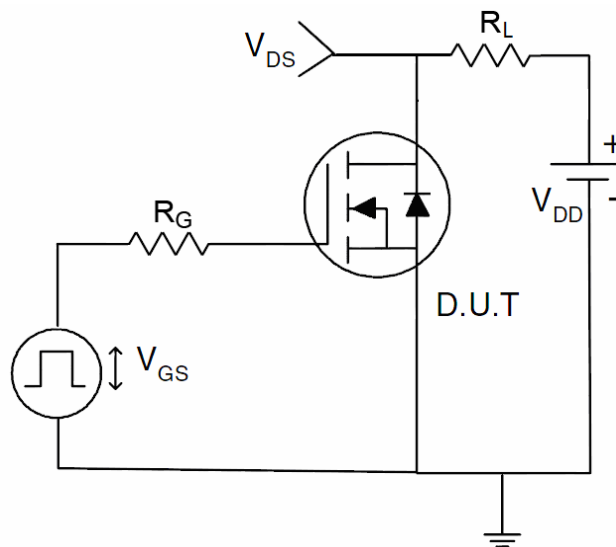
1) E_{AS} test Circuits



2) Gate charge test Circuit:



3) Switch Time Test Circuit:



Typical Electrical and Thermal Characteristics (curves)

Figure1. Safe operating area

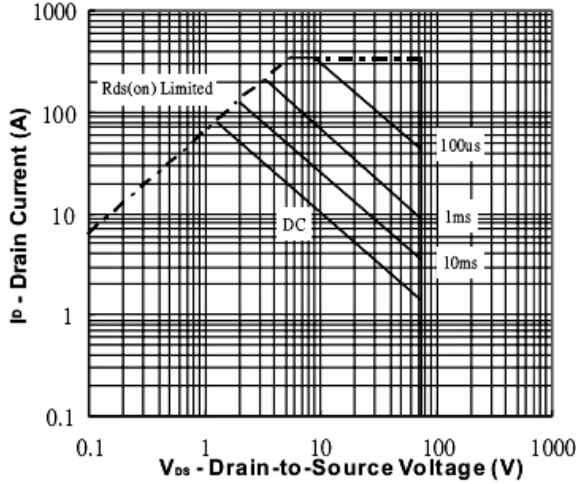


Figure2. Source-Drain Diode Forward Voltage

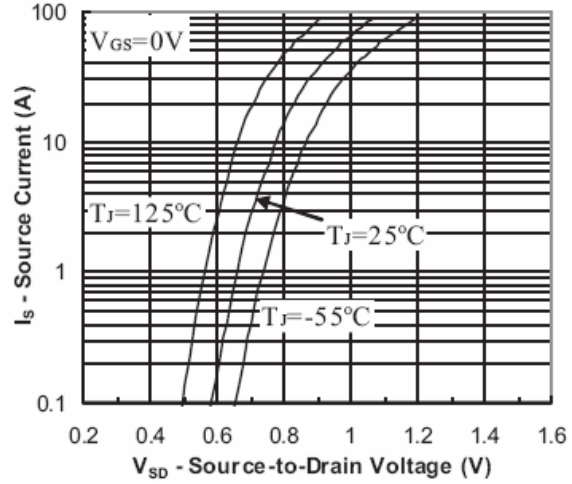


Figure3. Output characteristics

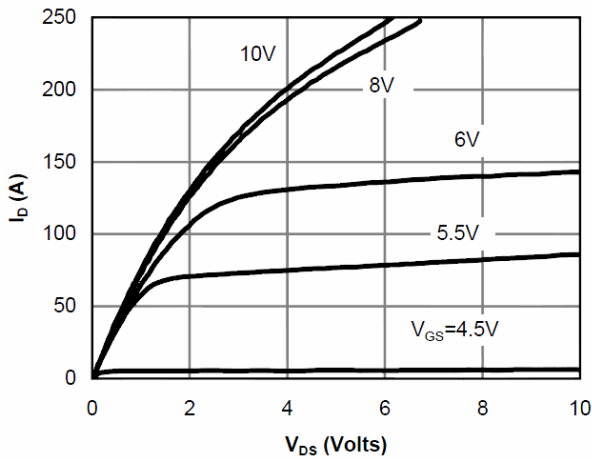


Figure4. Transfer characteristics

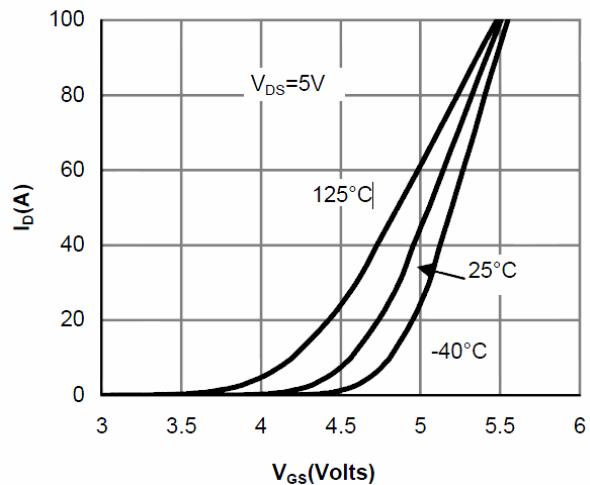


Figure5. Static drain-source on resistance

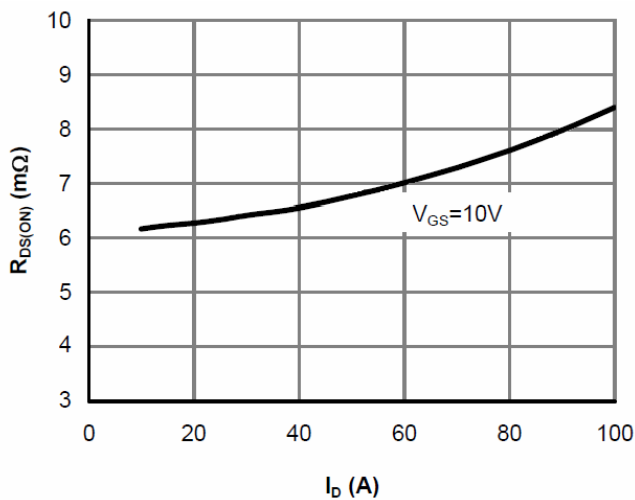


Figure6. RDS(ON) vs Junction Temperature

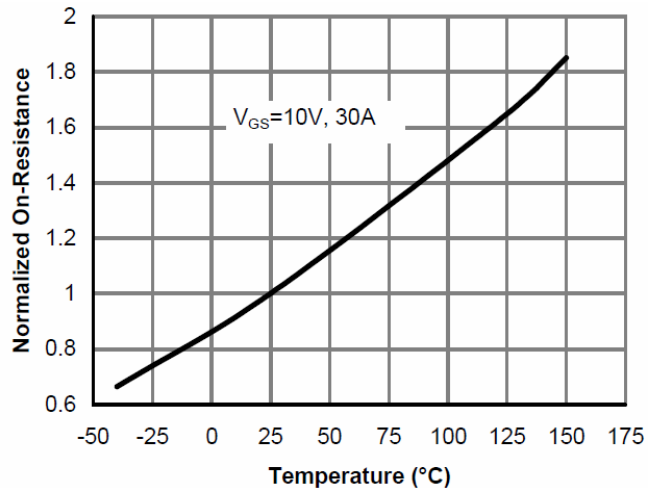


Figure7. BV_{DSS} vs Junction Temperature

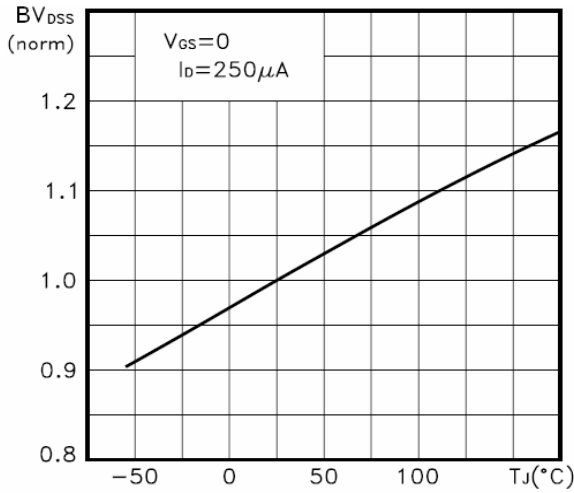


Figure8. $V_{GS(th)}$ vs Junction Temperature

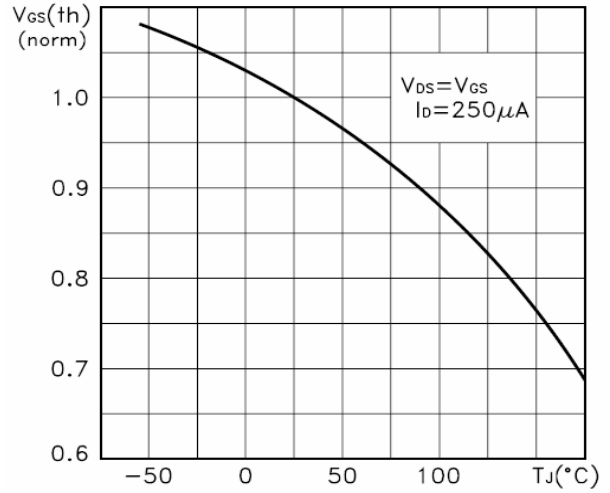


Figure9. Gate charge waveforms

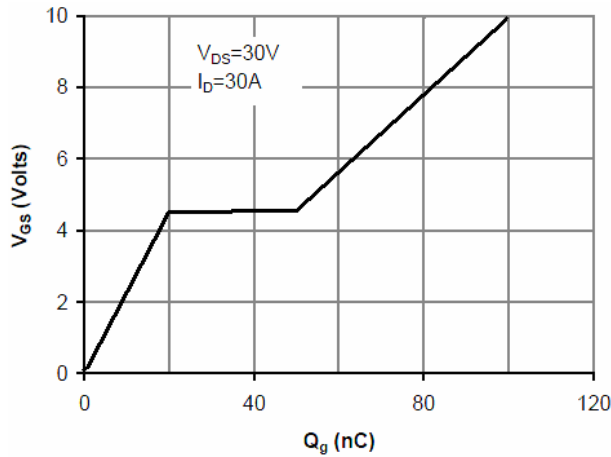
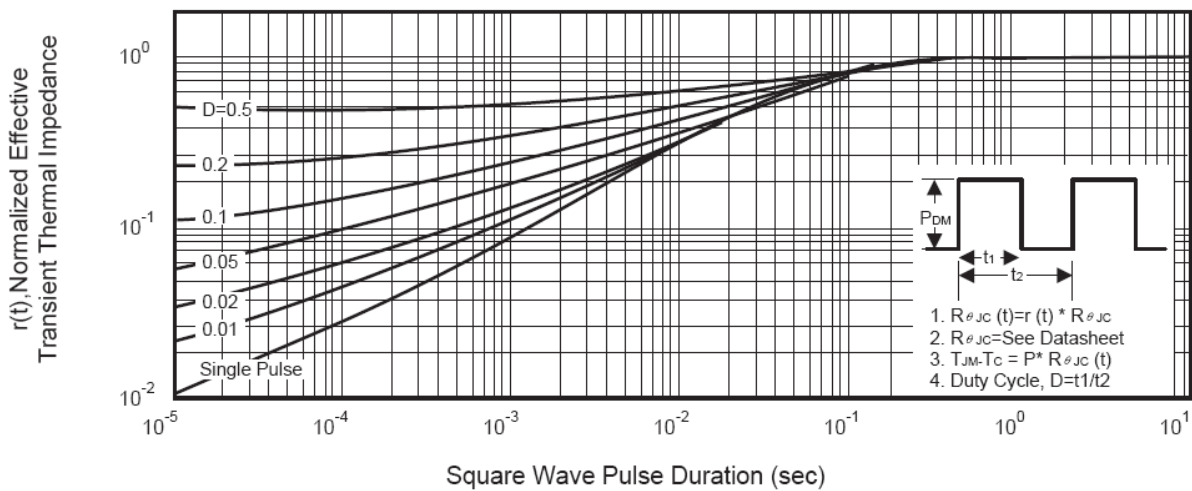
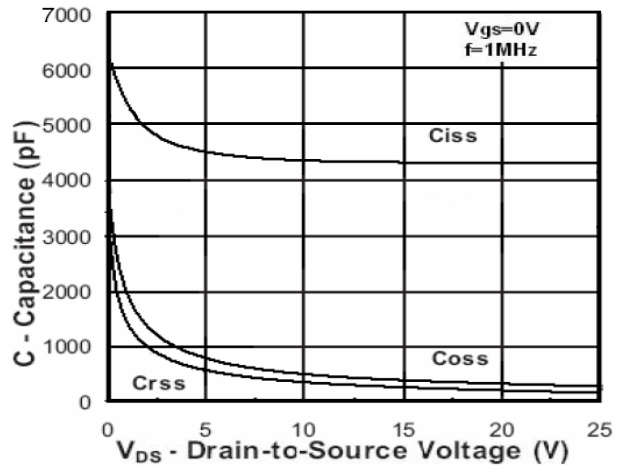
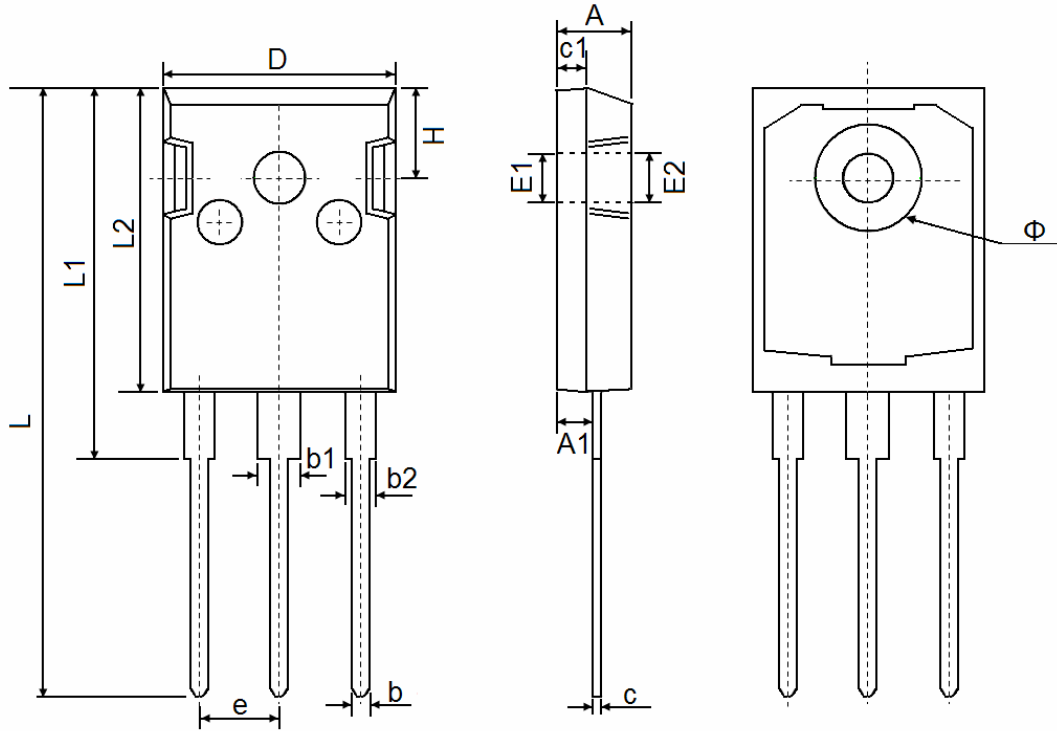


Figure10. Capacitance



TO-247 Package Information


Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	4.850	5.150	0.191	0.200
A1	2.200	2.600	0.087	0.102
b	1.000	1.400	0.039	0.055
b1	2.800	3.200	0.110	0.126
b2	1.800	2.200	0.071	0.087
c	0.500	0.700	0.020	0.028
c1	1.900	2.100	0.075	0.083
D	15.450	15.750	0.608	0.620
E1	3.500 REF		0.138 REF	
E2	3.600 REF		0.142 REF	
L	40.900	41.300	1.610	1.626
L1	24.800	25.100	0.976	0.988
L2	20.300	20.600	0.799	0.811
Φ	7.100	7.300	0.280	0.287
e	5.450 TYP		0.215 TYP	
H	5.980 REF		0.235 REF	

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