International
IOR Rectifier

PD-97534C

(5962F1023502K)
IRUH3301A2AK
IRUH3301A2AP
+5.0V_{IN} to V_{ADJ} @3.0A

Radiation Hardended Ultra Low Dropout Adjustable Positive Linear Regulator

Product Summary

Part Number	Dropout	I_O	V_{IN}	V_{OUT}
IRUH3301A2AK	0.4V	3.0A	5.0V	ADJ
IRUH3301A2AP				

8-LEAD FLAT PACK

Description

The IRUH3301A2 is a space qualified, ultra low dropout linear regulator designed specifically for applications requiring high reliability, low noise and radiation hardness. The output voltage can be adjusted to a low 0.8V with a droput voltage of 400mV at the full rated current of 3.0 Amps.

Features

- Silicon On Insulator (SOI) CMOS Regulator IC, CMOS Latch-Up Immune, Inherently Rad Hard
- Total Dose Capability up to 300Krads(Si) (Condition A); Tested to 500Krad (Si)
- ELDRS up to 100Krad(Si) (Condition D)
- SEU Immune up to LET = 80 MeV*cm^2/mg
- Space Level Screened
- Fast Transient Response
- Timed Latch-Off Over-Current Protection
- Internal Thermal Protection
- Adjustable Output as low as 0.8V
- On/Off Control via Shutdown Pin, Power Sequencing Easily Implemented
- Isolated Hermetic 8-Lead Flat Pack Ensures Higher Reliability
- This part is also available in MO-078 Package as IRUH3301A2BK / IRUH3301A2BP

Absolute Maximum Ratings

Parameter	Symbol	Min.	Max.	Units
Power Dissipation @ T_C = 125°C	P_D	-	25	W
Maximum Output Current @ Maximum Power Dissipation with no Derating	I_O	-	See Fig 4	A
Non-Operating Input Voltage	V_{IN}	-0.3	+8.0	V
Operating Input Voltage	V_{IN}	2.9	6.4	
Ground	GND	-0.3	0.3	
Shutdown Pin Voltage	V_{SHDN}	-0.3	V_{IN} + 0.3	
Output Pin Voltage	V_{OUT}	-0.3	V_{IN} + 0.3	
Operating Case Temperature Range	T_O	-55	+140	°C
Storage Temperature Range	T_S	-65	+150	
Maximmum Junction Temperature	T_J	-	+150	
Lead Temperature (Soldering 10sec)	T_L	-	+300	
Pass Transistor Thermal Resistance, Junction to Case	R_{THJC}	-	1.0	°C/W

Electrical Characteristics ①
Pre-Radiation @T_C = 25°C, V_{IN} = 5.0V (Unless Otherwise Specified)

Parameter	Test Conditions	Symbol	Min.	Typ.	Max.	Units
Reference Voltage (Measured @ ADJ Pin)	3.8V ≤ V_{IN} ≤ 5.8V, 50mA ≤ I_{OUT} ≤ 3.0A	V_{OUT}	0.788	0.800	0.812	V
	3.8V ≤ V_{IN} ≤ 5.8V, 50mA ≤ I_{OUT} ≤ 3.0A, -55°C to +125°C		0.776	0.800	0.824	
	3.8V ≤ V_{IN} ≤ 5.8V, 50mA ≤ I_{OUT} ≤ 3.0A, Post -Rad		0.772	0.800	0.816	
Dropout Voltage ①	I_O = 3.0A, V_{OUT} = 4.4V, -55°C to +125°C, Post -Rad	V_{DROP}	-	-	0.4	V
Current Limit	Over-Current Latching, -55°C to +125°C, Post -Rad	I_{LATCH}	3.5	-	-	A
Over-Current Time-to-Latch	I_O > I_{LATCH}	t_{LATCH}	-	10	-	ms
Maximum Shutdown Temp.②		T_{LATCH}	125	140	-	°C
Ripple Rejection②	F= 120Hz, I_O = 50mA, -55°C to +125°C	PSRR	65	-	-	dB
	F= 120Hz, I_O = 50mA, Post -Rad		40	-	-	
ADJ Pin Current ②	-55°C to +125°C	I_{ADJUST}	-	1.6	-	mA
Minimum SHDN Pin "On" Threshold Voltage	I_{SOURCE} = 200µA, -55°C to +125°C Post -Rad	V_{SHDN}	-	-	0.8	V
Maximum SHDN Pin "Off" Threshold Voltage	I_{SOURCE} = 200µA, -55°C to +125°C Post -Rad	V_{SHDN}	1.2	-	-	V
Output Voltage at Shutdown	R_{LOAD} = 36 Ohms, V_{SHDN} = 3.3V -55°C to +125°C, Post-Rad	V_{OUT}	-0.1	-	0.1	V
SHDN Pin Leakage Current ②	V_{SHDN} = 3.3V, -55°C to +125°C,Post-Rad	I_{SHDN}	-10	-	10	µA
SHDN Pin Pull-Up Current ②	V_{SHDN} = 0.4V	I_{SHDN}	-98	-	-56	µA
	V_{SHDN} = 0.4V, -55°C to +125°C		-140	-	-30	
	V_{SHDN} = 0.4V, Post-Rad		-98	-	-56	
Power On Reset Threshold ②	Sweep V_{IN} and Measure Output	V_{T-POR}	-	1.7	-	V
Quiescent Current ②	No Load	I_Q	-	-	15	mA
	Full Load		-	-	90	

Notes:

① Connected as shown in Fig.1 and measured at the junction of V_{OUT} and ADJ Pins.

② Under normal closed-loop operation. Guaranteed by design. Not tested in production.

Radiation Performance Characteristics

Test	Conditions	Min	Typ	Unit
Total Ionizing Dose (Gamma)	MIL-STD-883, Method 1019 (Condition A) Operating Bias applied during exposure Minimum Rated Load, Vin = 6.4V	300	500 ①	Krads (Si)
Total Ionizing Dose (Gamma)	MIL-STD-883, Method 1019 (Condition D) (ELDRS) Operating Bias applied during exposure Minimum Rated Load, Vin = 6.4V	100	See ②	Krads (Si)
Single Event effects SEU, SEL, SEGR, SEB	Heavy Ions (LET) Operating Bias applied during exposure under varying operating conditions	84		MeV*cm^2/mg
Neutron Fluence	MIL-STD-883, Method 1017		1.0e^{11}	Neutrons/cm^2

Notes:

① Tested to 500Krad (Si).

② See Fig. 5.

Space Level Screening Requirements

TEST/INSPECTION	SCREENING LEVEL	MIL-STD-883
	SPACE	METHOD
Nondestructive Bond Pull	100%	2023
Internal Visual	100%	2017
Seal	100%	1014
Temperature Cycle	100%	1010
Constant Acceleration	100%	2001
Mechanical Shock	100%	2002
PIND	100%	2020
Pre Burn-In-Electrical	100%	
Burn-In	100%	1015
Final Electrical	100%	
Radiographic	100%	2012
External Visual	100%	2009

Application Information

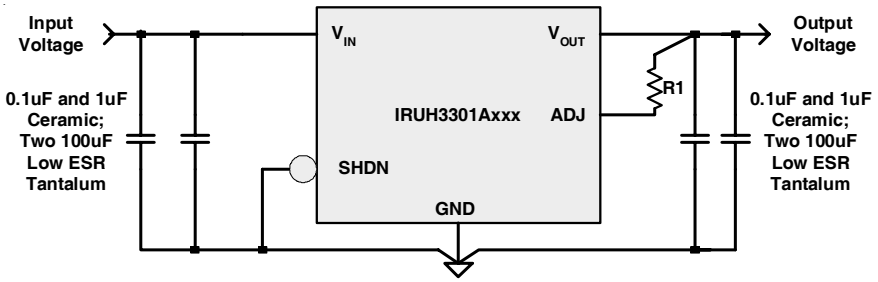


Fig. 1. Typical Regulator Circuit; Note the SHDN Pin is hardwired in the "ON" position. The ADJ Pin is connected as noted in the "General Layout Rules" section.

Setting the Output Voltage

Choose R1 based upon the desired output voltage using the formula below.

$$R1 = \left(\frac{V_{OUT}}{0.800V} - 1 \right) * 499\Omega$$

Table 1 shows the closest nominal 0.1% tolerance R1 value to provide a given output voltage.

Table 1- Values of R1 for a Given Output Voltage

V_{OUT} (V)	0.9	1.0	1.2	1.5	1.8	2.5	3.3
Nearest R1 Value (0.1%), (Ohms)	61.9	124	249	437	619	1060	1560

Over-Current & Over-Temperature Protection

The IRUH3301 series provides over-current protection by means of a timed latch function. Drive current to the internal PNP pass transistor is limited by an internal resistor (Rb in Fig. 3) between the base of the transistor and the control IC drive FET. If an over-current condition forces the voltage across this resistor to exceed 0.5V (nom), the latch feature will be triggered. The time-to-latch (t_{LATCH}) is nominally 10ms. If the over-current condition exists for less than t_{LATCH} , the latch will not be set. If the latch is set the drive current to the PNP pass transistor will be disabled. The latch will remain set until one of the following actions occur:

1. The SHDN Pin voltage is brought above 1.2V and then lowered below 0.8V.
2. The V_{IN} Pin voltage is lowered below 1.7V.

If the junction temperature of the regulator IC exceeds 140°C nominal, the thermal shutdown circuit will set the internal latch and disable the drive current to the PNP pass transistor as described above. After the junction temperature falls below a nominal 125°C, the latch can be reset using either of the actions described above.

Under-Voltage Lock-Out

The under-voltage lock-out (UVLO) function prevents operation when V_{IN} is less than 1.7V (nominal). There is a nominal 100mV hysteresis about this point.

Input Voltage Range

The device control functions fully when V_{IN} is greater than 2.9V. The output current may need to be reduced to avoid the activation of over current protection at 2.9V < V_{IN} < 3.8V. The IRUH3301A1 is recommended for performance optimization when 2.9V < V_{IN} < 3.8V is required. The device enters into under-voltage lock-out when V_{IN} < 1.7V (nominal). When 1.7V (nominal) < V_{IN} < 2.9V, V_{OUT} will track V_{IN} and overshoot may occur. A larger output capacitor should be used to slow down the V_{OUT} rise rate for slow V_{IN} ramp applications.

Shutdown (SHDN)

The regulator can be shutdown by applying a voltage of >1.2V to the SHDN Pin. The regulator will restart when the SHDN Pin is pulled below the shutdown threshold of 0.8V. If the remote shutdown feature is not required, the SHDN Pin should be connected to GND.

Input Capacitance

Input bypass capacitors: Two (0.1µF and 1µF) ceramics and two 100µF low ESR tantalums (AVX TPS or equivalent), placed very close to the V_{IN} Pin are required for proper operation. When the input voltage supply capacitance is more than 4 inches from the device, additional input capacitance is recommended. Larger input capacitor values will improve ripple rejection further improving the integrity of the output voltage.

Output Capacitance

Output bypass capacitors: Two (0.1µF and 1µF) ceramics and two 100µF low ESR tantalums (AVX TPS or equivalent) are required for loop stability. Faster transient performance can be achieved with multiple additional 1µF ceramic capacitors. Ceramic capacitors greater than 1µF in value are not recommended as they can cause stability issues.
Tantalum capacitor values larger than the suggested value are recommended to improve the transient response under large load current changes. The upper capacitance value limit is governed by the delayed over-current latch function of the regulator and can be as much as 10,000µF without causing the device to latch-off during start-up.

General Layout Rules

Low impedance connections between the regulator output and load are essential. Solid power and ground planes are highly recommended. In those cases where the board impedances are not kept very small, oscillations can occur due to the effect of parasitic series resistance and inductance on loop bandwidth and phase margin.

R1 must be directly conected to the V_{OUT} Pin using as short a trace as possible with the connection inside the first bypass capacitor (see Fig. 2a). The trace from ADJ Pin to R1 should be as short as possible.

Connect ceramic output capacitors directly across the V_{OUT} and GND Pins with as wide a trace as design rules allow (see Fig. 2a). Avoid the use of vias for these capacitors and avoid loops. Fig.2 shows the ceramic capacitors tied directly to the regulator output.

The input capacitors should be connected as close a possible to the V_{IN} Pin.

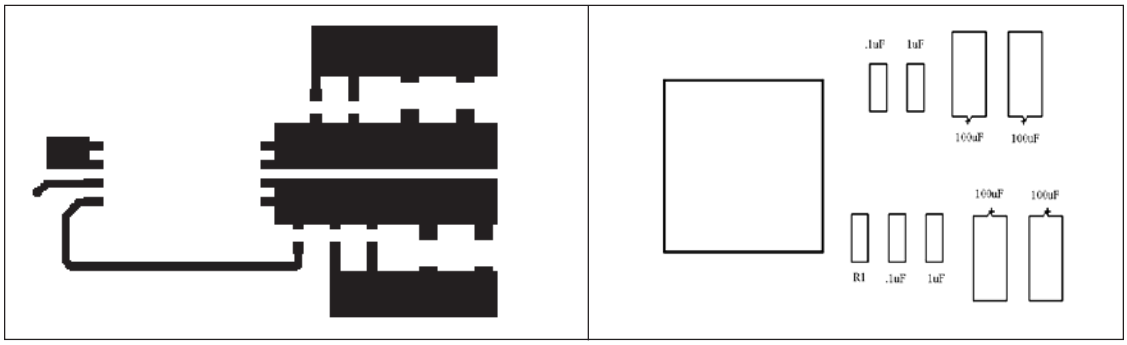


Fig. 2a. Layer 1 conductor.
Ground plane below layer 1

Fig. 2b. Layer 1 silkscreen

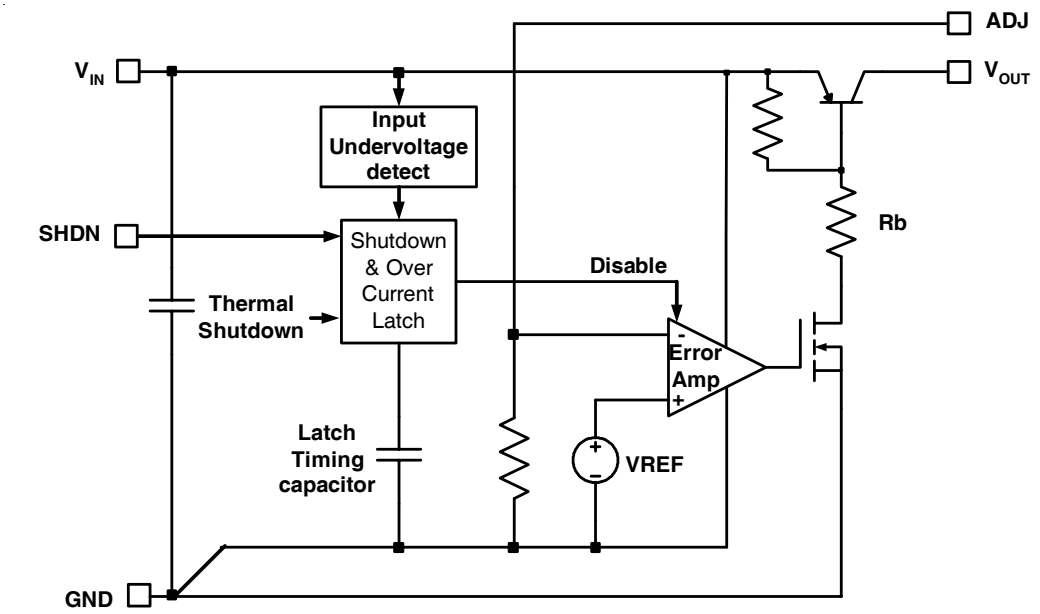


Fig. 3. Simplified Schematic Circuit

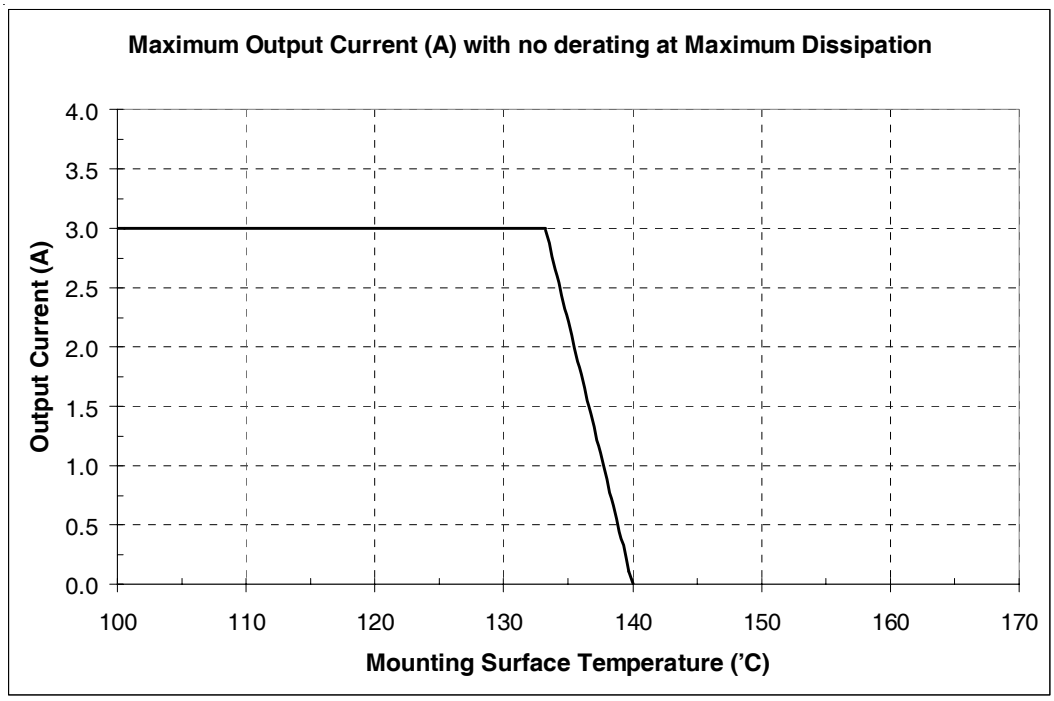


Fig. 4. Maximum Output Current versus Mounting Surface Temperature with no Derating at Maximum Dissipation

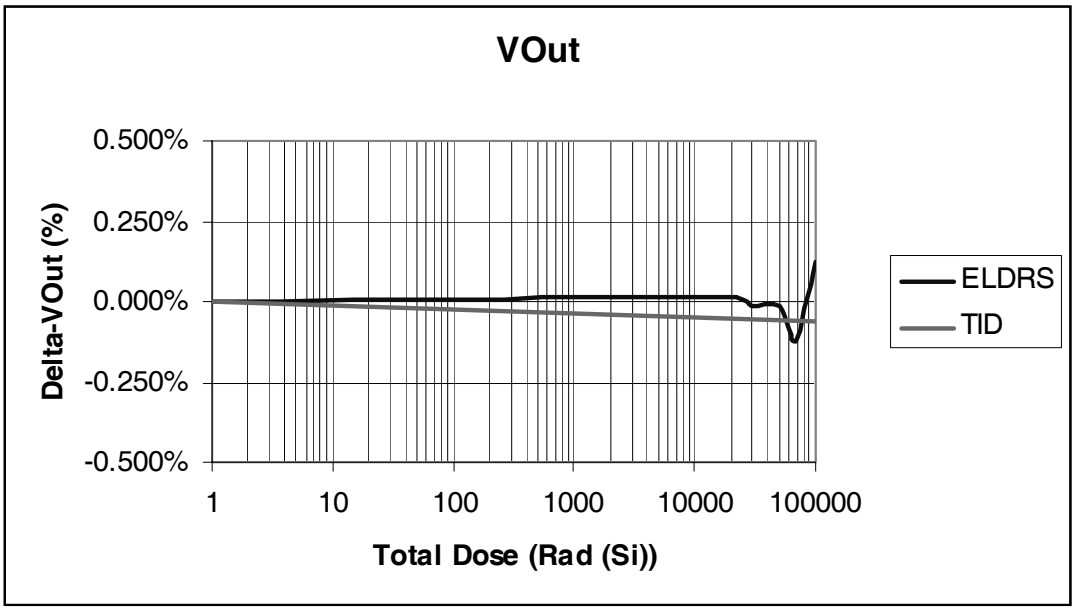


Fig. 5. Change in Output Voltage vs. Total Ionizing Dose Radiation Exposure at Both High and Low Dose Rates

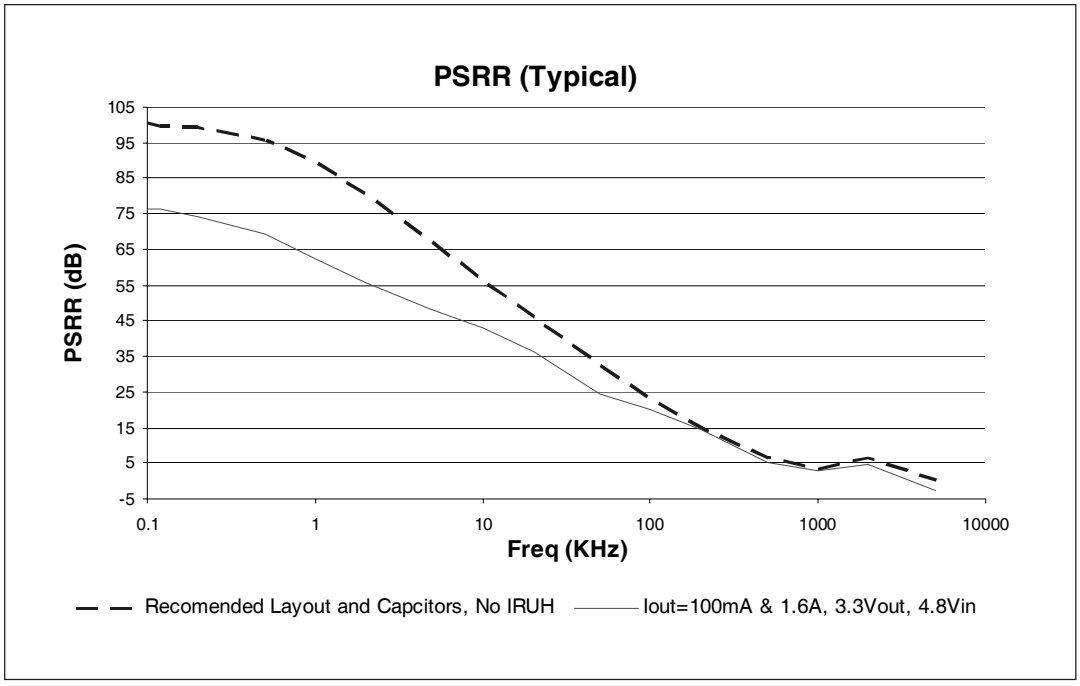
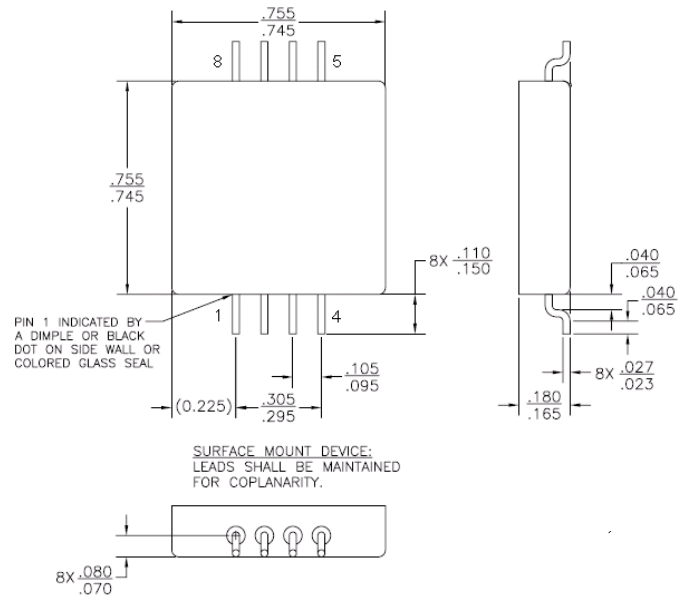


Fig. 6. Typical Power Supply Ripple Rejection at 100mA and 1.6A using recommended layout and capacitors. Results above 10KHz are influenced by testing setup and layout.

Fig 7. Case Outline and Dimensions - 8-Lead Flat Pack (Lead Form Down)



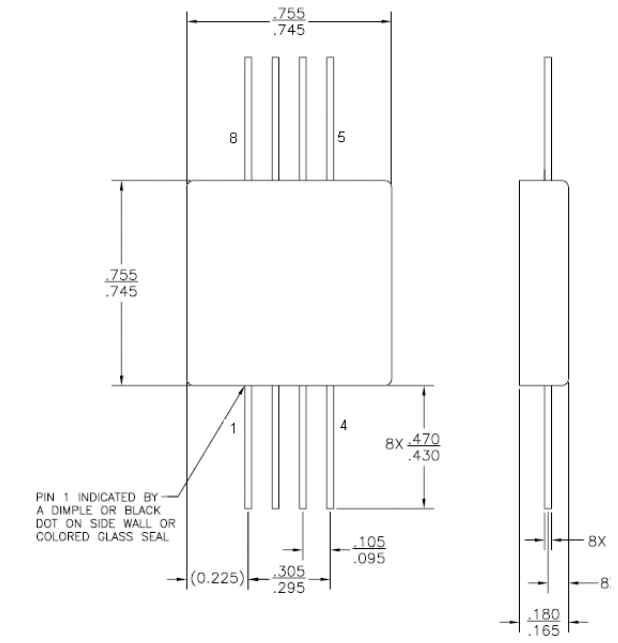
Pin Assignment

Pin #	Pin Description
1	GND
2	GND
3	SHUTDOWN
4	V_{ADJ}
5	V_{OUT}
6	V_{OUT}
7	V_{IN}
8	VIN

Note:
1) All dimensions are in inches

Warning: This Product contains BeO

Fig 8. Case Outline and Dimensions - 8-Lead Flat Pack (Lead Trimmed)



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8	VIN

Note:
1) All dimensions are in inches

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Part Numbering Nomenclature

IR U H3 301 A2 A K

Linear Regulator
U = Ultra Low Dropout Regulator

Radiation Hardening
H3 = 300 Krads

Device indicator
301 = 3 Amp Positive Regulator

Output Voltage
18 = 1.8V
25 = 2.5V
33 = 3.3V
A1 = Adjustable Optimized for 3.3 V Input
A2 = Adjustable Optimized for 5.0V Input

Package Type
A = 8 Lead Flat Pack

Screening Level
P = Unscreened. 25°C
Electrical Test Not for Qualification
K = Class K per MIL-PRF-38534

Lead Form Options
Blank = Lead Form Down (Fig. 7)
B = Lead Form Up
C = Lead Trimmed (Fig. 8)

International
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