

HVD400C

Variable Capacitance Diode for VCO

REJ03G0220-0100Z

Rev.1.00

Apr 22, 2004

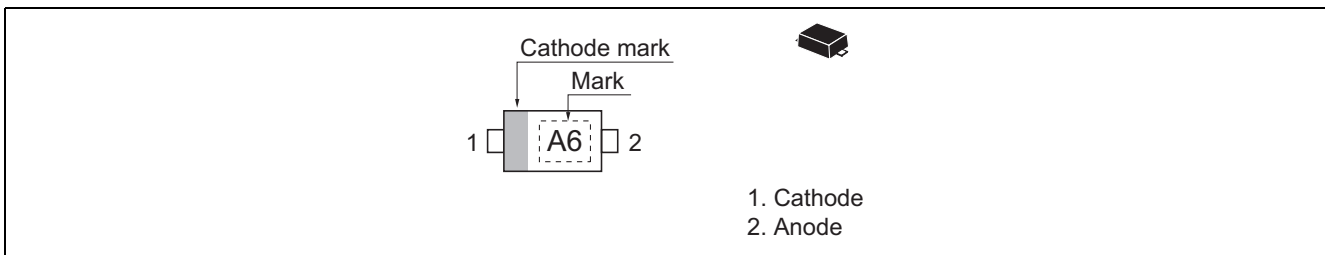
Features

- High capacitance ratio. ($n = 1.60$ min)
- Low series resistance. ($r_s = 0.70 \Omega$ max)
- Super small Flat Package (SFP) is suitable for surface mount design.

Ordering Information

Type No.	Laser Mark	Package Code
HVD400C	A6	SFP

Pin Arrangement



Absolute Maximum Ratings

(Ta = 25°C)

Item	Symbol	Value	Unit
Reverse voltage	V_R	15	V
Junction temperature	T_j	125	°C
Storage temperature	T_{stg}	-55 to +125	°C

Electrical Characteristics

(Ta = 25°C)

Item	Symbol	Min	Typ	Max	Unit	Test Condition
Reverse current	I_{R1}	—	—	10	nA	$V_R = 15\text{ V}$
	I_{R2}	—	—	50		$V_R = 15\text{ V}, T_a = 60^\circ\text{C}$
Capacitance	C_1	2.05	—	2.24	pF	$V_R = 1\text{ V}, f = 1\text{ MHz}$
	C_3	1.18	—	1.29		$V_R = 3\text{ V}, f = 1\text{ MHz}$
Capacitance ratio	n	1.60	—	1.85	—	C_1 / C_3
Series resistance	r_s	—	—	0.70	Ω	$V_R = 1\text{ V}, f = 470\text{ MHz}$

Notes: 1. Please do not use the soldering iron due to avoid high stress to the SFP package.

2. The material of lead is exposed for cutting plane. There for, soldering nature of lead tip part is considered as unquestioned. Please kindly consider soldering nature.

Main Characteristic

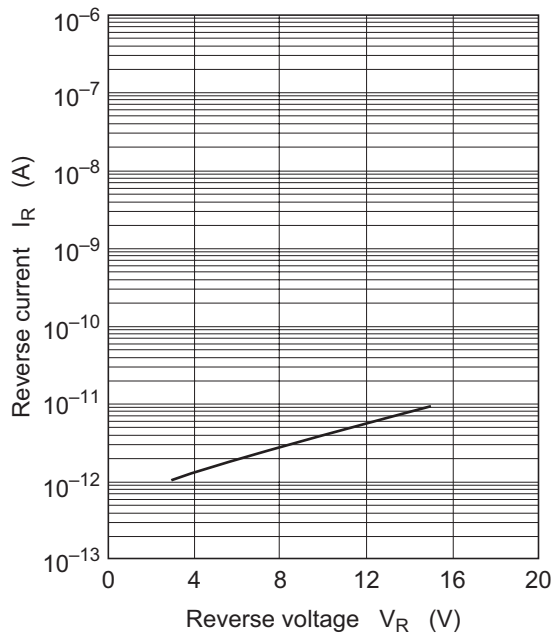


Fig.1 Reverse current vs. Reverse voltage

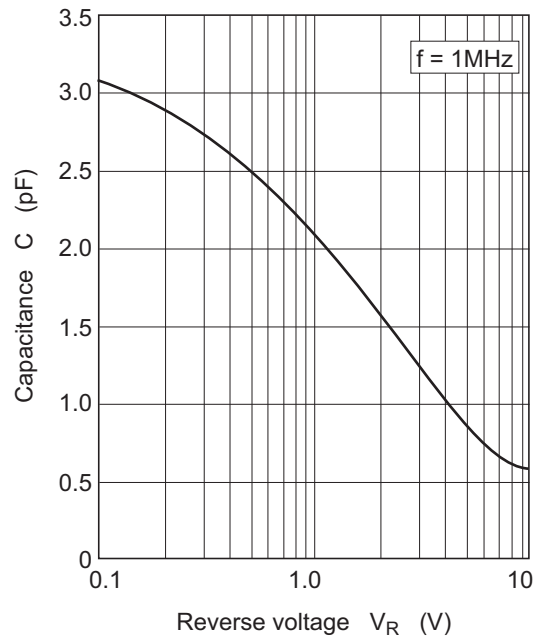


Fig.2 Capacitance vs. Reverse voltage

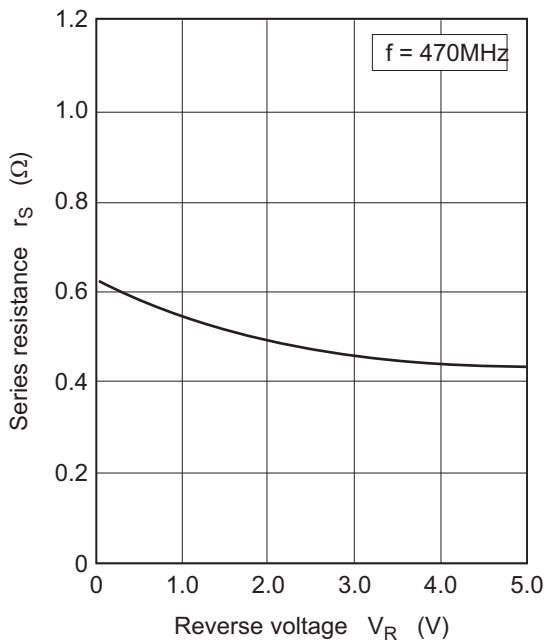


Fig.3 Series resistance vs. Reverse voltage

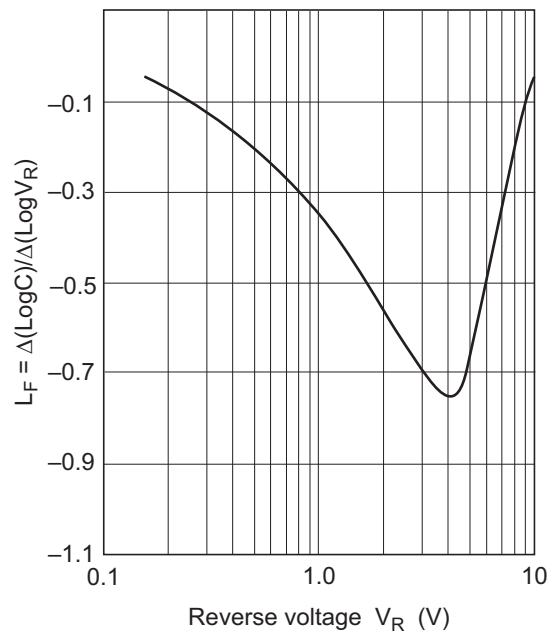
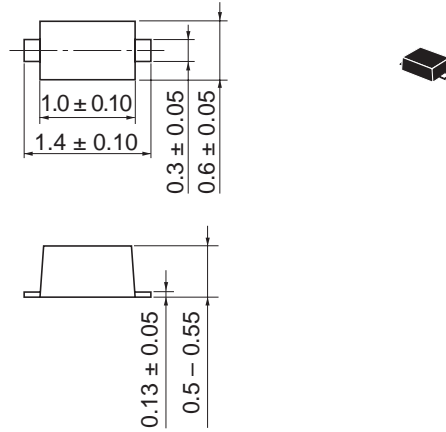


Fig.4 Linearity factor vs. Reverse voltage

Package Dimensions

As of January, 2003
Unit: mm



Package Code	SFP
JEDEC	—
JEITA	—
Mass (reference value)	0.0010 g

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