BLF574XR; BLF574XRS

Power LDMOS transistor

Rev. 1 — 20 June 2013 Product data sheet

1. Product profile

1.1 General description

A 600 W extremely rugged LDMOS power transistor for broadcast and industrial applications in the HF to 500 MHz band. This product is an enhanced version of the BLF574 using NXP's XR process to provide maximum ruggedness capability in the most severe applications without compromising the RF performance.

Table 1. Application information

Test signal	f (MHz)	V_{DS} (V)	P_L (W)	G_p (dB)	η_D (%)
CW	225	50	600	23.5	74.5
pulsed RF	225	50	600	24	74.7

1.2 Features and benefits

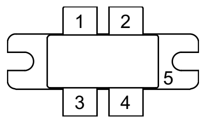
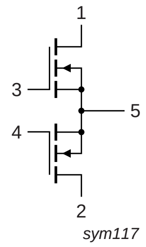
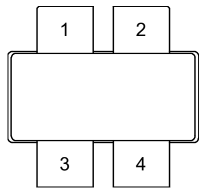
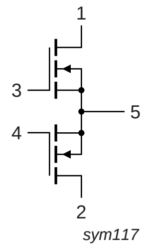
- Easy power control
- Integrated ESD protection
- Excellent ruggedness
- High efficiency
- Excellent thermal stability
- Designed for broadband operation (HF to 500 MHz)
- Compliant to Directive 2002/95/EC, regarding Restriction of Hazardous Substances (RoHS)

1.3 Applications

- Industrial, scientific and medical applications
- Broadcast transmitter applications

2. Pinning information

Table 2. Pinning

Pin	Description	Simplified outline	Graphic symbol
BLF574XR (SOT1214A)			
1	drain1		
2	drain2		
3	gate1		
4	gate2		
5	source [1]		
BLF574XRS (SOT1214B)			
1	drain1		
2	drain2		
3	gate1		
4	gate2		
5	source [1]		

[1] Connected to flange.

3. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
BLF574XR	-	flanged ceramic package; 2 mounting holes; 4 leads	SOT1214A
BLF574XRS	-	earless flanged ceramic package; 4 leads	SOT1214B

4. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DS}	drain-source voltage		-	110	V
V_{GS}	gate-source voltage		–6	+11	V
T_{stg}	storage temperature		–65	+150	°C
T_j	junction temperature	[1]	-	225	°C

[1] Continuous use at maximum temperature will affect the reliability. For details refer to the on-line MTF calculator.

5. Thermal characteristics

Table 5. Thermal characteristics

Symbol	Parameter	Conditions		Typ	Unit
$R_{th(j-c)}$	thermal resistance from junction to case	T_j = 150 °C	[1][2]	0.18	K/W

[1] T_j is the junction temperature.

[2] $R_{th(j-c)}$ is measured under RF conditions.

6. Characteristics

Table 6. DC characteristics

T_j = 25 °C; per section unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{(BR)DSS}$	drain-source breakdown voltage	V_{GS} = 0 V; I_D = 2.75 mA	110	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	V_{DS} = 10 V; I_D = 275 mA	1.25	1.7	2.25	V
I_{DSS}	drain leakage current	V_{GS} = 0 V; V_{DS} = 50 V	-	-	1.4	μA
I_{DSX}	drain cut-off current	V_{GS} = $V_{GS(th)}$ + 3.75 V; V_{DS} = 10 V	-	38	-	A
I_{GSS}	gate leakage current	V_{GS} = 11 V; V_{DS} = 0 V	-	-	140	nA
$R_{DS(on)}$	drain-source on-state resistance	V_{GS} = $V_{GS(th)}$ + 3.75 V; I_D = 9.625 A	-	0.15	-	Ω

Table 7. DC characteristics

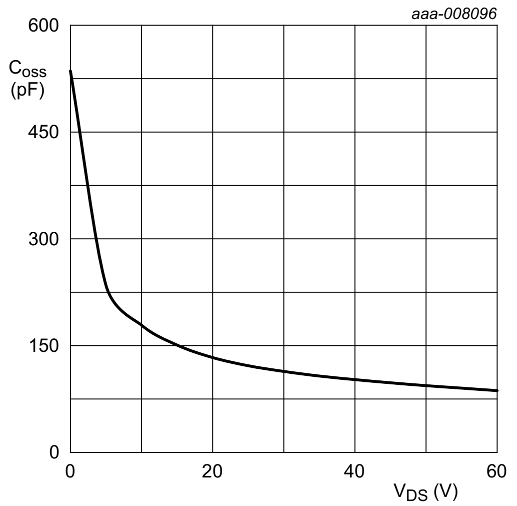
T_j = 25 °C; per section unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
C_{rs}	feedback capacitance	V_{GS} = 0 V; V_{DS} = 50 V; f = 1 MHz	-	2.4	-	pF
C_{iss}	input capacitance	V_{GS} = 0 V; V_{DS} = 50 V; f = 1 MHz	-	210	-	pF
C_{oss}	output capacitance	V_{GS} = 0 V; V_{DS} = 50 V; f = 1 MHz	-	94	-	pF

Table 8. RF characteristics

Test signal: CW; f = 225 MHz; RF performance at V_{DS} = 50 V; I_{Dq} = 100 mA; T_{case} = 25 °C; unless otherwise specified; in a class-AB production test circuit.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
G_p	power gain	P_L = 600 W	21.65	23.5	-	dB
RL_{in}	input return loss	P_L = 600 W	-	−17	−13	dB
η_D	drain efficiency	P_L = 600 W	70	74.5	-	%



V_{GS} = 0 V; f = 1 MHz.

Fig 1. Output capacitance as a function of drain-source voltage; typical values per section

7. Test information

7.1 Ruggedness in class-AB operation

The BLF574XR and BLF574XRS are capable of withstanding a load mismatch corresponding to VSWR > 65 : 1 through all phases under the following conditions: V_{DS} = 50 V; I_{Dq} = 100 mA; P_L = 600 W pulsed; f = 225 MHz.

7.2 Impedance information

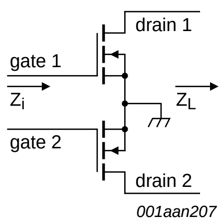


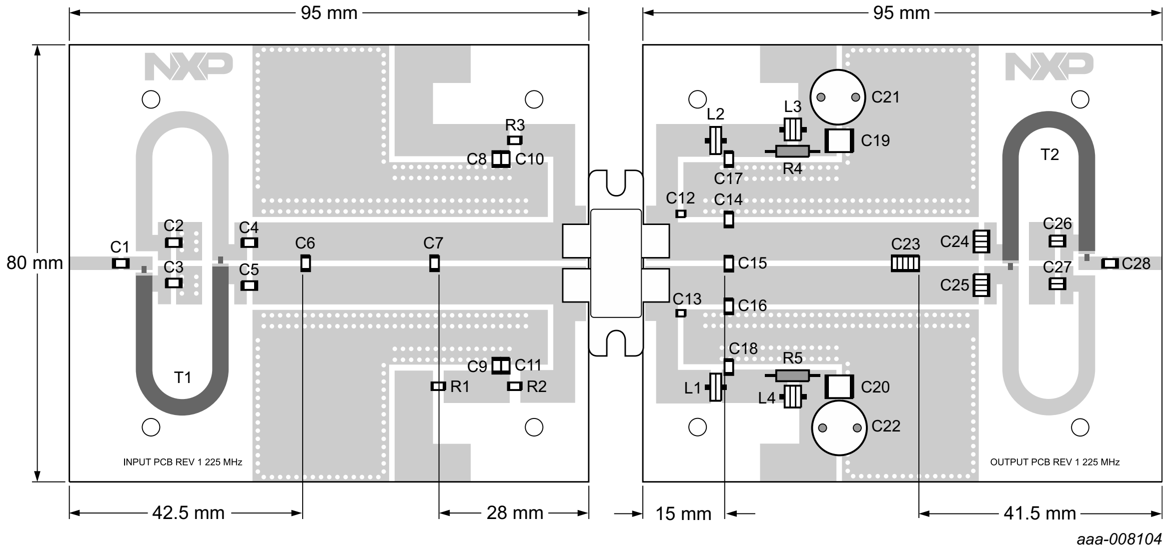
Fig 2. Definition of transistor impedance

Table 9. Typical push-pull impedance

Simulated Z_i and Z_L device impedance; impedance info at V_{DS} = 50 V and P_L = 600 W.

f (MHz)	Z_i (Ω)	Z_L (Ω)
225	4.67 – j5.47	5.66 + j2.05

7.3 Test circuit



Printed-Circuit Board (PCB) Rogers 5880: ε_r = 2.2 F/m; thickness = 0.79 mm; thickness copper plating = 35 μm.

See Table 10 for a list of components.

Fig 3. Component layout for class-AB production test circuit

Table 10. List of components

For test circuit see Figure 3.

Component	Description	Value		Remarks
C1, C2, C3, C10, C11, C17, C18	multilayer ceramic chip capacitor	1 nF	[1]	
C4, C5	multilayer ceramic chip capacitor	62 pF	[1]	
C6, C7	multilayer ceramic chip capacitor	51 pF	[1]	
C8, C9	multilayer ceramic chip capacitor	4.7 μF, 50 V		Kemet C1210X475K5RAC-T4
C12, C13	multilayer ceramic chip capacitor	33 pF	[2]	
C14, C16	multilayer ceramic chip capacitor	43 pF	[1]	
C15	multilayer ceramic chip capacitor	20 pF	[1]	
C19, C20	multilayer ceramic chip capacitor	4.7 μF; 100 V		
C21, C22	electrolytic capacitor	470 μF; 63 V		
C23	multilayer ceramic chip capacitor	5 × 12 pF	[3]	
C24, C25	multilayer ceramic chip capacitor	4 × 16 pF	[3]	
C26, C27	multilayer ceramic chip capacitor	2 × 510 pF	[3]	
C28	multilayer ceramic chip capacitor	56 pF	[1]	
L1, L2	2 turn 1 mm copper wire	D = 3 mm, length = 3 mm		
L3, L4	3 turn 1 mm copper wire	D = 3 mm, length = 3 mm		
R1	chip resistor	0 Ω		

Table 10. List of components *…continued*
For test circuit see Figure 3.

Component	Description	Value	Remarks
R2, R3	chip resistor	10 Ω	SMD 1206
R4, R5	metal film resistor	2 Ω, 0.6 W	
T1, T2	semi rigid coax	50 Ω, 58 mm	HUBER+SUHNER EZ-141-AL-TP-M17

[1] American Technical Ceramics type 100B or capacitor of same quality.

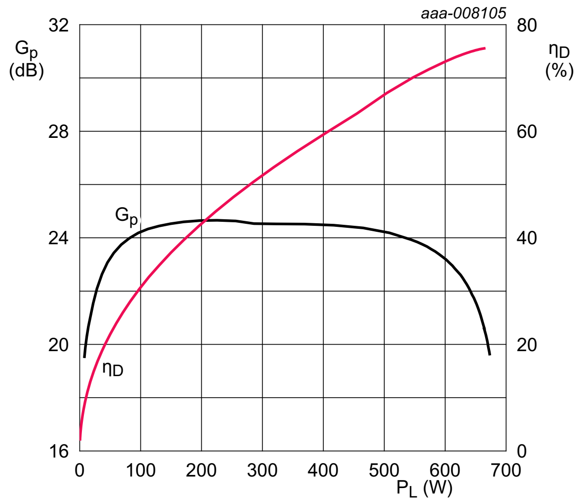
[2] American Technical Ceramics type 100A or capacitor of same quality.

[3] American Technical Ceramics type 800B or capacitor of same quality.

7.4 Graphical data

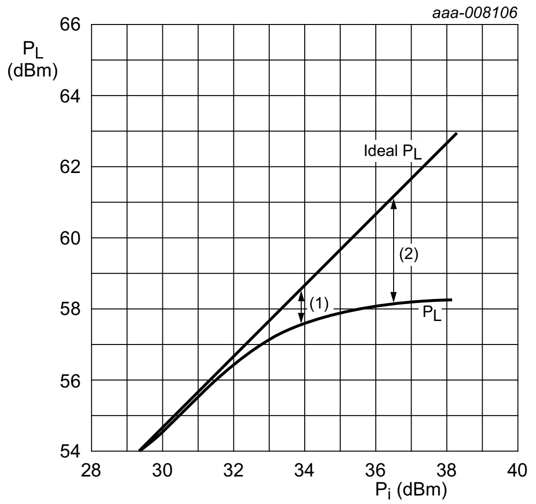
The following figures are measured in a class-AB production test circuit.

7.4.1 1-Tone CW



V_{DS} = 50 V; I_{Dq} = 100 mA; f = 225 MHz.

Fig 4. Power gain and drain efficiency as function of output power; typical values

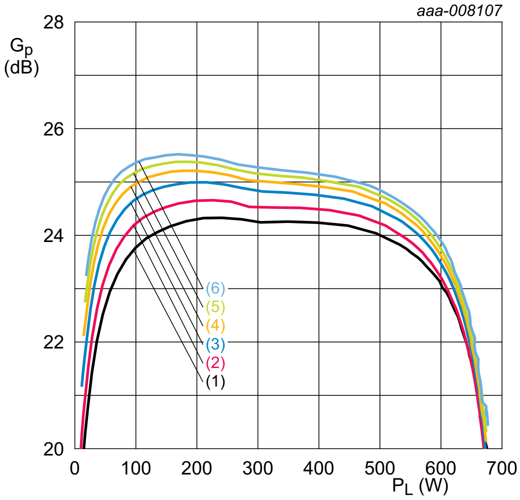


V_{DS} = 50 V; I_{Dq} = 100 mA; f = 225 MHz.

(1) $P_{L(1dB)}$ = 57.56 dBm (570 W)

(2) $P_{L(3dB)}$ = 58.13 dBm (649 W)

Fig 5. Output power as a function of input power; typical values



V_{DS} = 50 V; f = 225 MHz.

(1) I_{Dq} = 50 mA

(2) I_{Dq} = 100 mA

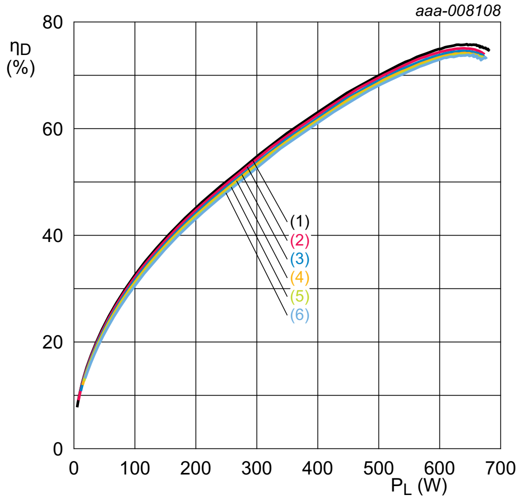
(3) I_{Dq} = 200 mA

(4) I_{Dq} = 300 mA

(5) I_{Dq} = 400 mA

(6) I_{Dq} = 500 mA

Fig 6. Power gain as a function of output power; typical values



V_{DS} = 50 V; f = 225 MHz.

(1) I_{Dq} = 50 mA

(2) I_{Dq} = 100 mA

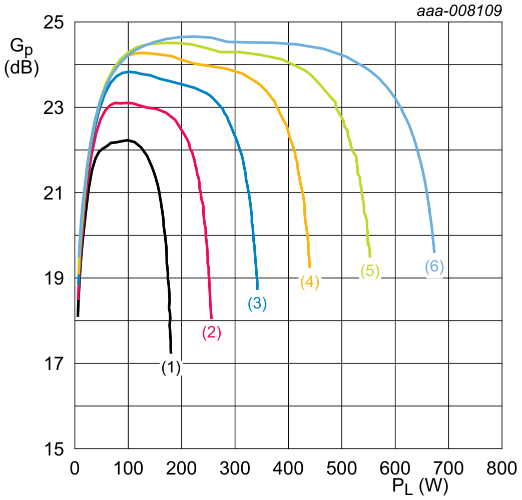
(3) I_{Dq} = 200 mA

(4) I_{Dq} = 300 mA

(5) I_{Dq} = 400 mA

(6) I_{Dq} = 500 mA

Fig 7. Drain efficiency as a function of output power; typical values



I_{Dq} = 100 mA; f = 225 MHz.

(1) V_{DS} = 25 V

(2) V_{DS} = 30 V

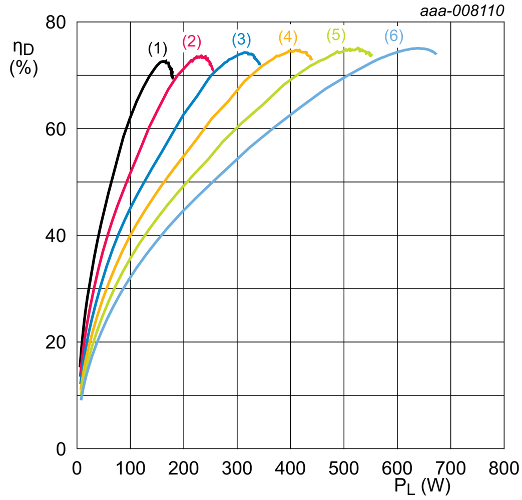
(3) V_{DS} = 35 V

(4) V_{DS} = 40 V

(5) V_{DS} = 45 V

(6) V_{DS} = 50 V

Fig 8. Power gain as a function of output power; typical values



I_{Dq} = 100 mA; f = 225 MHz.

(1) V_{DS} = 25 V

(2) V_{DS} = 30 V

(3) V_{DS} = 35 V

(4) V_{DS} = 40 V

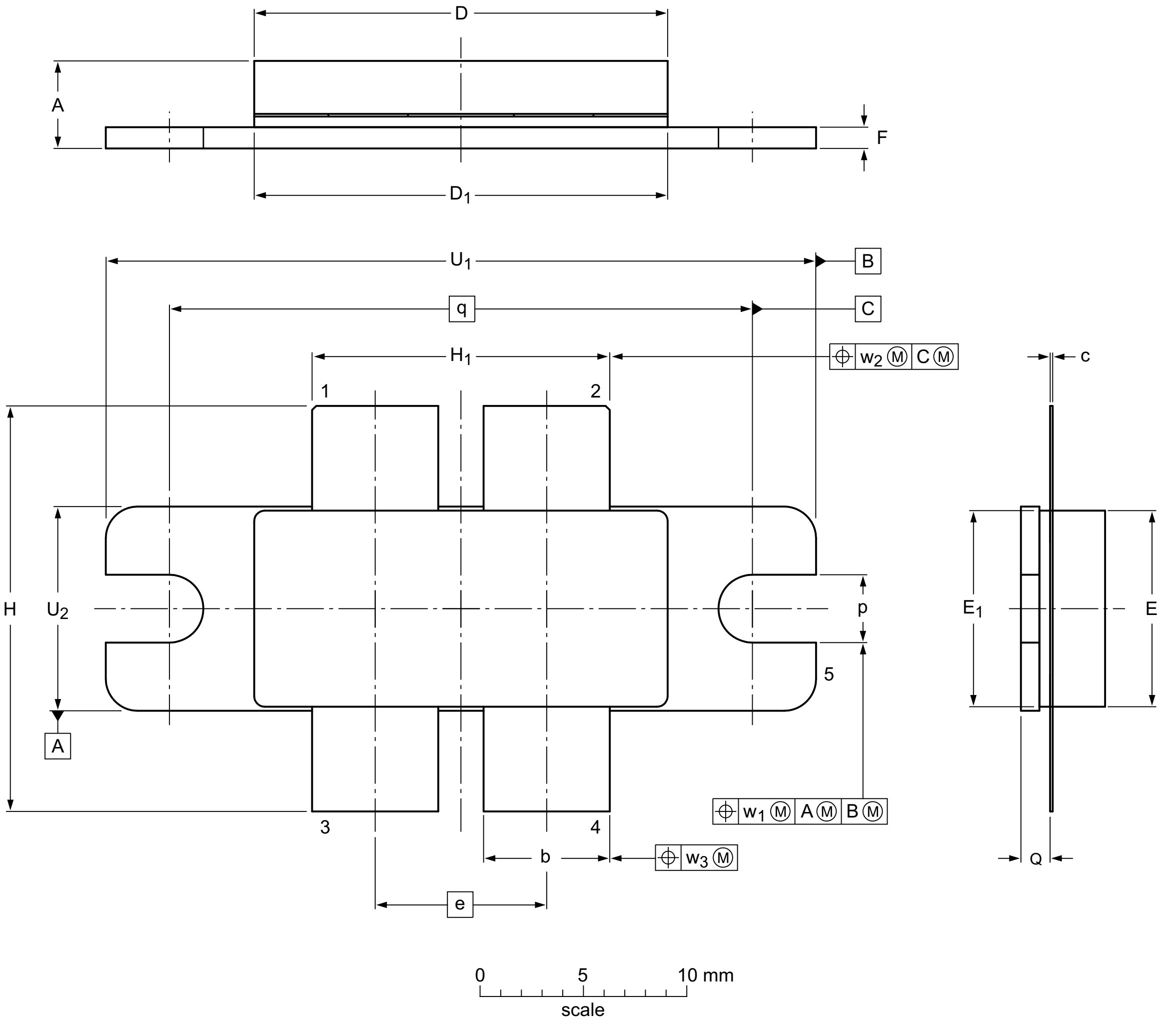
(5) V_{DS} = 45 V

(6) V_{DS} = 50 V

Fig 9. Drain efficiency as a function of output power; typical values

8. Package outline

Flanged ceramic package; 2 mounting holes; 4 leads **SOT1214A**



Dimensions

Unit(1)		A	b	c	D	D_1	e	E	E_1	F	H	H_1	p	Q(2)	q	U_1	U_2	w_1	w_2	w_3
mm	max	4.72	6.17	0.15	20.02	19.96		9.53	9.50	1.14	19.94		3.38	1.70		34.16	9.91			
	nom						8.21					14.24			27.94			0.25	0.51	0.25
	min	3.43	5.92	0.08	19.61	19.66		9.27	9.29	0.89	18.92		3.12	1.45		33.91	9.65			
inches	max	0.187	0.243	0.006	0.788	0.786		0.375	0.374	0.045	0.785		0.133	0.067		1.345	0.39			
	nom						0.323					0.56			1.10			0.01	0.02	0.01
	min	0.135	0.233	0.003	0.772	0.774		0.365	0.366	0.035	0.745		0.123	0.057		1.335	0.38			

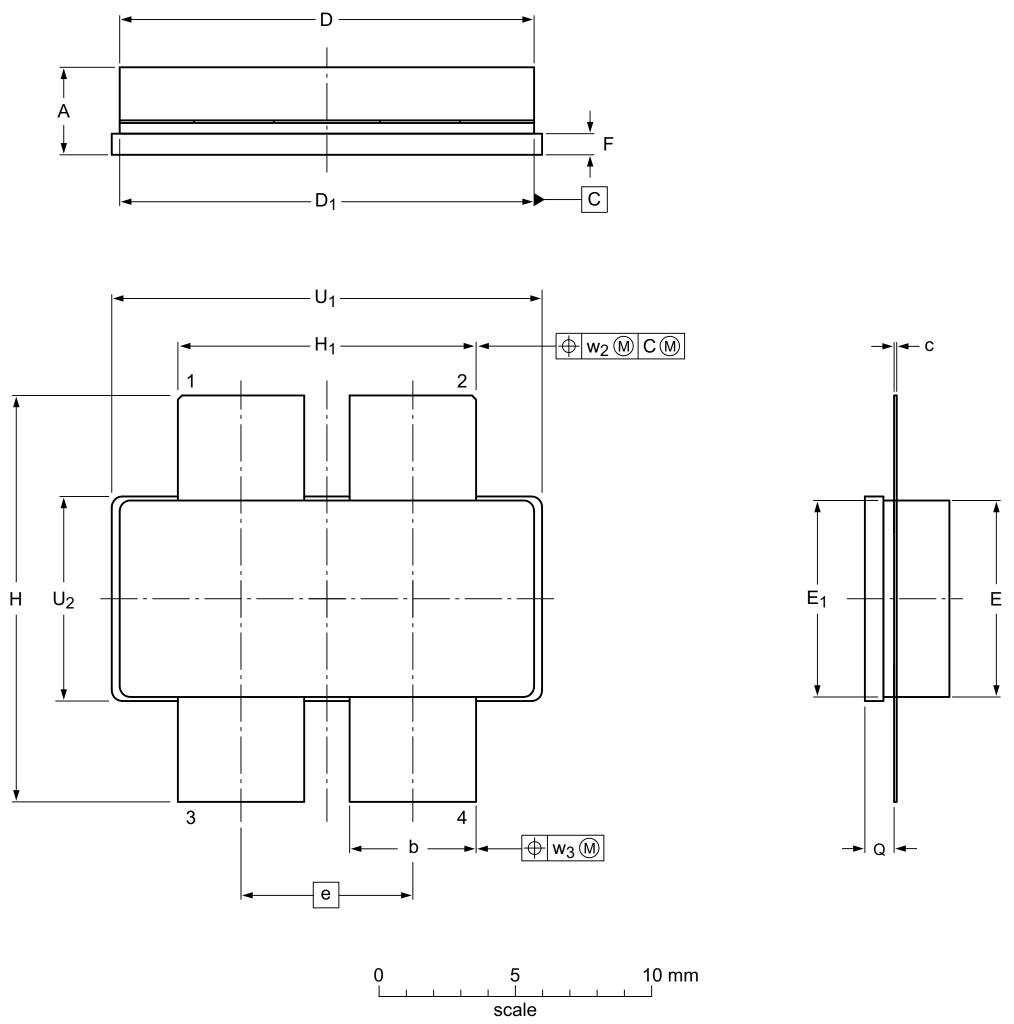
Note
1. millimeter dimensions are derived from the original inch dimensions.
2. dimension is measured 0.030 inch (0.76 mm) from body.

sot1214a_po

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
SOT1214A						~~12-08-16~~ 12-10-10

Fig 10. Package outline SOT1214A

Earless flanged ceramic package; 4 leads **SOT1214B**



Dimensions

Unit(1)		A	b	c	D	D_1	e	E	E_1	F	H	H_1	Q(2)	U_1	U_2	w_2	w_3
mm	max	4.72	6.17	0.15	20.02	19.96		9.53	9.50	1.14	19.94		1.70	20.70	9.91		
	nom						8.21					14.24				0.51	0.25
	min	3.43	5.92	0.08	19.61	19.66		9.27	9.29	0.89	18.92		1.45	20.45	9.65		
inches	max	0.187	0.243	0.006	0.788	0.786		0.375	0.374	0.045	0.785		0.067	0.815	0.39		
	nom						0.323					0.56				0.02	0.01
	min	0.135	0.233	0.003	0.772	0.774		0.365	0.366	0.035	0.745		0.057	0.805	0.38		

Note

1. millimeter dimensions are derived from the original inch dimensions.
2. dimension is measured 0.030 inch (0.76 mm) from body.

sot1214b_po

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
SOT1214B						~~11-10-05~~ 12-10-10

Fig 11. Package outline SOT1214B

9. Handling information

CAUTION

This device is sensitive to ElectroStatic Discharge (ESD). Observe precautions for handling electrostatic sensitive devices.

Such precautions are described in the *ANSI/ESD S20.20*, *IEC/ST 61340-5*, *JESD625-A* or equivalent standards.

10. Abbreviations

Table 11. Abbreviations

Acronym	Description
CW	Continuous Wave
ESD	ElectroStatic Discharge
HF	High Frequency
LDMOS	Laterally Diffused Metal-Oxide Semiconductor
MTF	Median Time to Failure
SMD	Surface Mounted Device
VSWR	Voltage Standing-Wave Ratio
XR	eXtremely Rugged

11. Revision history

Table 12. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
BLF574XR_BLF574XRS v.1	20130620	Product data sheet	-	-

12. Legal information

12.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
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