SONY

CXP836P60
CXP836P61

CMOS 8-bit Single Chip Microcomputer

Description

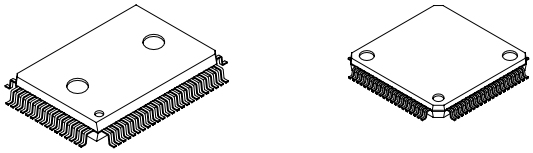
The CXP836P60/836P61 is a CMOS 8-bit single chip microcomputer integrating on a single chip an A/D converter, serial interface, timer/counter, time-base timer, sub timer/counter, LCD controller/driver and remote control reception circuit besides the basic configurations of 8-bit CPU, PROM, RAM, and I/O port.

The CXP836P60/836P61 also provides a sleep/stop function that enables lower power consumption.

The CXP836P60 and CXP836P61 are the PROM-incorporated version of the CXP83508/83512/83516/83620/83624 and CXP83509/83513/83517/83621/83625 with built-in mask ROM, and they are able to write directly into the program. Thus, it is most suitable for evaluation use during system development and for small-quantity production.

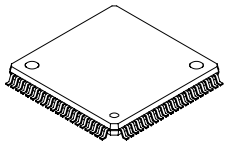
CXP836P60

80 pin QFP (Plastic) 80 pin LQFP (Plastic)



CXP836P61

80 pin QFP (Plastic)



Features

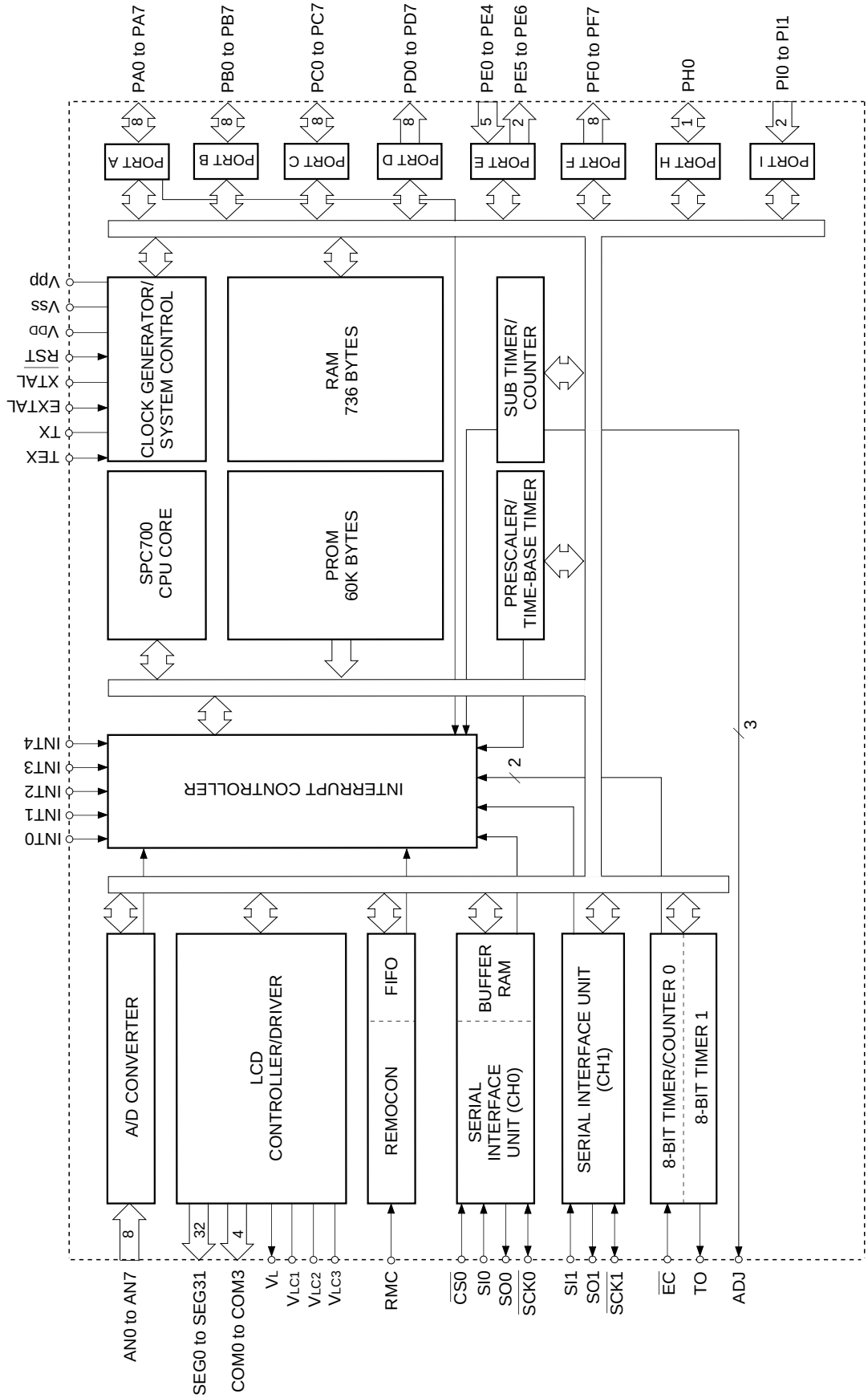
- Wide-range instruction system (213 instructions) to cover various types of data.
  — 16-bit arithmetic/multiplication and division/boolean bit operation instructions
- Minimum instruction cycle 400ns at 10MHz operation (4.5 to 5.5V)
  1µs at 4MHz operation (2.7 to 5.5V)
  122µs at 32kHz operation (2.7 to 5.5V)
- Incorporated PROM capacity 60K bytes
- Incorporated RAM capacity 736 bytes (includes LCD display data area and serial interface RAM)
- Peripheral functions
  — A/D converter 8-bit, 8-channel, successive approximation method
  (Conversion time of 12.4µs/10MHz)
  — Serial interface Incorporated buffer RAM
  (Auto transfer for 1 to 32 bytes), 1 channel
  8-bit clock synchronized type (MSB/LSB first selectable), 1 channel
  — Timer 8-bit timer, 8-bit timer/counter, 19-bit time-base timer,
  Sub timer/counter
  — LCD controller/driver Maximum 128 segment display possible (during 1/4 duty)
  4 common output, 32 segment output
  Display method static, 1/2, 1/3, 1/4 duty
  Bias method 1/2, 1/3 bias
  — Remote control reception circuit 8-bit pulse measuring counter, 6-stage FIFO
- Interruption 14 factors, 14 vectors, multi-interruption possible
- Standby mode Sleep/stop
- Package 80-pin plastic QFP/LQFP

Structure

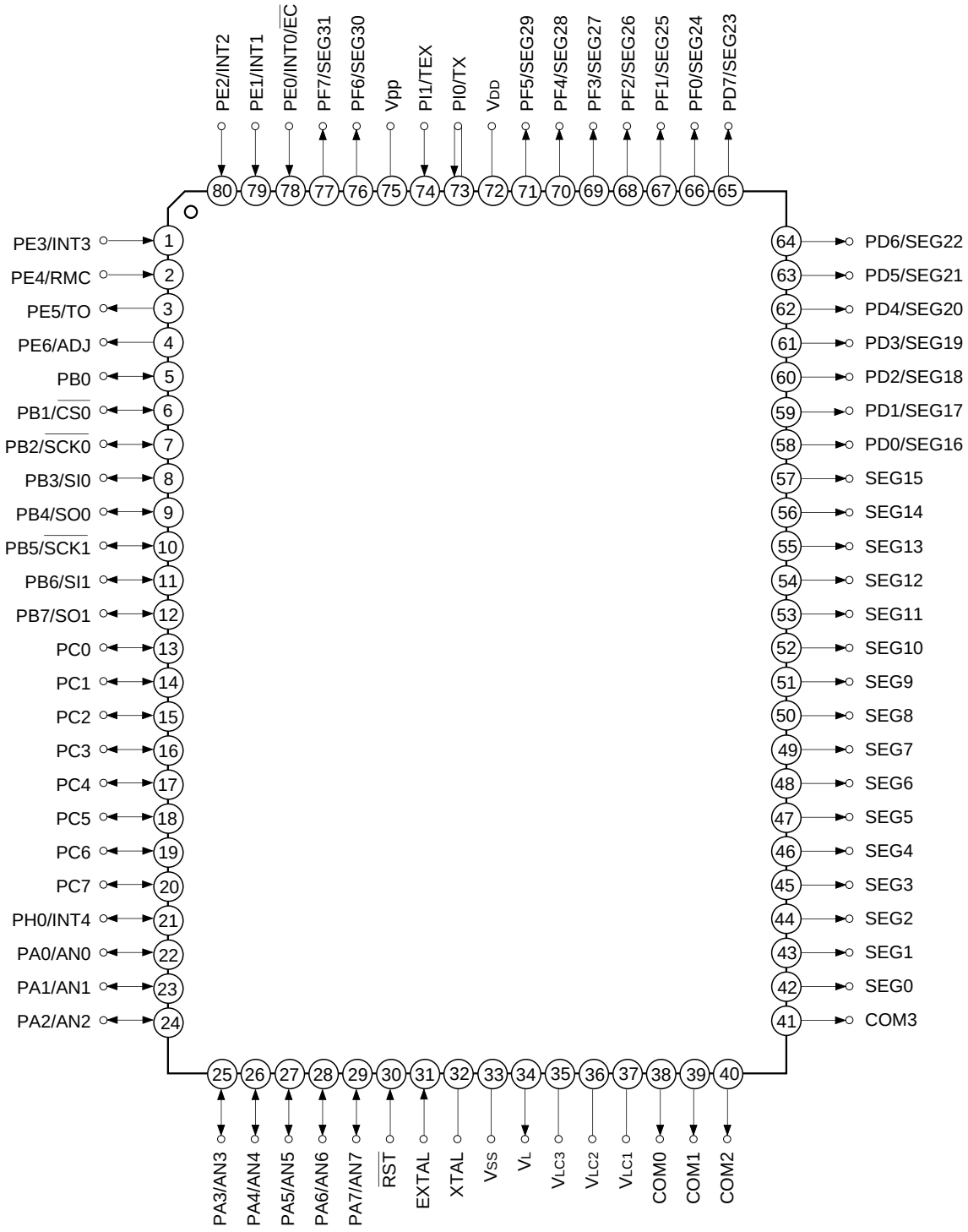
Silicon gate CMOS IC

E98342C1Y-PS

Block Diagram

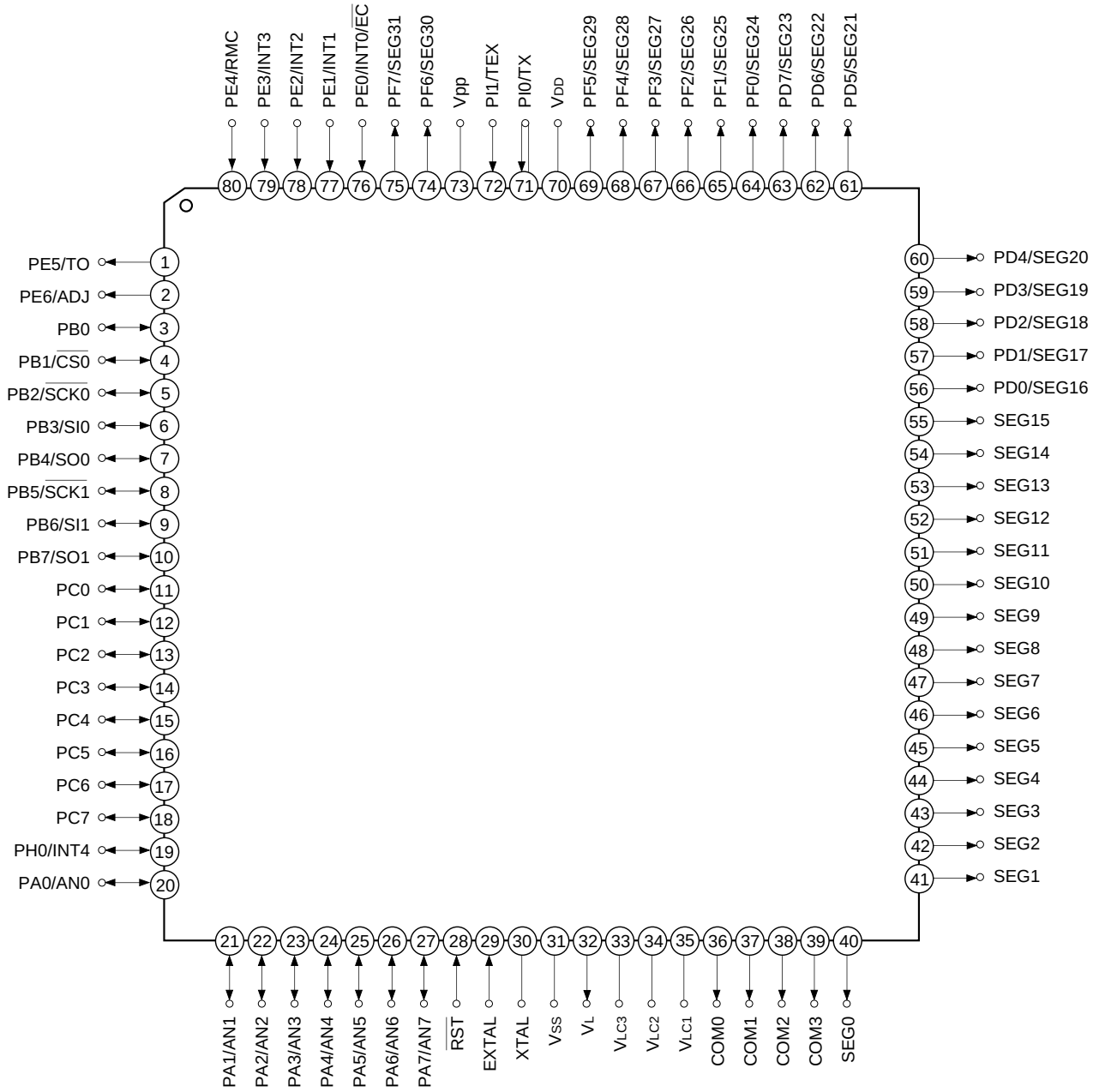


Pin Assignment (Top View) CXP836P60 (QFP package)



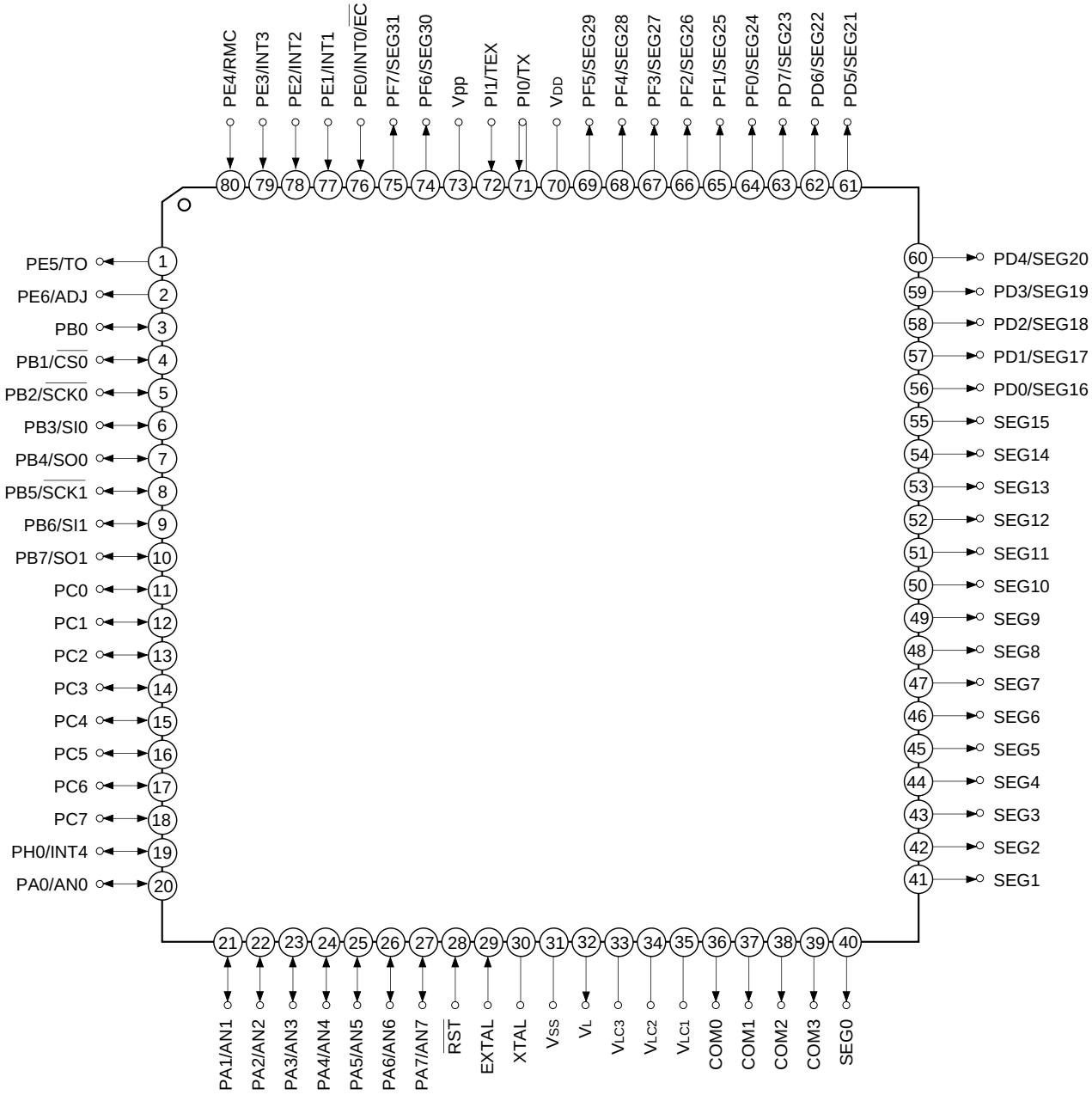
Note) Do not make any connections to Vpp (Pin 75).

Pin Assignment (Top View) CXP836P60 (LQFP package)



Note) Do not make any connections to Vpp (Pin 73).

Pin Assignment (Top View) CXP836P61 (QFP package)



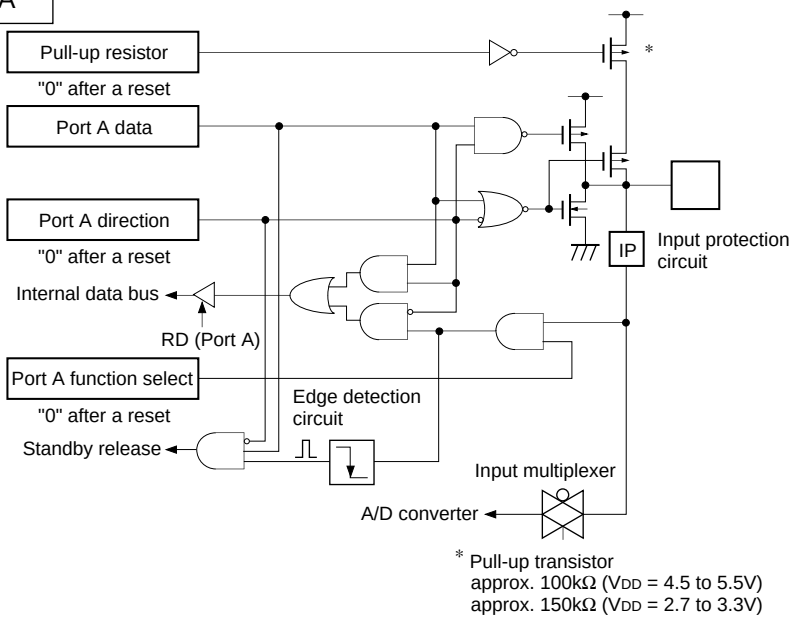
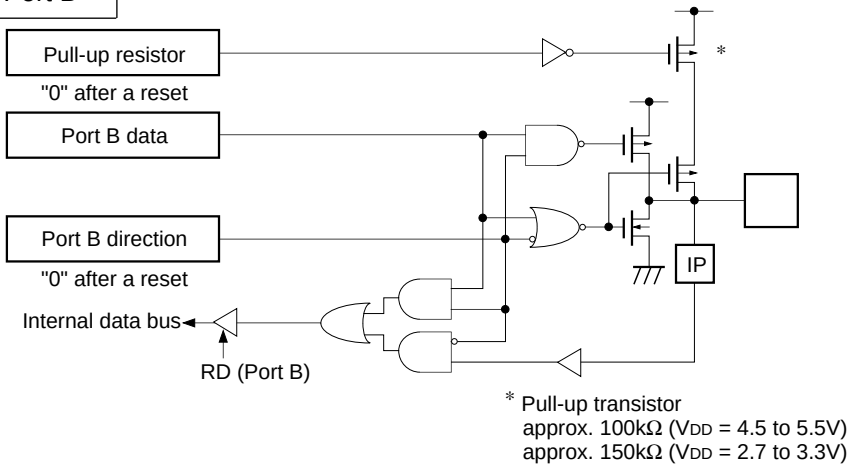
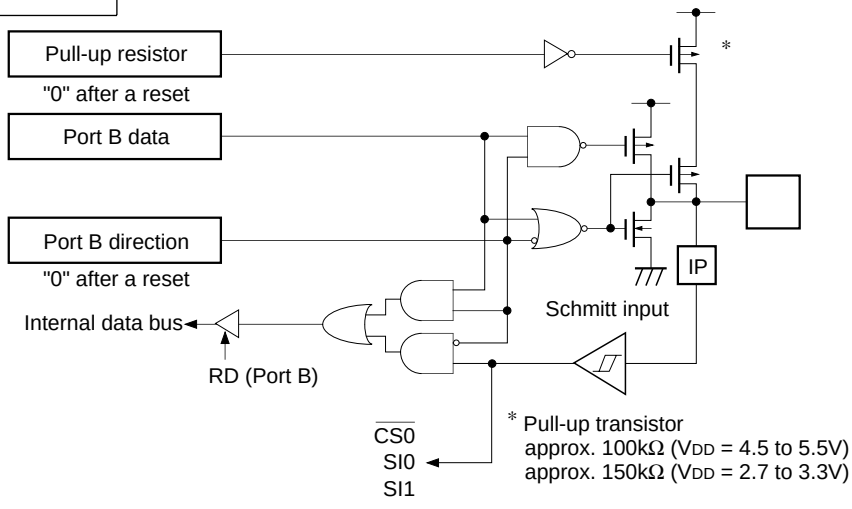
Note) Do not make any connections to Vpp (Pin 73).

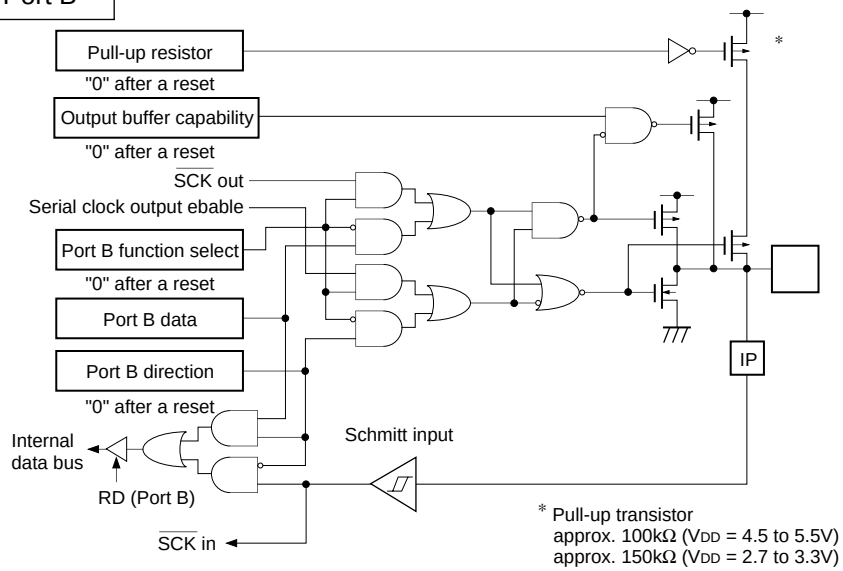
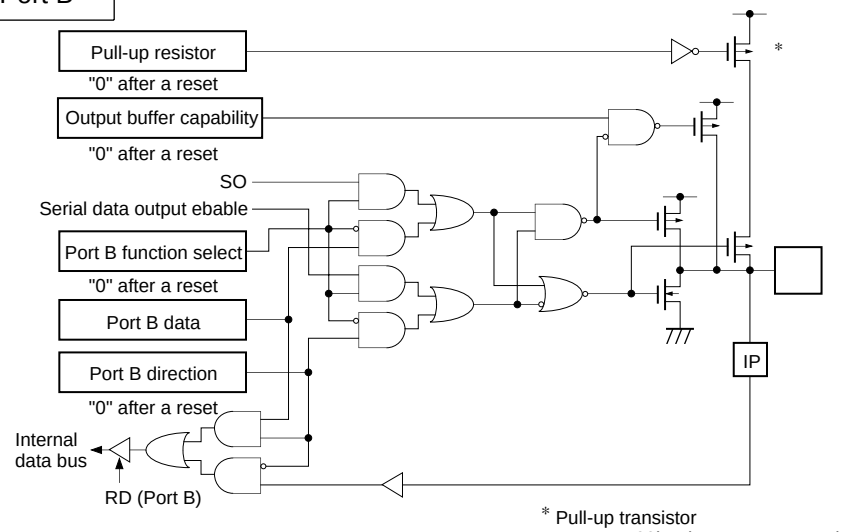
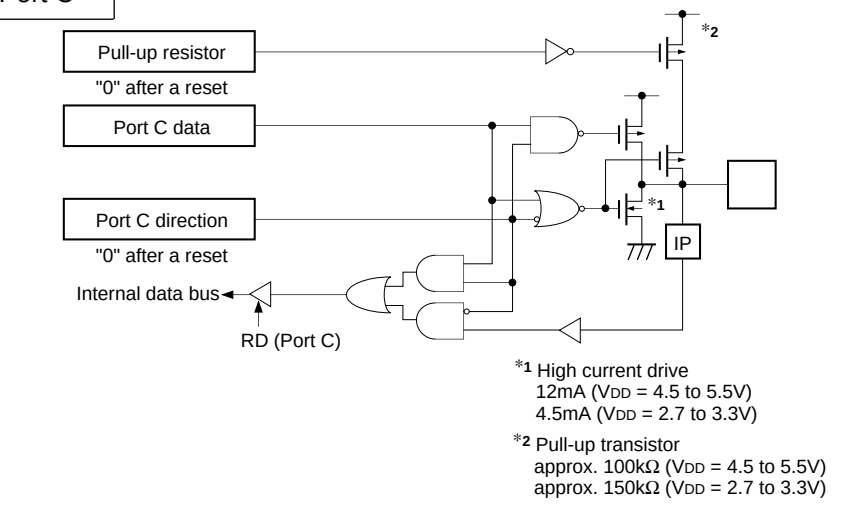
Pin Description

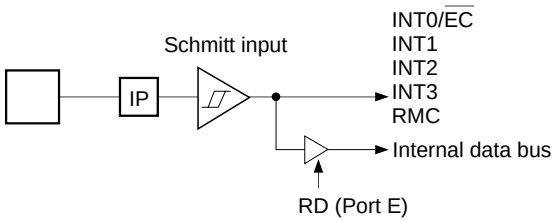
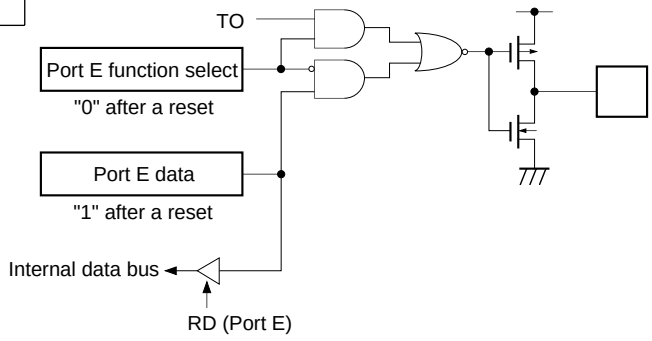
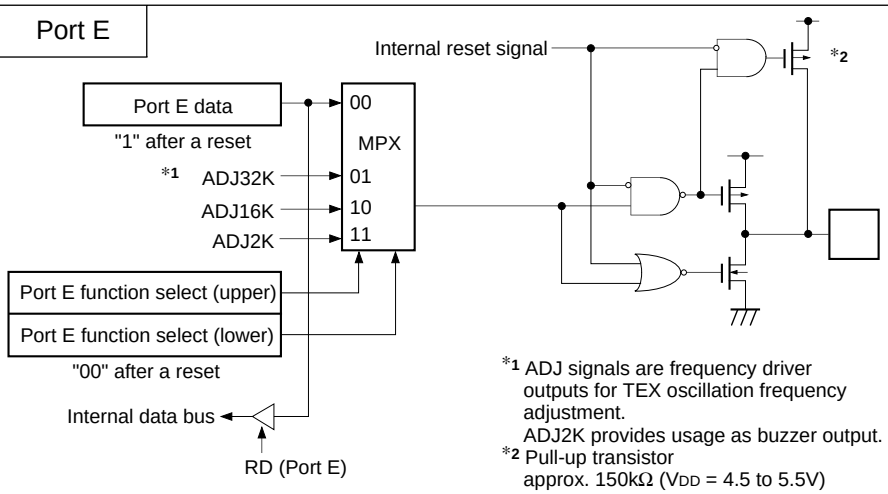
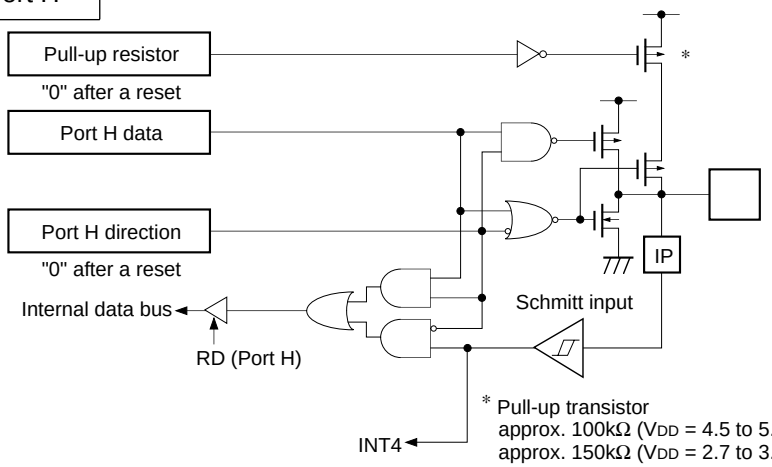
Symbol	I/O	Functions	
PA0/AN0 to PA7/AN7	I/O/Analog input	(Port A) 8-bit I/O port. I/O can be set in a bit unit. Standby release input can be set in a bit unit. Incorporation of pull-up resistor can be set through the program in a bit unit. (8 pins)	Analog inputs to A/D converter. (8 pins)
PB0	I/O	(Port B) 8-bit I/O port. I/O can be set in a bit unit. Incorporation of pull-up resistor can be set through the program in a bit unit. (8 pins)	
PB1/$\overline{CS0}$	I/O/Input		Chip select input for serial interface (CH0).
PB2/$\overline{SCK0}$	I/O/I/O		Serial clock I/O (CH0).
PB3/SI0	I/O/Input		Serial data input (CH0).
PB4/SO0	I/O/Output		Serial data output (CH0).
PB5/$\overline{SCK1}$	I/O/I/O		Serial clock I/O (CH1).
PB6/SI1	I/O/Input		Serial data input (CH1).
PB7/SO1	I/O/Output		Serial data output (CH1).
PC0 to PC7	I/O	(Port C) 8-bit I/O port. I/O can be set in a bit unit. Capable of driving 12mA sink current. Incorporation of pull-up resistor can be set through the program in a bit unit. (8 pins)	
PE0/INT0/$\overline{EC}$	Input/Input/Input	(Port E) 7-bit port. Lower 5 bits are for inputs; upper 2 bits are for outputs. (7 pins)	External event inputs for 8-bit timer/counter.
PE1/INT1	Input/Input		External interruption request inputs. (4 pins)
PE2/INT2	Input/Input		
PE3/INT3	Input/Input		
PE4/RMC	Input/Input		Remote control reception circuit input.
PE5/TO	Output/Output		Output for 8-bit timer/counter rectangular wave.
PE6/ADJ	Output/Output		Output for TEX oscillation frequency division.
PH0/INT4	I/O/Input	(Port H) 1-bit I/O port. Incorporation of pull-up resistor can be set through the program. (1 pin)	External interruption request input. (1 pin)
PI0/TX	Input	(Port I) 2-bit input port. (2 pins)	Crystal connectors for sub timer/counter clock oscillation. For usage as event counter, input to TEX, and leave TX open.
PI1/TEX	Input/Input		

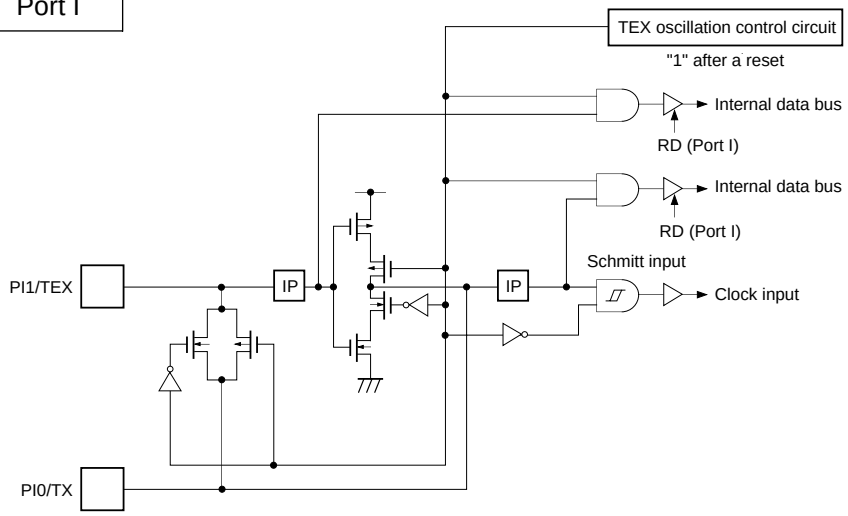
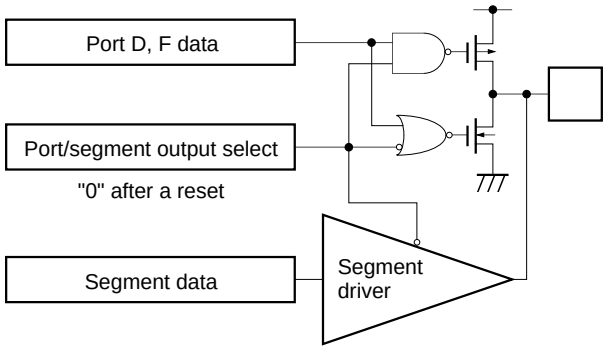
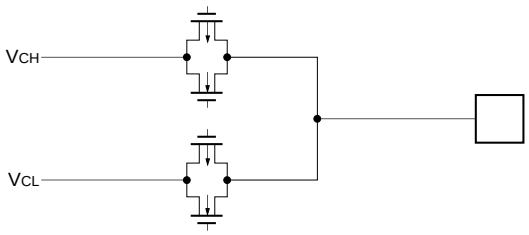
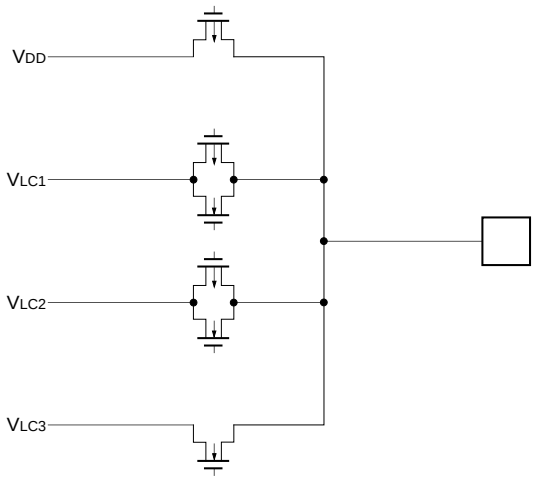
Symbol	I/O	Functions	
PD0/SEG16 to PD7/SEG23	Output/Output	(Port D) 8-bit output port. (8 pins)	LCD segment signal outputs. (16 pins)
PF0/SEG24 to PF7/SEG31	Output/Output	(Port F) 8-bit output port. (8 pins)	
SEG0 to SEG15	Output	LCD segment signal output. (16 pins)	
COM0 to COM3	Output	LCD common signal output. (4 pins)	
V_{LC1} to V_{LC3}		LCD bias power supply. (3 pins)	
V_L	Output	Control pin to cut off the current flowing to external LCD bias resistor during standby.	
EXTAL	Input	Crystal connectors for system clock oscillation. When the clock is supplied externally, input to EXTAL; opposite phase clock should be input to XTAL.	
XTAL			
$\overline{RST}$	Input	Low-level active system reset.	
Vpp		Positive power supply pin for writing of built-in PROM. Do not make any connections under normal operation.	
V_{DD}		Positive power supply.	
V_{SS}		GND.	

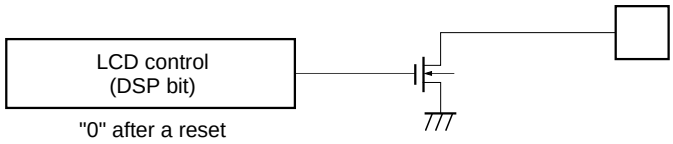
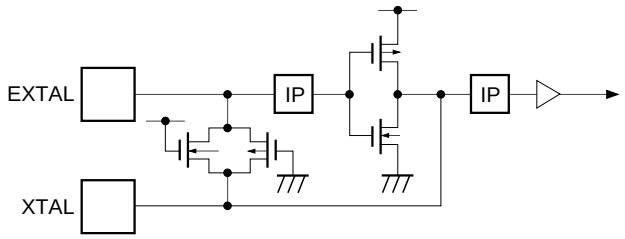
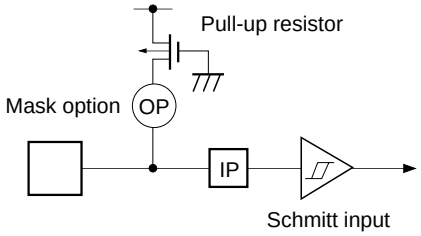
I/O Circuit Format for Pins

Pin	Circuit format	After a reset
PA0/AN0 to PA7/AN7 8 pins	Port A  	Hi-Z
PB0 1 pin	Port B  	Hi-Z
PB1/$\overline{CS0}$ PB3/SI0 PB6/SI1 3 pins	Port B  	Hi-Z

Pin	Circuit format	After a reset
PB2/$\overline{SCK0}$ PB5/$\overline{SCK1}$ 2 pins	Port B  * Pull-up transistor approx. 100kΩ (V_{DD} = 4.5 to 5.5V) approx. 150kΩ (V_{DD} = 2.7 to 3.3V)	Hi-Z
PB4/SO0 PB7/SO1 2 pins	Port B  * Pull-up transistor approx. 100kΩ (V_{DD} = 4.5 to 5.5V) approx. 150kΩ (V_{DD} = 2.7 to 3.3V)	Hi-Z
PC0 to PC7 8 pins	Port C  *1 High current drive 12mA (V_{DD} = 4.5 to 5.5V) 4.5mA (V_{DD} = 2.7 to 3.3V) *2 Pull-up transistor approx. 100kΩ (V_{DD} = 4.5 to 5.5V) approx. 150kΩ (V_{DD} = 2.7 to 3.3V)	Hi-Z

Pin	Circuit format	After a reset
PE0/INT0/$\overline{EC}$ PE1/INT1 PE2/INT2 PE3/INT3 PE4/RMC 5 pins	Port E 	Hi-Z
PE5/TO 1 pin	Port E 	High level
PE6/ADJ 1 pin	Port E  *1 ADJ signals are frequency driver outputs for TEX oscillation frequency adjustment. ADJ2K provides usage as buzzer output. *2 Pull-up transistor approx. 150kΩ (V_{DD} = 4.5 to 5.5V) approx. 200kΩ (V_{DD} = 2.7 to 3.3V)	High level (High level at ON resistance of pull-up transistor during a reset.)
PH0/INT4 1 pin	Port H  * Pull-up transistor approx. 100kΩ (V_{DD} = 4.5 to 5.5V) approx. 150kΩ (V_{DD} = 2.7 to 3.3V)	Hi-Z

Pin	Circuit format	After a reset
PI0/TX PI1/TEX 2 pins	Port I 	Oscillation halted port input
PD0/SEG16 to PD7/SEG23 PF0/SEG24 to PF7/SEG31 16 pins	Port D Port F 	Segment Output (V_{DD} level)
SEG0 to SEG15 16 pins	Segment 	V_{DD} level
COM0 to COM3 4 pins	Common 	V_{DD} level

Pin	Circuit format	After a reset
V_L 1 pin		Hi-Z
EXTAL XTAL 2 pins	 • Diagram shows circuit composition during oscillation. • Feedback resistor is removed during stop. XTAL becomes high level.	Oscillation
$\overline{RST}$ 1 pin		Low level (during a reset)

Absolute Maximum Ratings (Vss = 0V)

Item	Symbol	Rating	Unit	Remarks
Supply voltage	V_{DD}	–0.3 to +7.0	V	
	Vpp	–0.3 to +13.0	V	PROM incorporated version fixed
LCD bias voltage	V_{LC1}, V_{LC2}, V_{LC3}	–0.3 to +7.0*1	V	
Input voltage	V_{IN}	–0.3 to +7.0*1	V	
Output voltage	V_{OUT}	–0.3 to +7.0*1	V	
High level output current	I_{OH}	–5	mA	Output per pin
High level total output current	ΣI_{OH}	–50	mA	Total for all output pins
Low level output current	I_{OL}	15	mA	Value per pin, excluding high current output pins
	I_{OLC}	20	mA	Value per pin for high current output pins*2
Low level total output current	ΣI_{OL}	100	mA	Total for all output pins
Operating temperature	Topr	–20 to +75	°C	
Storage temperature	Tstg	–55 to +150	°C	
Allowable power dissipation	P_D	600	mW	QFP-80P-L01
		380	mW	LQFP-80P-L01
		380	mW	QFP-80P-L03

*1 V_{IN} and V_{OUT} must not exceed V_{DD} + 0.3V.

*2 The high current drive transistor is the N-ch transistor of Port C (PC).

Note) Usage exceeding absolute maximum ratings may permanently impair the LSI. Normal operation should be conducted under the recommended operating conditions. Exceeding these conditions may adversely affect the reliability of the LSI.

Recommended Operating Conditions (Vss = 0V)

Item	Symbol	Min.	Max.	Unit	Remarks	
Supply voltage	V_{DD}	4.5	5.5	V	fc = 10MHz or less	Guaranteed operation range during 1/2 and 1/4 frequency dividing mode
		2.7	5.5		fc = 4MHz or less	
		2.7	5.5		Guaranteed operation range during 1/16 frequency dividing mode or sleep mode	
		2.7	5.5		Guaranteed operation range with TEX clock	
		2.5	5.5		Guaranteed data hold range during stop	
LCD bias voltage	V_{LC1}	Vss	V_{DD}	V	LCD power supply range*4	
	V_{LC2}					
	V_{LC3}					
High level input voltage	V_{IH}	0.7V_{DD}	V_{DD}	V	*1	
	V_{IHS}	0.8V_{DD}	V_{DD}	V	Hysteresis input*2	
	V_{IHEX}	V_{DD} – 0.4	V_{DD} + 0.3	V	EXTAL*3, TEX*5	
Low level input voltage	V_{IL}	0	0.3V_{DD}	V	*1	
	V_{ILS}	0	0.2V_{DD}	V	Hysteresis input*2	
	V_{ILEX}	–0.3	0.4	V	EXTAL*3, TEX*5	
Operating temperature	Topr	–20	+75	°C		

*1 Value for each pin of normal input ports (PA, PB0, PB4, PB7, PC and PI).

*2 Value of the following pins; $\overline{RST}$, $\overline{CS0}$, SI0, SI1, $\overline{SCK0}$, $\overline{SCK1}$, $\overline{EC}$/INT0, INT1, INT2, INT3, INT4 and RMC.

*3 Specifies only during external clock input.

*4 Optimal values are determined by LCD used.

*5 Specifies only during external event count input.

Electrical Characteristics

DC Characteristics (V_{DD} = 4.5 to 5.5V) (Ta = –20 to +75°C, Vss = 0V)

Item	Symbol	Pins	Conditions	Min.	Typ.	Max.	Unit
High level output voltage	V_{OH}	$\overline{SCK0}$*1, SO0*1	V_{DD} = 4.5V, I_{OH} = –1.0mA	4.0			V
		$\overline{SCK1}$*1, SO1*1	V_{DD} = 4.5V, I_{OH} = –2.4mA	3.5			V
		PA, PB, PC, PD*2, PE5, PE6, PF*2, PH0, V_L (V_{OL} only)	V_{DD} = 4.5V, I_{OH} = –0.5mA	4.0			V
			V_{DD} = 4.5V, I_{OH} = –1.2mA	3.5			V
Low level output voltage	V_{OL}		V_{DD} = 4.5V, I_{OL} = 1.8mA			0.4	V
			V_{DD} = 4.5V, I_{OL} = 3.6mA			0.6	V
		PC	V_{DD} = 4.5V, I_{OL} = 12.0mA			1.5	V
Input current	I_{IHE}	EXTAL	V_{DD} = 5.5V, V_{IH} = 5.5V	0.5		40	V
	I_{ILE}		V_{DD} = 5.5V, V_{IL} = 0.4V	–0.5		–40	µA
	I_{IHT}	TEX	V_{DD} = 5.5V, V_{IH} = 5.5V	0.1		10	µA
	I_{ILT}		V_{DD} = 5.5V V_{IL} = 0.4V	–0.1		–10	µA
	I_{ILR}	$\overline{RST}$*3		–1.5		–400	µA
	I_{IL}	PA to PC*4, PE0 to PE4, $\overline{PH}$*4, PI, $\overline{RST}$*3				–45	µA
	I_{IH}		V_{DD} = 4.5V, V_{IH} = 4.0V	–2.78			µA
I/O leakage current	I_{IZ}		V_{DD} = 5.5V V_I = 0, 5.5V			±10	µA
Common output impedance	R_{COM}	COM0 to COM3	V_{DD} = 5V V_{LC1} = 3.75V V_{LC2} = 2.5V V_{LC3} = 1.25V		3	5	kΩ
Segment output impedance	R_{SEG}	SEG0 to SEG15, SEG16 to SEG31*2			5	15	kΩ
Supply current*5	I_{DD1}	V_{DD}	High-speed mode operation (1/2 frequency dividing clock) V_{DD} = 5.5V, 10MHz crystal oscillation (C_1 = C_2 = 15pF)		14	45	mA
	I_{DDS1}		Sleep mode V_{DD} = 5.5V, 10MHz crystal oscillation (C_1 = C_2 = 15pF)		2.8	9	mA
	I_{DDS3}		Stop mode V_{DD} = 5.5V, 10MHz and termination of TEX oscillation			10	µA

Item	Symbol	Pins	Conditions	Min.	Typ.	Max.	Unit
Input capacity	C_{IN}	PA to PC, PE0 to PE4, PH, PI, EXTAL, $\overline{RST}$	Clock 1MHz 0V for all pins excluding measured pins		10	20	pF

*1 Specifies when Port B output buffer capability switching register (BUFB: 01F4h) selects the buffer capability to high.

*2 Common pins of PD0/SEG16 to PD7/SEG23, PF0/SEG24 to PF7/SEG31, PD and PF is the case when the common pin is selected as port; SEG16 to SEG31 is when the common pin is selected as segment output.

*3 $\overline{RST}$ specifies the input current when pull-up resistor has been selected; leakage current when no resistor has been selected.

*4 Pins PA to PC, and PH0 specifies the input current when pull-up resistor has been selected; leakage current when no resistor has been selected.

*5 When all output pins are left open.

Electrical Characteristics

DC Characteristics (V_{DD} = 2.7 to 3.3V) (Ta = –20 to +75°C, Vss = 0V)

Item	Symbol	Pins	Conditions	Min.	Typ.	Max.	Unit
High level output voltage	V_{OH}	$\overline{SCK0}$*1, SO0*1	V_{DD} = 2.7V, I_{OH} = –0.24mA	2.5			V
		$\overline{SCK1}$*1, SO1*1	V_{DD} = 2.7V, I_{OH} = –0.9mA	2.1			V
		PA, PB, PC, PD*2, PE5, PE6, PF*2, PH0, V_L (V_{OL} only)	V_{DD} = 2.7V, I_{OH} = –0.12mA	2.5			V
			V_{DD} = 2.7V, I_{OH} = –0.45mA	2.1			V
Low level output voltage	V_{OL}		V_{DD} = 2.7V, I_{OL} = 1.0mA			0.25	V
			V_{DD} = 2.7V, I_{OL} = 1.4mA			0.4	V
		PC	V_{DD} = 2.7V, I_{OL} = 4.5mA			0.9	V
Input current	I_{IHE}	EXTAL	V_{DD} = 3.3V, V_{IH} = 3.3V	0.3		20	V
	I_{ILE}		V_{DD} = 3.3V, V_{IL} = 0.3V	–0.3		–20	µA
	I_{IHT}	TEX	V_{DD} = 3.3V, V_{IH} = 3.3V	0.1		10	µA
	I_{ILT}		V_{DD} = 3.3V V_{IL} = 0.3V	–0.1		–10	µA
	I_{ILR}	$\overline{RST}$*3		–0.9		–200	µA
	I_{IL}	PA to PC*4, PE0 to PE4, $\overline{PH}$*4, PI, $\overline{RST}$*3				–20	µA
	I_{IH}		V_{DD} = 2.7V, V_{IH} = 2.4V	0.9			µA
I/O leakage current	I_{IZ}		V_{DD} = 3.3V V_I = 0, 3.3V			±10	µA
Common output impedance	R_{COM}	COM0 to COM3	V_{DD} = 3V V_{LC1} = 2.25V V_{LC2} = 1.5V V_{LC3} = 0.75V		4.5	7.5	kΩ
Segment output impedance	R_{SEG}	SEG0 to SEG15, SEG16 to SEG31*2			10	30	kΩ
Supply current*5	I_{DD1}	V_{DD}	High-speed mode operation (1/2 frequency dividing clock) V_{DD} = 3.3V, 4MHz crystal oscillation (C_1 = C_2 = 15pF)		3	9	mA
	I_{DD2}		V_{DD} = 3.3V, TEX*6 crystal oscillation (C_1 = C_2 = 47pF)		34	100	µA
	I_{DDS1}		Sleep mode V_{DD} = 3.3V, 4MHz crystal oscillation (C_1 = C_2 = 15pF)		0.65	2.5	mA
	I_{DDS2}		V_{DD} = 3.3V, TEX*6 crystal oscillation (C_1 = C_2 = 47pF)		16	30	µA
	I_{DDS3}		Stop mode V_{DD} = 3.3V, 4MHz and termination of TEX oscillation			10	µA

Item	Symbol	Pins	Conditions	Min.	Typ.	Max.	Unit
Input capacity	C_{IN}	PA to PC, PE0 to PE4, PH, PI, EXTAL, $\overline{RST}$	Clock 1MHz 0V for all pins excluding measured pins		10	20	pF

*1 Specifies when Port B output buffer capability switching register (BUFB: 01F4h) selects the buffer capability to high.

*2 Common pins of PD0/SEG16 to PD7/SEG23, PF0/SEG24 to PF7/SEG31, PD and PF is the case when the common pin is selected as port; SEG16 to SEG31 is when the common pin is selected as segment output.

*3 $\overline{RST}$ specifies the input current when pull-up resistor has been selected; leakage current when no resistor has been selected.

*4 Pins PA to PC, and PH0 specifies the input current when pull-up resistor has been selected; leakage current when no resistor has been selected.

*5 When all output pins are left open.

*6 The value when 32.768kHz oscillator is connected to TEX.

AC Characteristics

(1) Clock timing

(Ta = –20 to +75°C, V_{DD} = 2.7 to 5.5V, Vss = 0V)

Item	Symbol	Pin	Conditions	Min.	Typ.	Max.	Unit
System clock frequency	f_C	XTAL EXTAL	Fig. 1, Fig. 2 V_{DD} = 4.5 to 5.5V	1		10	MHz
				1		5	
System clock input pulse width	t_{XL}, t_{XH}	EXTAL	Fig. 1, Fig. 2 external clock drive V_{DD} = 4.5 to 5.5V	37.5			ns
				77.5			
System clock input rise and fall time	t_{CR}, t_{CF}	EXTAL	Fig. 1, Fig. 2 external clock drive			200	ns
Event count input clock pulse width	t_{EH}, t_{EL}	$\overline{EC}$	Fig. 3	tsys + 50*1			ns
Event count input clock rise and fall time	t_{ER}, t_{EF}	$\overline{EC}$	Fig. 3			20	ms
System clock frequency	f_C	TEX TX	V_{DD} = 2.7 to 5.5V Fig. 2 (32kHz clock applied condition)		32.768		kHz
Event count input clock input pulse width	t_{TL}, t_{TH}	TEX	Fig. 3	10			µs
Event count input clock rise and fall time	t_{TR}, t_{TF}	TEX	Fig. 3			20	ms

*1 tsys indicates the three values below according to the upper two bits (CPU clock selection) of the clock control register (CLC: 00FEh).
tsys [ns] = 2000/fc (upper two bits = “00”), 4000/fc (upper two bits = “01”), 16000/fc (upper two bits = “11”).

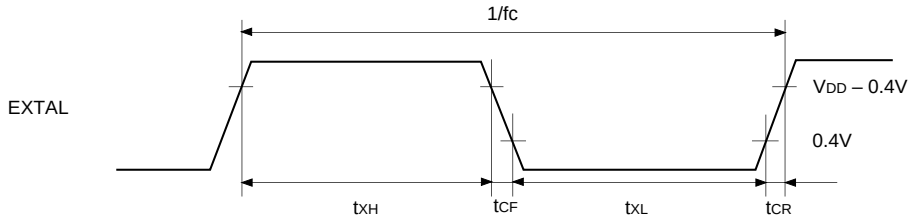


Fig. 1. Clock timing

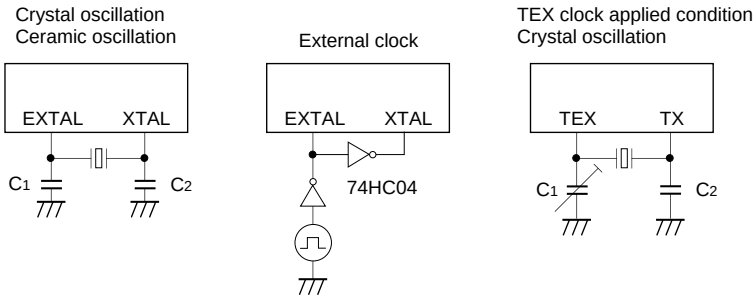


Fig. 2. Clock applied conditions

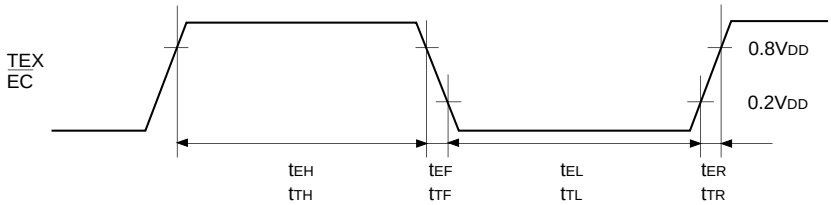


Fig. 3. Event count clock timing

(2) Serial transfer (CH0) (Ta = –20 to +75°C, V_{DD} = 4.5 to 5.5V, Vss = 0V)

Item	Symbol	Pin	Conditions	Min.	Max.	Unit
$\overline{CS}\downarrow\rightarrow\overline{SCK}$ delay time	t_{DCSK}	$\overline{SCK0}$	Chip select transfer mode ($\overline{SCK}$ = output mode)		tsys + 200	ns
$\overline{CS}\uparrow\rightarrow\overline{SCK}$ float delay time	t_{DCSKF}	$\overline{SCK0}$	Chip select transfer mode ($\overline{SCK}$ = output mode)		tsys + 200	ns
$\overline{CS}\downarrow\rightarrow$ SO delay time	t_{DCSO}	SO0	Chip select transfer mode		tsys + 200	ns
$\overline{CS}\downarrow\rightarrow$ SO float delay time	t_{DCSOF}	SO0	Chip select transfer mode		tsys + 200	ns
$\overline{CS}$ high level width	t_{WHCS}	$\overline{CS0}$	Chip select transfer mode	tsys + 200		ns
$\overline{SCK}$ cycle time	t_{KCY}	$\overline{SCK0}$	Input mode	2tsys + 200		ns
			Output mode	16000/fc		ns
$\overline{SCK}$ high and low level widths	t_{KH} t_{KL}	$\overline{SCK0}$	Input mode	tsys + 100		ns
			Output mode	8000/fc – 100		ns
SI input setup time (for $\overline{SCK}\uparrow$)	t_{SIK}	SI0	$\overline{SCK}$ input mode	–tsys + 100		ns
			$\overline{SCK}$ output mode	200		ns
SI input hold time (for $\overline{SCK}\uparrow$)	t_{KSI}	SI0	$\overline{SCK}$ input mode	2tsys + 100		ns
			$\overline{SCK}$ output mode	100		ns
$\overline{SCK}\downarrow\rightarrow$ SO delay time	t_{KSO}	SO0	$\overline{SCK}$ input mode		2tsys + 200	ns
			$\overline{SCK}$ output mode		100	ns

Note 1) tsys indicates the three values below according to the upper two bits (CPU clock selection) of the clock control register (CLC: 00FEh).
tsys [ns] = 2000/fc (upper two bits = “00”), 4000/fc (upper two bits = “01”), 16000/fc (upper two bits = “11”)

Note 2) $\overline{CS}$, $\overline{SCK}$, SI and SO indicates $\overline{CS0}$, $\overline{SCK0}$, SI0 and SO0, respectively.

Note 3) The load condition for the $\overline{SCK}$ output mode, SO output delay time is 50pF + 1TTL.

Note 4) The value when Port B output buffer capability switching register (BUFB: 01F4h) selects buffer capability to normal.

Serial transfer (CH0) (Ta = –20 to +75°C, V_{DD} = 2.7 to 3.3V, Vss = 0V)

Item	Symbol	Pin	Conditions	Min.	Max.	Unit
$\overline{CS} \downarrow \rightarrow \overline{SCK}$ delay time	t_{DCSK}	$\overline{SCK0}$	Chip select transfer mode ($\overline{SCK}$ = output mode)		tsys + 250	ns
$\overline{CS} \uparrow \rightarrow \overline{SCK}$ float delay time	t_{DCSKF}	$\overline{SCK0}$	Chip select transfer mode ($\overline{SCK}$ = output mode)		tsys + 200	ns
$\overline{CS} \downarrow \rightarrow$ SO delay time	t_{DCSO}	SO0	Chip select transfer mode		tsys + 250	ns
$\overline{CS} \downarrow \rightarrow$ SO float delay time	t_{DCSOF}	SO0	Chip select transfer mode		tsys + 200	ns
$\overline{CS}$ high level width	t_{WHCS}	$\overline{CS0}$	Chip select transfer mode	tsys + 200		ns
$\overline{SCK}$ cycle time	t_{KCY}	$\overline{SCK0}$	Input mode	2tsys + 200		ns
			Output mode	16000/fc		ns
$\overline{SCK}$ high and low level widths	t_{KH} t_{KL}	$\overline{SCK0}$	Input mode	tsys + 100		ns
			Output mode	8000/fc – 150		ns
SI input setup time (for $\overline{SCK} \uparrow$)	t_{SIK}	SI0	$\overline{SCK}$ input mode	–tsys + 100		ns
			$\overline{SCK}$ output mode	200		ns
SI input hold time (for $\overline{SCK} \uparrow$)	t_{KSI}	SI0	$\overline{SCK}$ input mode	2tsys + 100		ns
			$\overline{SCK}$ output mode	100		ns
$\overline{SCK} \downarrow \rightarrow$ SO delay time	t_{KSO}	SO0	$\overline{SCK}$ input mode		2tsys + 250	ns
			$\overline{SCK}$ output mode		125	ns

Note 1) tsys indicates the three values below according to the upper two bits (CPU clock selection) of the clock control register (CLC: 00FEh).
tsys [ns] = 2000/fc (upper two bits = “00”), 4000/fc (upper two bits = “01”), 16000/fc (upper two bits = “11”)

Note 2) $\overline{CS}$, $\overline{SCK}$, SI and SO indicates $\overline{CS0}$, $\overline{SCK0}$, SI0 and SO0, respectively.

Note 3) The load condition for the $\overline{SCK}$ output mode, SO output delay time is 50pF.

Note 4) The value when Port B output buffer capability switching register (BUFB: 01F4h) selects buffer capability to high.

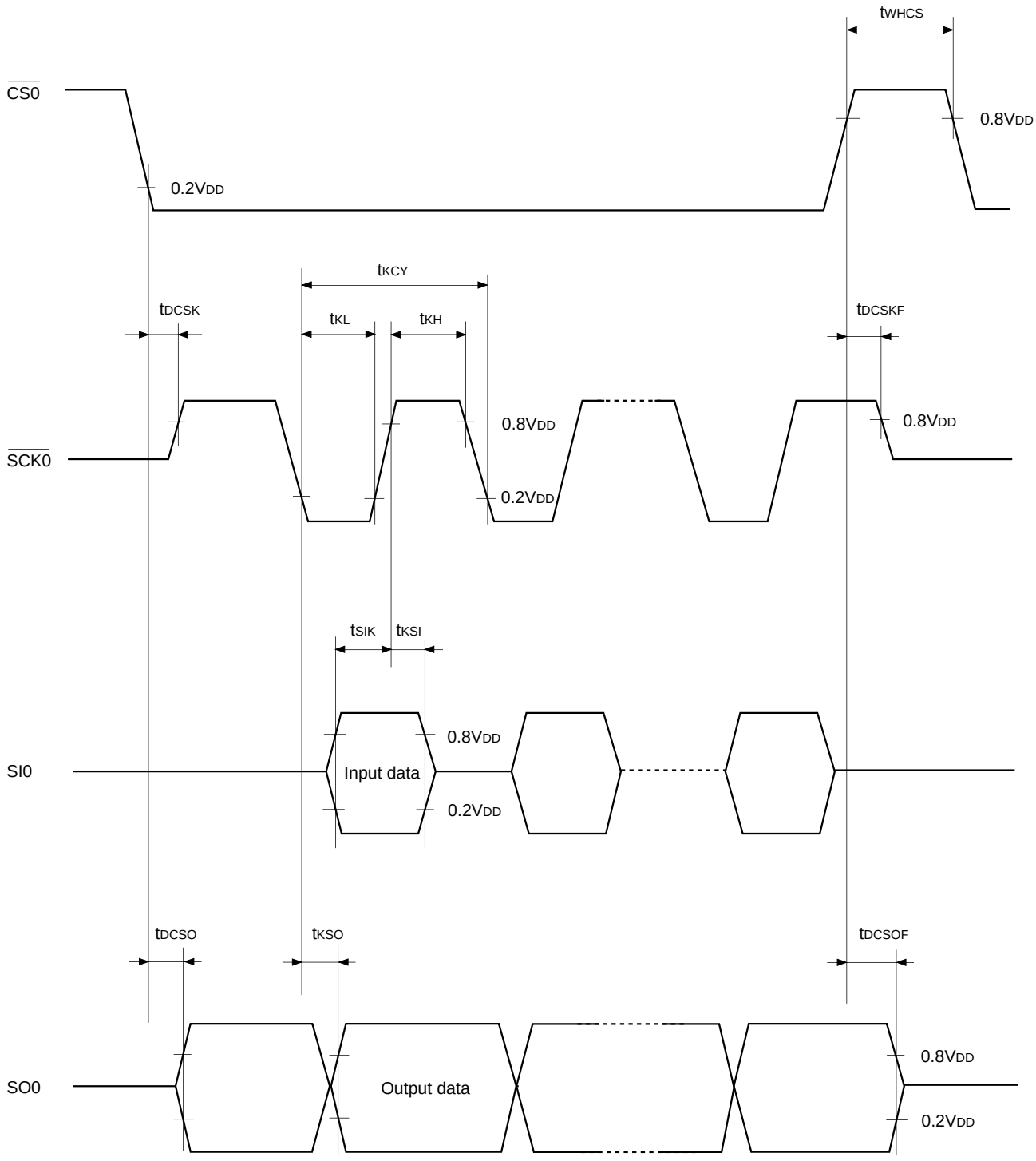


Fig. 4. Serial transfer CH0 timing

Serial Transfer (CH1) (Ta = –20 to +75°C, V_{DD} = 4.5 to 5.5V, Vss = 0V)

Item	Symbol	Pin	Conditions	Min.	Max.	Unit
$\overline{SCK}$ cycle time	t_{KCY}	$\overline{SCK1}$	Input mode	1000		ns
			Output mode	8000/fc		ns
$\overline{SCK}$ high and low level widths	t_{KH} t_{KL}	$\overline{SCK1}$	Input mode	400		ns
			Output mode	4000/fc – 50		ns
SI input setup time (for $\overline{SCK}$ ↑)	t_{SIK}	SI1	$\overline{SCK}$ input mode	100		ns
			$\overline{SCK}$ output mode	200		ns
SI input hold time (for $\overline{SCK}$ ↑)	t_{KSI}	SI1	$\overline{SCK}$ input mode	200		ns
			$\overline{SCK}$ output mode	100		ns
$\overline{SCK}$ ↓ → SO delay time	t_{KSO}	SO1	$\overline{SCK}$ input mode		200	ns
			$\overline{SCK}$ output mode		100	ns

Note 1) tsys indicates the three values below according to the upper two bits (CPU clock selection) of the clock control register (CLC: 00FEh).
tsys [ns] = 2000/fc (upper two bits = "00"), 4000/fc (upper two bits = "01"), 16000/fc (upper two bits = "11")

Note 2) $\overline{SCK}$, SI and SO indicates $\overline{SCK1}$, SI1 and SO1, respectively.

Note 3) The load condition for the $\overline{SCK1}$ output mode, SO1 output delay time is 50pF + 1TTL.

Note 4) The value when Port B output buffer capability switching register (BUFB: 01F4h) selects buffer capability to normal.

Serial Transfer (CH1) (Ta = –20 to +75°C, V_{DD} = 2.7 to 3.3V, Vss = 0V)

Item	Symbol	Pin	Conditions	Min.	Max.	Unit
$\overline{SCK}$ cycle time	t_{KCY}	$\overline{SCK1}$	Input mode	1000		ns
			Output mode	8000/fc		ns
$\overline{SCK}$ high and low level widths	t_{KH} t_{KL}	$\overline{SCK1}$	Input mode	400		ns
			Output mode	4000/fc – 100		ns
SI input setup time (for $\overline{SCK}$ ↑)	t_{SIK}	SI1	$\overline{SCK}$ input mode	100		ns
			$\overline{SCK}$ output mode	200		ns
SI input hold time (for $\overline{SCK}$ ↑)	t_{KSI}	SI1	$\overline{SCK}$ input mode	200		ns
			$\overline{SCK}$ output mode	100		ns
$\overline{SCK}$ ↓ → SO delay time	t_{KSO}	SO1	$\overline{SCK}$ input mode		250	ns
			$\overline{SCK}$ output mode		125	ns

Note 1) tsys indicates the three values below according to the upper two bits (CPU clock selection) of the clock control register (CLC: 00FEh).
tsys [ns] = 2000/fc (upper two bits = "00"), 4000/fc (upper two bits = "01"), 16000/fc (upper two bits = "11")

Note 2) $\overline{SCK}$, SI and SO indicates $\overline{SCK1}$, SI1 and SO1, respectively.

Note 3) The load condition for the $\overline{SCK1}$ output mode, SO1 output delay time is 50pF.

Note 4) The value when Port B output buffer capability switching register (BUFB: 01F4h) selects buffer capability to high.

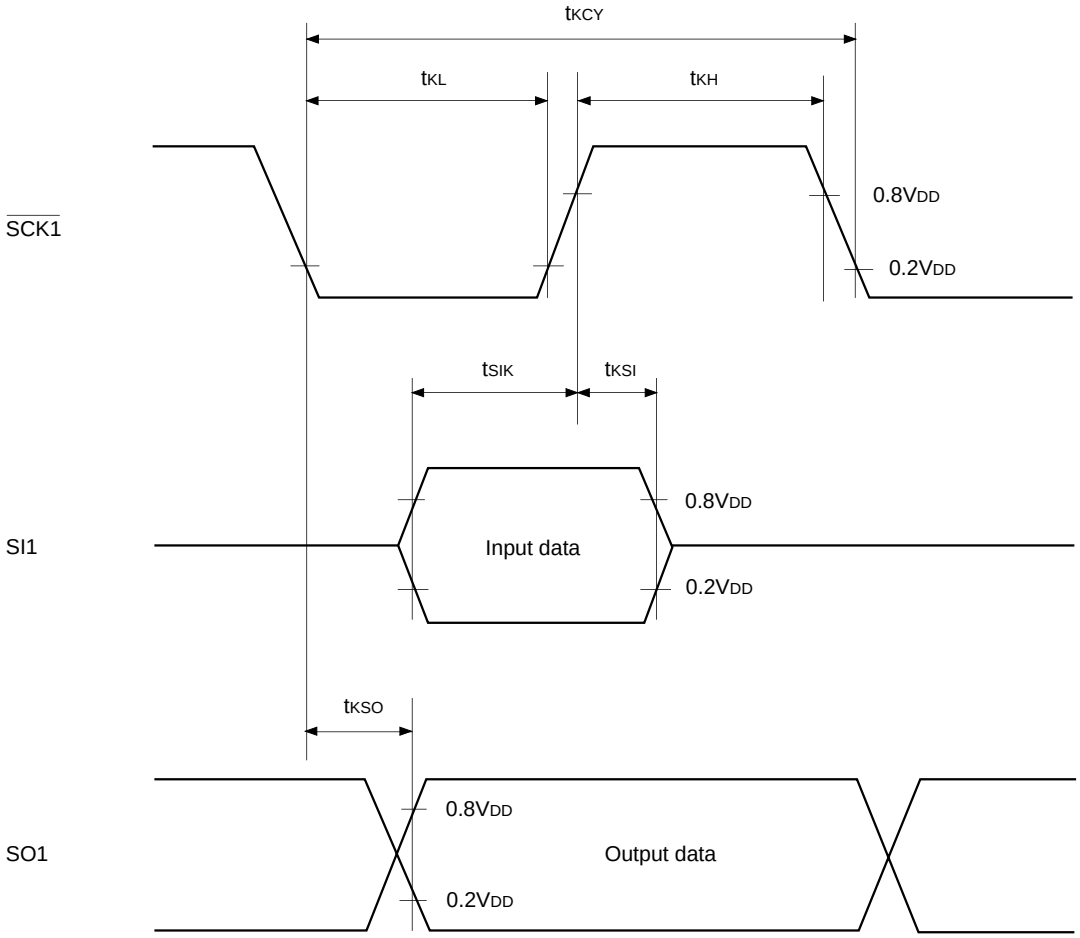


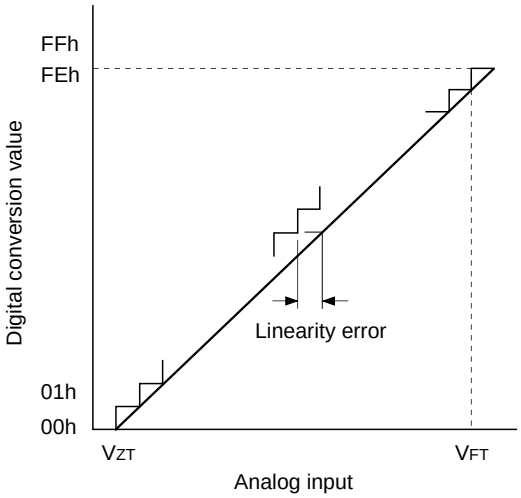
Fig. 5. Serial transfer CH1 timing

(3) A/D converter characteristics (Ta = –20 to +75°C, V_{DD} = 4.5 to 5.5V, Vss = 0V)

Item	Symbol	Pin	Conditions	Min.	Typ.	Max.	Unit
Resolution						8	Bits
Linearity error			Ta = 25°C V_{DD} = 5.0V V_{SS} = 0V			±3	LSB
Zero transition voltage	V_{ZT}*1			–10	10	70	mV
Full-scale transition voltage	V_{FT}*2			4910	4970	5030	mV
Conversion time	t_{CONV}			31/f_{ADC}*3			µs
Sampling time	t_{SAMP}			10/f_{ADC}*3			µs
Analog input voltage	V_{IAN}	AN0 to AN7		0		V_{DD}	V

(Ta = –20 to +75°C, V_{DD} = 2.7 to 3.3V, Vss = 0V)

Item	Symbol	Pin	Conditions	Min.	Typ.	Max.	Unit
Resolution						8	Bits
Linearity error			Ta = 25°C V_{DD} = 2.7V V_{SS} = 0V			±3	LSB
Zero transition voltage	V_{ZT}*1			–10	11	40	mV
Full-scale transition voltage	V_{FT}*2			2651	2688	2716	mV
Conversion time	t_{CONV}			31/f_{ADC}*3			µs
Sampling time	t_{SAMP}			10/f_{ADC}*3			µs
Analog input voltage	V_{IAN}	AN0 to AN7		0		V_{DD}	V



*1 V_{ZT}: Value at which the digital conversion value changes from 00h to 01h and vice versa.

*2 V_{FT}: Value at which the digital conversion value changes from FEh to FFh and vice versa.

*3 f_{ADC} = fc/4

Fig. 6. Definition of A/D converter terms

(4) Interruption, reset input (Ta = –20 to +75°C, V_{DD} = 2.7 to 5.5V, Vss = 0V)

Item	Symbol	Pin	Conditions	Min.	Max.	Unit
External interruption high and low level widths	t_{IH} t_{IL}	INT0 INT1 INT2 INT3 INT4		1		µs
Reset input low level width	t_{RSL}	$\overline{RST}$		32/fc		µs

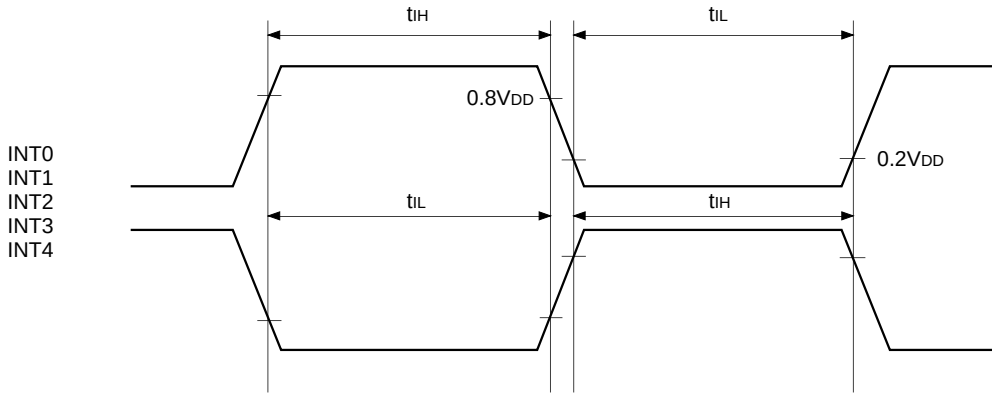


Fig. 7. Interruption input timing

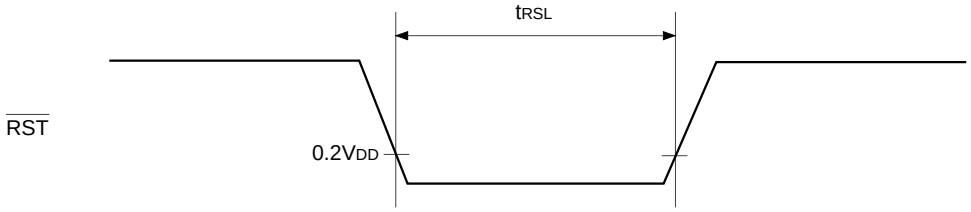


Fig. 8. $\overline{RST}$ input timing

Appendix

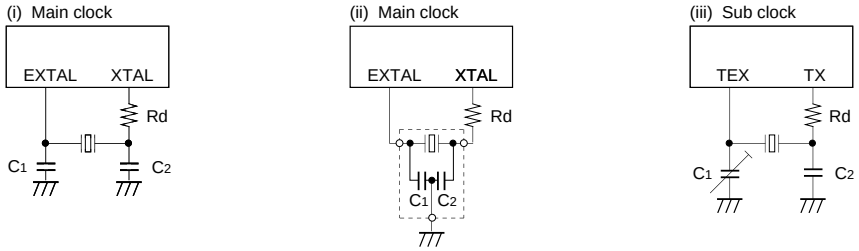


Fig. 9. SPC700 series recommended oscillation circuit

Manufacturer	Model	fc (MHz)	C_1 (pF)	C_2 (pF)	Rd (Ω)	Circuit example	Remarks
MURATA MFG CO., LTD.	CSA4.19MG	4.19	100	100	0	(i)	
	CSA8.00MG	8.00	30	30	0		
	CSA10.0MT	10.00	30	30	0		
	CST4.19MGW*1	4.19	100	100	0	(ii)	
	CST8.00MTW*1	8.00	30	30	0		
	CST10.00MTW*1	10.00	30	30	0		
RIVER ELETEC CO., LTD.	HC-49/U03	4.19	22	22	1.0k	(i)	
		8.00	15	15	100		
		10.00	10	10	100		
KINSEKI LTD.	CX-5F	4.19	33	33	2.2k		CL = 12.0pF
		8.00	18	18	0		CL = 12.0pF
		10.00	15	15	0		CL = 12.0pF
TDK Corporation	FCR4.19MC5*1	4.19	30 (± 20%)	30 (± 20%)	0	(ii)	
	FCR8.0MC5*1	8.00	20 (± 20%)	20 (± 20%)			
	FCR10.0MC5*1	10.00	20 (± 20%)	20 (± 20%)			
	CCR4.19MC3*1	4.19	36 (± 20%)	36 (± 20%)			
	CCR8.0MC5*1	8.00	20 (± 20%)	20 (± 20%)			
	CCR10.0MC5*1	10.00	20 (± 20%)	20 (± 20%)			
Seiko Instruments Inc.	VTC-200 SP-T	32.768	18	18	330k	(iii)	CL = 12.5pF
		75.00	4	4	100k		CL = 6.0pF

*1 Those marked with an *1 signify types with built-in ground capacitance (C_1, C_2).

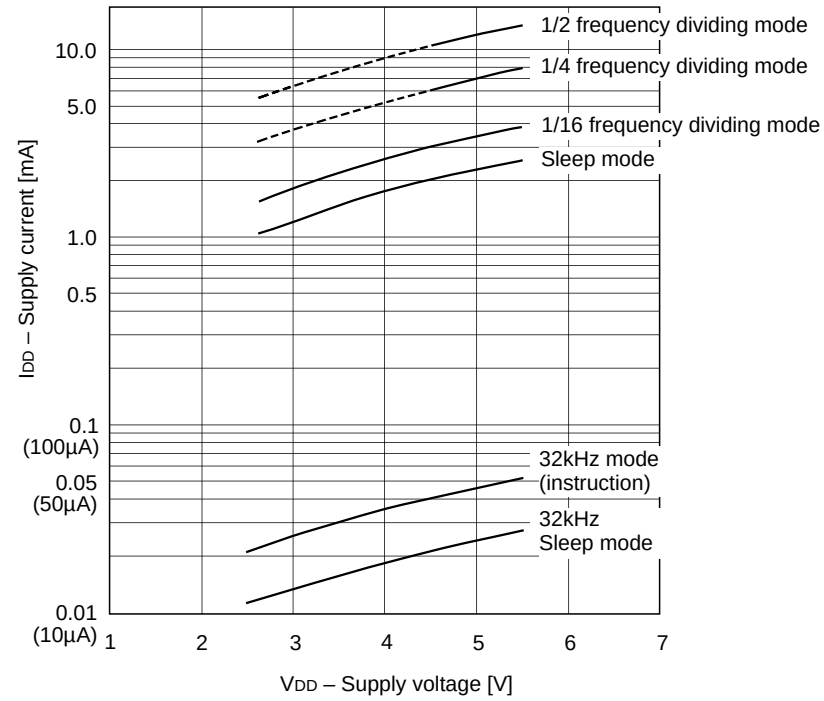
FCR***: Lead-type ceramic oscillator
CCR***: Surface mounted-type ceramic oscillator
CL : Load Capacitor

Product List

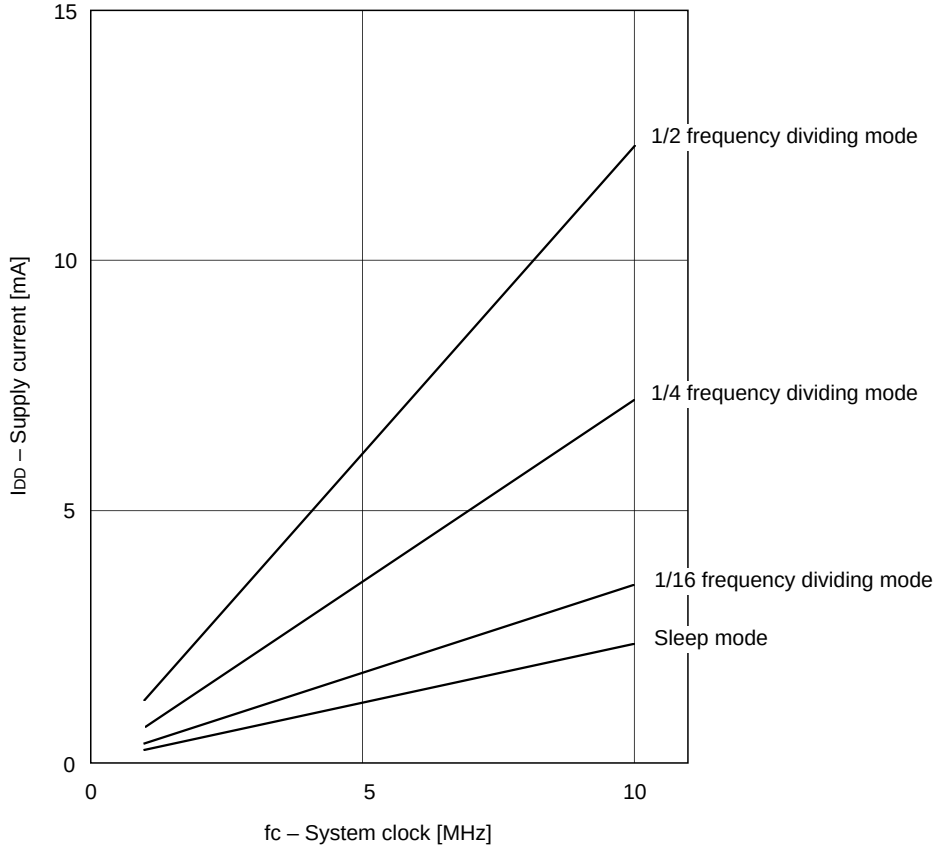
Item	Products												
	Mask										PROM		
	CXP 83508	CXP 83512	CXP 83516	CXP 83620	CXP 83624	CXP 83509	CXP 83513	CXP 83517	CXP 83621	CXP 83625	CXP836P60Q -1- □□□	CXP836P60R -1- □□□	CXP836P61Q -1- □□□
Package	80-pin plastic QFP/LQFP					0.65mm pitch 80-pin plastic QFP					80-pin plastic QFP	80-pin plastic LQFP	80-pin plastic QFP (0.65mm pitch)
ROM capacity	8K bytes	12K bytes	16K bytes	20K bytes	24K bytes	8K bytes	12K bytes	16K bytes	20K bytes	24K bytes	PROM 60K bytes		
$\overline{\text{RST}}$ pin pull-up resistor	Existent/Non-existent										Existent		

Characteristics Curve

IDD vs. VDD
(fc = 10MHz, Ta = 25°C, typical)



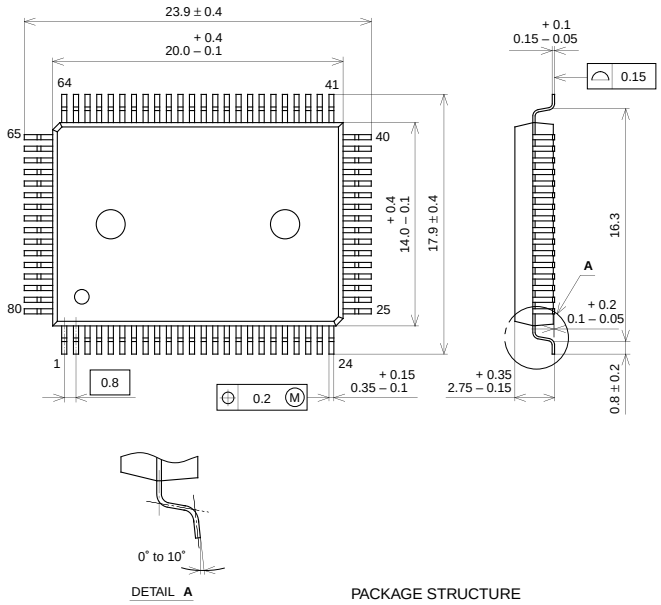
IDD vs. fc
(VDD = 5V, Ta = 25°C, typical)



Package Outline Unit: mm

80PIN QFP (PLASTIC)

CXP836P60



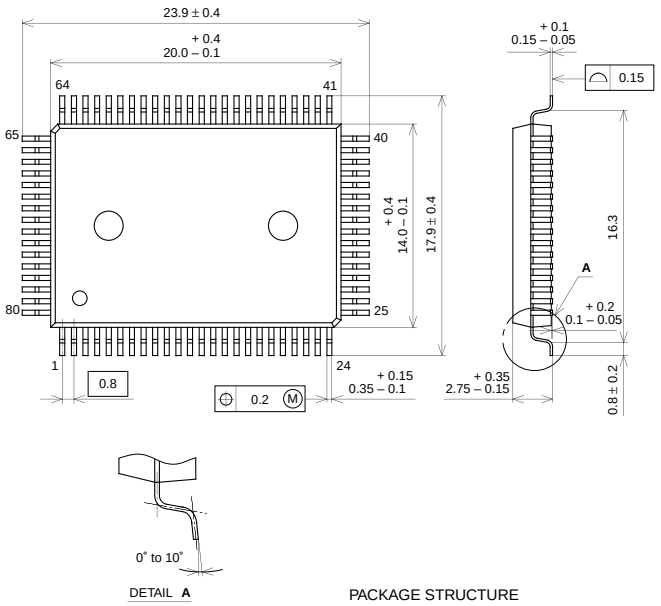
SONY CODE	QFP-80P-L01
EIAJ CODE	QFP080-P-1420
JEDEC CODE	————

PACKAGE STRUCTURE

PACKAGE MATERIAL	EPOXY RESIN
LEAD TREATMENT	SOLDER PLATING
LEAD MATERIAL	42/COPPER ALLOY
PACKAGE MASS	1.6g

CXP836P60

80PIN QFP (PLASTIC)



SONY CODE	QFP-80P-L01
EIAJ CODE	QFP080-P-1420
JEDEC CODE	————

PACKAGE STRUCTURE

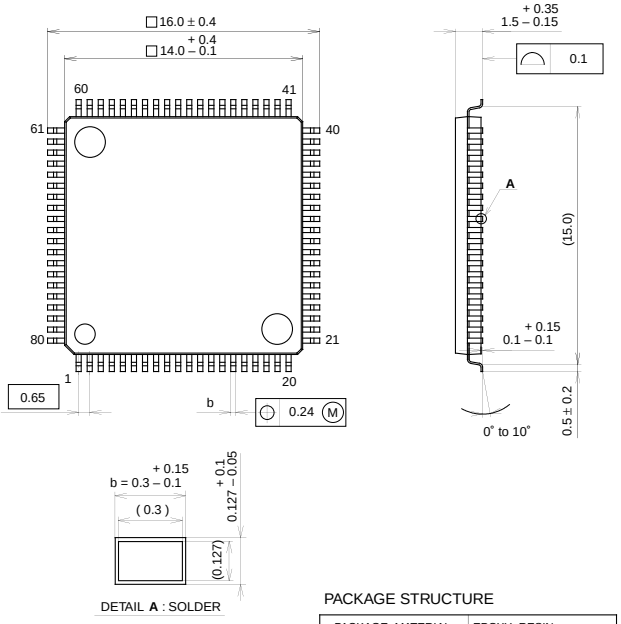
PACKAGE MATERIAL	EPOXY RESIN
LEAD TREATMENT	SOLDER PLATING
LEAD MATERIAL	42/COPPER ALLOY
PACKAGE MASS	1.6g

LEAD PLATING SPECIFICATIONS

ITEM	SPEC.
LEAD MATERIAL	42 ALLOY
SOLDER COMPOSITION	Sn-Bi Bi:1-4wt%
PLATING THICKNESS	5-18µm

Package Outline Unit: mm

CXP836P61 80PIN QFP (PLASTIC)

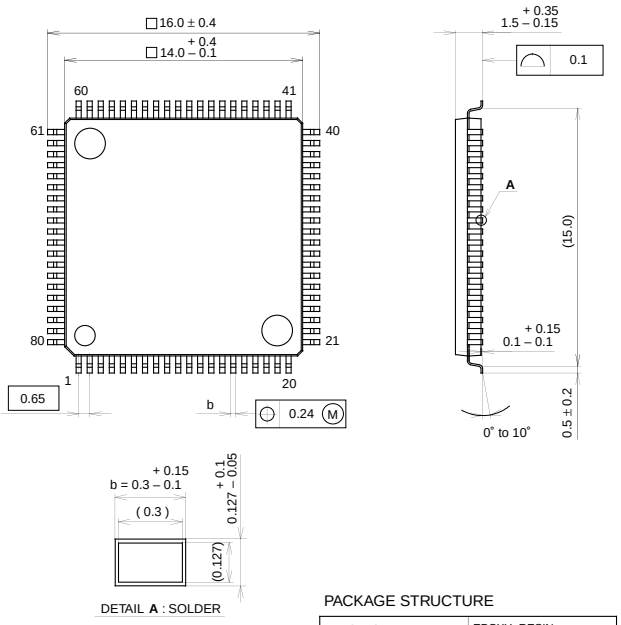


PACKAGE STRUCTURE

PACKAGE MATERIAL	EPOXY RESIN
LEAD TREATMENT	SOLDER PLATING
LEAD MATERIAL	42 / COPPER ALLOY
PACKAGE MASS	0.6g

SONY CODE	QFP-80P-L03
EIAJ CODE	P-QFP80-14x14-0.65
JEDEC CODE	————

CXP836P61 80PIN QFP (PLASTIC)



PACKAGE STRUCTURE

PACKAGE MATERIAL	EPOXY RESIN
LEAD TREATMENT	SOLDER PLATING
LEAD MATERIAL	42 / COPPER ALLOY
PACKAGE MASS	0.6g

SONY CODE	QFP-80P-L03
EIAJ CODE	P-QFP80-14x14-0.65
JEDEC CODE	————

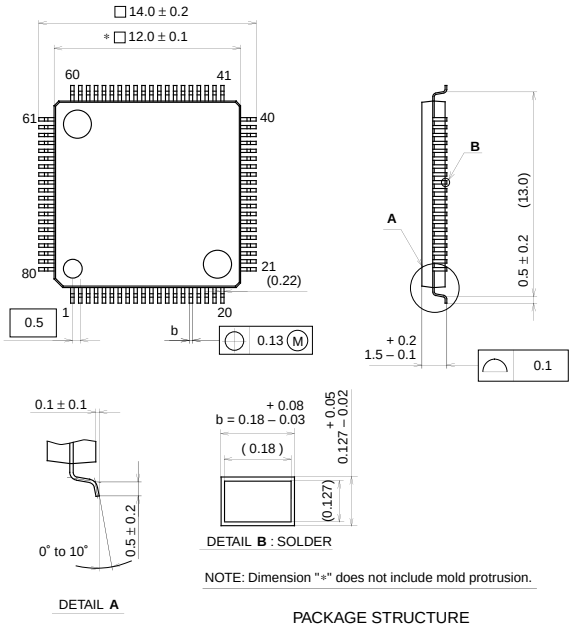
LEAD PLATING SPECIFICATIONS

ITEM	SPEC.
LEAD MATERIAL	42 ALLOY
SOLDER COMPOSITION	Sn-Bi Bi:1-4wt%
PLATING THICKNESS	5-18µm

Package Outline Unit: mm

80PIN LQFP (PLASTIC)

CXP836P60



NOTE: Dimension "∗" does not include mold protrusion.

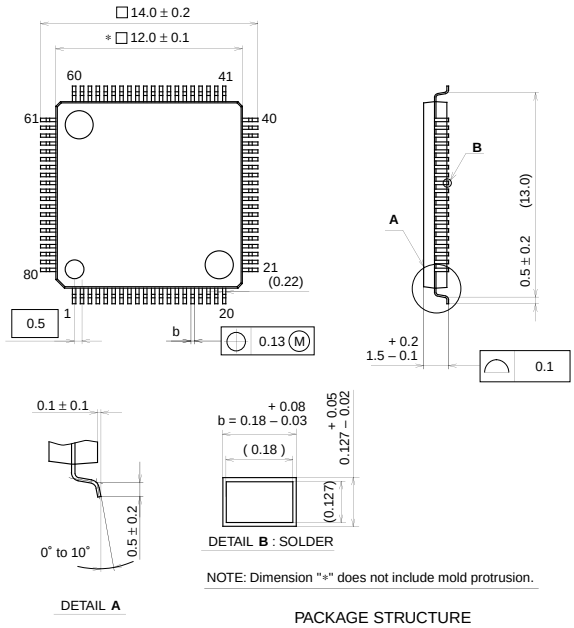
SONY CODE	LQFP-80P-L01
EIAJ CODE	P-LQFP80-12x12-0.5
JEDEC CODE	————

PACKAGE STRUCTURE

PACKAGE MATERIAL	EPOXY RESIN
LEAD TREATMENT	SOLDER PLATING
LEAD MATERIAL	42 / COPPER ALLOY
PACKAGE MASS	0.5g

80PIN LQFP (PLASTIC)

CXP836P60



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LEAD PLATING SPECIFICATIONS

ITEM	SPEC.
LEAD MATERIAL	42 ALLOY
SOLDER COMPOSITION	Sn-Bi Bi:1-4wt%
PLATING THICKNESS	5-18μm