TCP-3056N

5.6 pF Passive Tunable Integrated Circuits (PTIC)

ON Semiconductor®

http://onsemi.com

WLCSP12
1.18x0.72
CASE 567KE

QFN6
1.6x1.2
CASE 485DX

Introduction

ON Semiconductor's PTICs have excellent RF performance and power consumption, making them suitable for any mobile handset or radio application. The fundamental building block of our PTIC product line is a tunable material called ParaScan™, based on Barium Strontium Titanate (BST). PTICs have the ability to change their capacitance from a supplied bias voltage generated by the Control IC. The 5.6 pF PTICs are available as wafer-level chip scale packages (WLCSP) and in QFN packages for easy mounting directly on printed circuit boards.

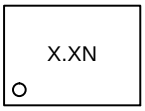
Key Features

- High Tuning Range and Operation up to 20 V
- Usable Frequency Range: from 700 MHz to 2.4 GHz
- High Quality Factor (Q) for Low Loss
- High Power Handling Capability
- Compatible with PTIC Control IC TCC-103
- WLCSP Package: 0.722 x 1.179 x 0.611 mm (12 pillar)
- QFN Package: 1.200 x 1.600 x 0.950 mm
- QFN: MSL−2 Moisture Sensitivity Level (per J−STD−020)
- These devices are Pb−Free and RoHS Compliant

Typical Applications

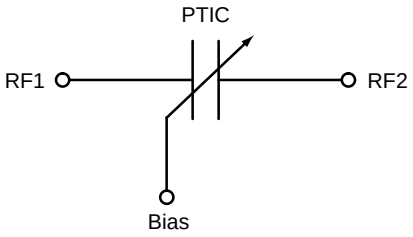
- Multi-band, Multi-standard, Advanced and Simple Mobile Phones
- Tunable Antenna Matching Networks
- Tunable RF Filters
- Active Antennas

MARKING DIAGRAM



X.X = 5.6
N = Normal Tuning

FUNCTIONAL BLOCK DIAGRAM



PTIC Functional Block Diagram

ORDERING INFORMATION

Device	Package	Shipping†
TCP−3056N−DT	WLCSP12 (Pb−Free)	4000 Units / 7" Reel
TCP−3056N−QT	QFN6 (Pb−Free)	8000 Units / 13" Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

TYPICAL SPECIFICATIONS

Representative Performance Data at 25°C

Table 1. PERFORMANCE DATA

Parameter	Min	Typ	Max	Units
Operating Bias Voltage	2.0		20	V
Capacitance (V_{bias} = 2 V)	4.82	5.60	6.16	pF
Capacitance (V_{bias} = 20 V)	1.52	1.60	1.68	pF
Tuning Range (2 V - 20 V)	3.00	3.50	4.05	
Tuning Range (20 V - 2 V)	2.80	3.30	4.05	
Leakage Current (WLCSP)			4.0	μA
Operating Frequency	700		2400	MHz
Quality Factor @ 700 MHz, 10 V		100		
Quality Factor @ 2.4 GHz, 10 V		65		
IP3 (V_{bias} = 2 V) [1,3]		70		dBm
IP3 (V_{bias} = 20 V) [1,3]		85		dBm
2nd Harmonic (V_{bias} = 2 V) [2,3]		−70		dBm
2nd Harmonic (V_{bias} = 20 V) [2,3]		−80		dBm
3rd Harmonic (V_{bias} = 2 V) [2,3]		−40		dBm
3rd Harmonic (V_{bias} = 20 V) [2,3]		−70		dBm
Transition Time (Cmin → Cmax) [4]		80		μs
Transition Time (Cmax → Cmin) [4]		70		μs

1. f_1 = 850 MHz, f_2 = 860 MHz, Pin 25 dBm/Tone
2. 850 MHz, Pin +34 dBm
3. IP3 and Harmonics are measured in the shunt configuration in a 50 Ω environment
4. RF1 and RF2 are both connected to DC ground

Representative performance data at 25°C for 5.6 pF WLCSP Package

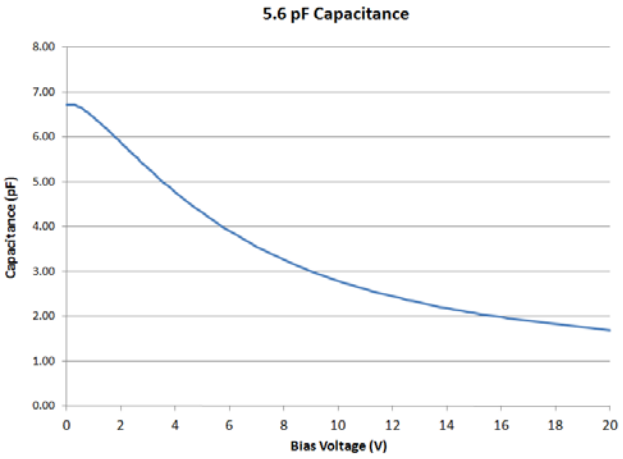


Figure 1. Capacitance

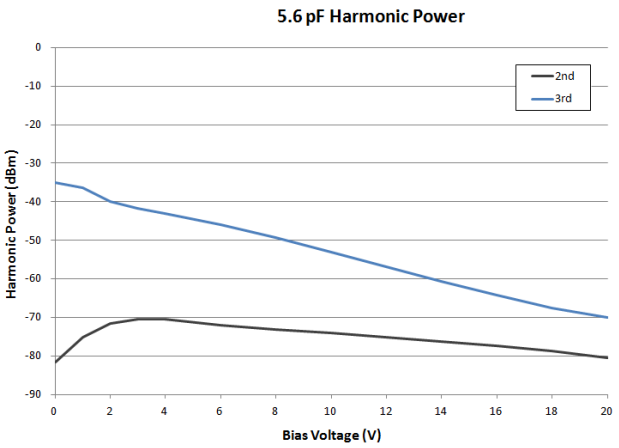


Figure 2. Harmonic Power

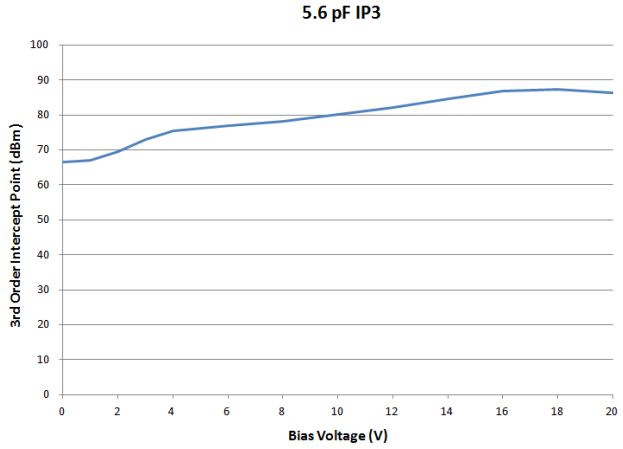


Figure 3. IP3

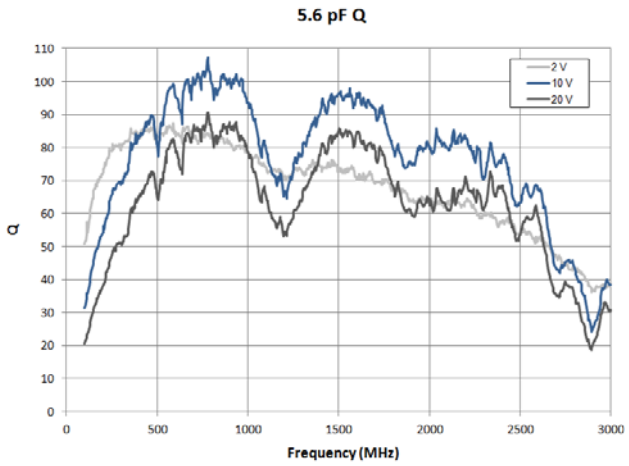


Figure 4. Q

Table 2. ABSOLUTE MAXIMUM RATINGS

Parameter	Rating	Units
Input Power	+40	dBm
Bias Voltage	+25 (Note 5)	V
Operating Temperature Range	−30 to +85	°C
Storage Temperature Range	−55 to +125	°C
ESD − Human Body Model	Class 1A JEDEC HBM Standard (Note 6)	

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

5. WLCSP: Recommended Bias Voltage not to exceed 20 V
6. Class 1A defined as passing 250 V, but may fail after exposure to 500 V ESD pulse

ASSEMBLY CONSIDERATIONS AND REFLOW PROFILE

The following assembly considerations should be observed:

Cleanliness

These chips should be handled in a clean environment.

Electro-static Sensitivity

ON Semiconductor's PTICs are ESD Class 1A sensitive. The proper ESD handling procedures should be used.

Mounting

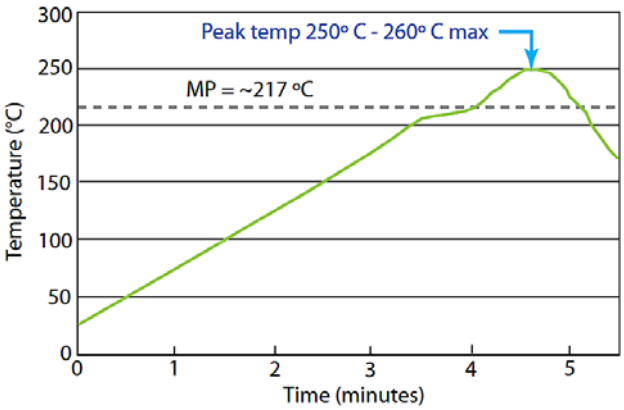
The WLCSP PTIC is fabricated for Flip Chip solder mounting. Connectivity to the RF and Bias terminations on the PTIC die is established through copper pillar posts (53 μm nominal height) topped with lead-free SAC351 solder caps (28 μm nominal height). The PTIC die is RoHS-compliant and compatible with lead-free soldering profile.

Post-reflow Cleaning

Use of ultrasonic cleaning is not recommended for pillared devices as it may lead to premature fatigue failure of the pillars.

Molding

The PTIC die is compatible for over-molding or under-fill.



This reflow profile is a guideline for Pb-free solder materials. Adjustments to this profile are necessary based on specific process requirements and board size, thickness and density.
Not to exceed 260° C for 5 seconds.

Figure 5. Reflow Profile

ORIENTATION OF THE PTIC FOR OPTIMUM LOSSES

When configuring the PTIC in your specific circuit design, at least one of the RF terminals must be connected to DC ground. If minimum transition times are required, DC ground on both RF terminals is recommended. To minimize losses, the PTIC should be oriented such that RF2 is at the lower RF impedance of the two RF nodes. A shunt PTIC, for example, should have RF2 connected to RF ground.

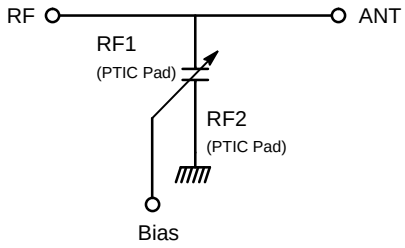


Figure 6. PTIC Orientation Functional Block Diagram

PART NUMBER DEFINITION

Example: TCP−3056N−DT

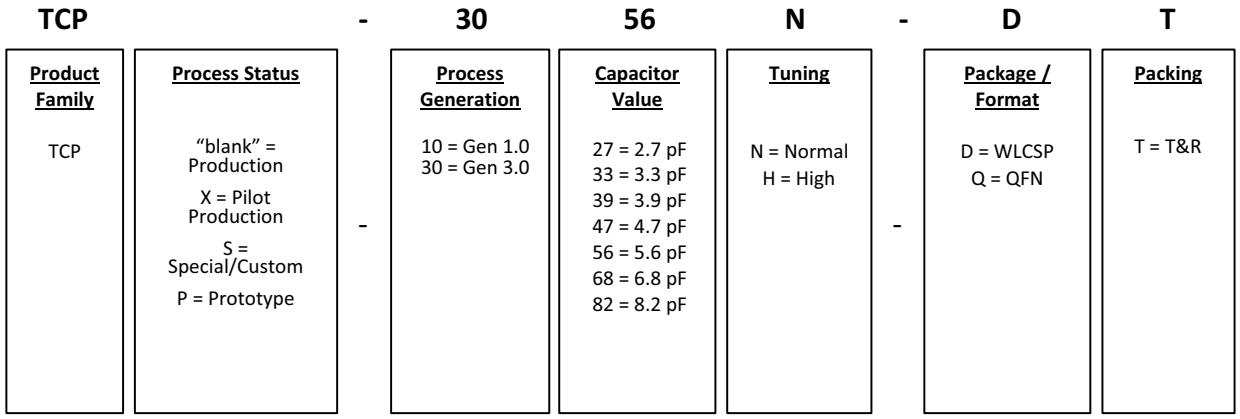
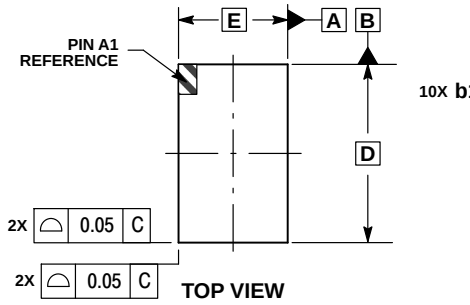


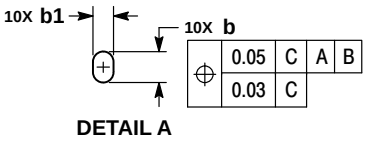
Table 3. PART NUMBERS

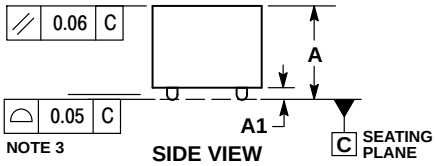
Part Number	Capacitance		Package
	2 V	20 V	
TCP-3056N-DT	5.60	1.60	12-Pillar WLCSP
TCP-3056N-QT	5.60	1.60	6-Pin QFN

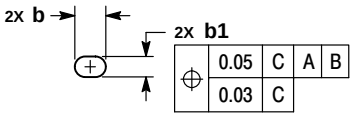
PACKAGE DIMENSIONS

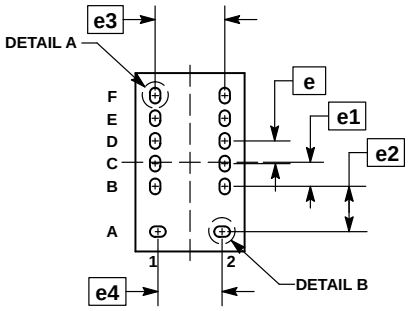
WLCSP12, 1.18x0.72
CASE 567KE
ISSUE O







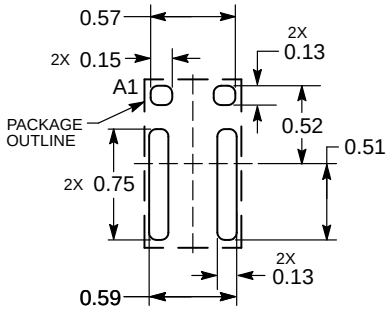




NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. COPLANARITY APPLIES TO SPHERICAL CROWNS OF SOLDER BALLS.

	MILLIMETERS	
DIM	MIN	MAX
A	0.590	0.639
A1	0.069	0.093
b	0.079	0.129
b1	0.044	0.094
D	1.179 BSC	
E	0.722 BSC	
e	0.150 BSC	
e1	0.159 BSC	
e2	0.300 BSC	
e3	0.460 BSC	
e4	0.425 BSC	

RECOMMENDED SOLDERING FOOTPRINT*

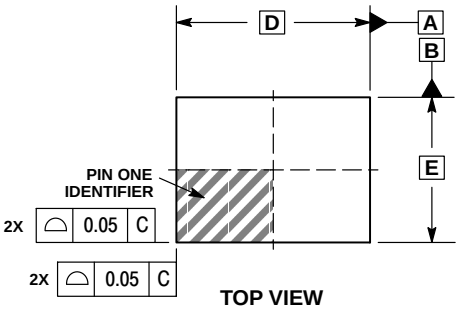


DIMENSIONS: MILLIMETERS

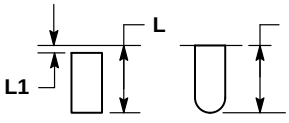
*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

PACKAGE DIMENSIONS

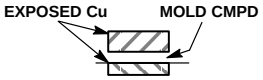
QFN6 1.6x1.2, 0.5P
CASE 485DX
ISSUE O



TOP VIEW



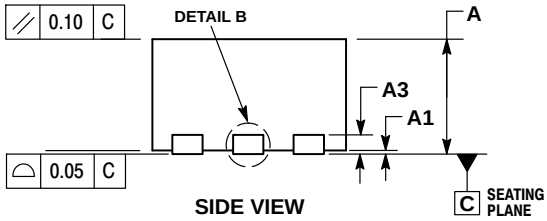
DETAIL A
ALTERNATE TERMINAL CONSTRUCTIONS



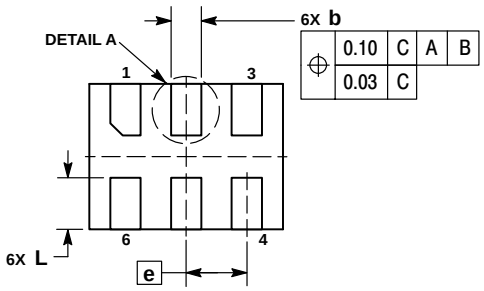
DETAIL B
ALTERNATE CONSTRUCTIONS

NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.

	MILLIMETERS	
DIM	MIN	MAX
A	0.90	1.00
A1	0.00	0.05
A3	0.15 REF	
b	0.22	0.28
D	1.60 BSC	
E	1.20 BSC	
e	0.50 BSC	
L	0.39	0.46
L1	−−−	0.15

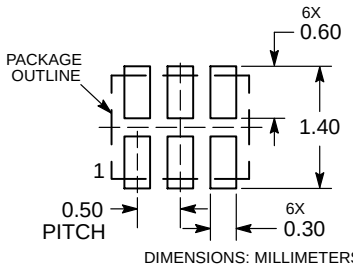


SIDE VIEW



BOTTOM VIEW

RECOMMENDED MOUNTING FOOTPRINT*



DIMENSIONS: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

ParaScan is a trademark of Paratek Microwave, Inc.

PUBLICATION ORDERING INFORMATION

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