Ordering number : ENA2324

LE24163LBXA

ON Semiconductor®

http://onsemi.com

CMOS LSI

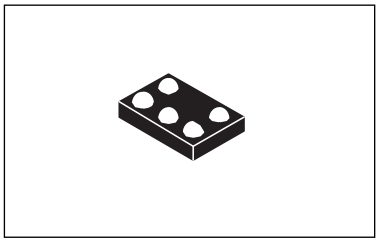
16 kb I²C CMOS Serial EEPROM

Overview

The LE24163LBXA (hereinafter referred to as 'this device') is two-wire serial interface EEPROM (Electrically Erasable and Programmable ROM). This device realizes high speed and a high level reliability by our company's high performance CMOS EEPROM technology. This device is compatible with I²C memory protocol, therefore it is best suited for application that requires re-writable nonvolatile parameter memory.

Function

- Capacity: 16k bits (2k x 8 bits)
- Single supply voltage: 1.7V to 3.6V (Read)
- Operating temperature: –40ºC to +85ºC
- Interface: Two wire serial interface (I²C Bus*)
- Operating clock frequency: 400kHz
- Low Power consumption
  : Standby: 2 µA (max.)
  : Active (Read): 0.5 mA (max.)
- Automatic page write mode: 16 Bytes
- Read mode: Sequential Read and random read
- Erase/Write cycles: 10^5 cycles (Page Write)
- Data Retention: 20 years
- Shipped Data Pattern: FFh
- High reliability: Adopts proprietary symmetric memory array configuration (USP6947325)
  Hardware write protect feature
  Noise filters connected to SCL and SDA pins
  Incorporates a feature to prohibit write operations under low voltage conditions.



WLCSP5, 1.20x0.80

Specifications

Absolute Maximum Ratings at Ta = 25°C

Parameter	Symbol	Conditions	Ratings	Unit
Supply voltage			–0.5 to +4.6	V
DC input voltage			–0.5 to VCC+0.5	V
Over-shoot voltage			–1.0 to VCC+1.0	V
Storage temperature	Tstg		–65 to +150	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

* This product is licensed from Silicon Storage Technology, Inc. (USA).

* I²C Bus is a trademark of Philips Corporation.

ORDERING INFORMATION

See detailed ordering and shipping information on page 15 of this data sheet.

Semiconductor Components Industries, LLC, 2014

Recommended Operating Conditions

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Operating supply voltage (Read)			1.7		3.6	V
Operating supply voltage (Write)			1.8		3.6	V
Operating temperature			−40		+85	°C

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

DC Electrical Characteristics

Parameter	Symbol	Conditions	Spec.			Unit
			min	typ	max	
Supply current at reading	$I_{CC}1$	f=400kHz, VDD = VDD Max			0.5	mA
Supply current at writing	$I_{CC}2$	f=400kHz, tWC=5ms, VDD = VDD Max			5	mA
Standby current	I_{SB}	V_{IN}=VDD or GND			2	μA
Input leakage current	I_{LI}	V_{IN}= GND to VDD, VDD = VDD Max	−2.0		+2.0	μA
Output leakage current	I_{LO}	V_{IN}= GND to VDD, VDD = VDD Max	−2.0		+2.0	μA
Input Low voltage	V_{IL}				VDD×0.2	V
Input High voltage	V_{IH}		VDD×0.8			V
Output Low voltage	V_{OL}	I_{OL}=0.7mA, VDD=1.7V			0.2	V
		I_{OL}=2.0mA, VDD=2.5V			0.4	V

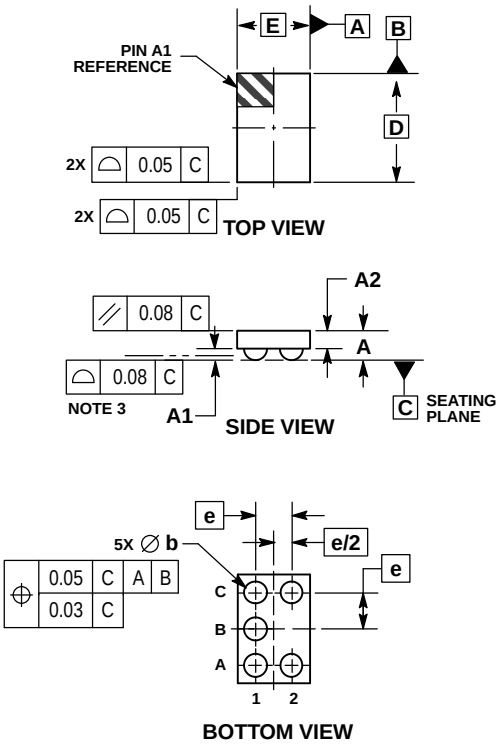
Capacitance at Ta = 25°C, f=1MHz

Parameter	Symbol	Conditions	max	Unit
In/Output pin capacitance	$C_{I/O}$	$V_{I/O}$=0V (SDA)	6	pF
Input pin capacitance	C_I	V_{IN}=0V	6	pF

Package Dimensions

unit : mm

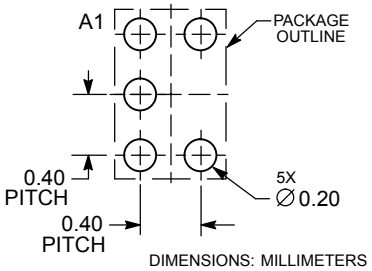
WLCSP5, 1.20x0.80
CASE 567GS
ISSUE O



NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. COPLANARITY APPLIES TO SPHERICAL CROWNS OF SOLDER BALLS.

	MILLIMETERS	
DIM	MIN	MAX
A	---	0.33
A1	0.03	0.13
A2	0.20 REF	
b	0.15	0.25
D	1.20 BSC	
E	0.80 BSC	
e	0.40 BSC	

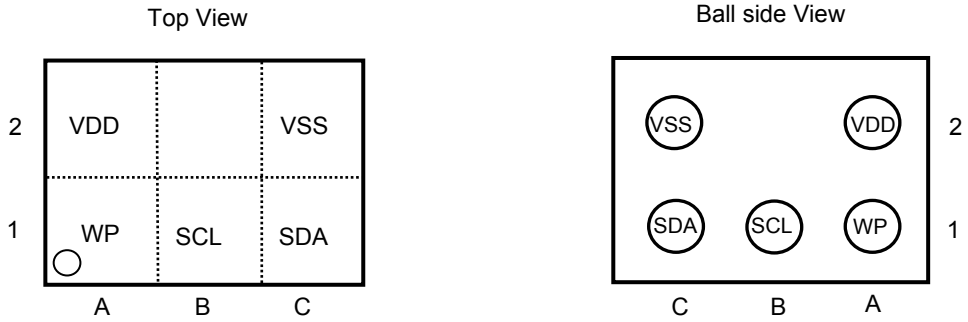
RECOMMENDED SOLDERING FOOTPRINT*



DIMENSIONS: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

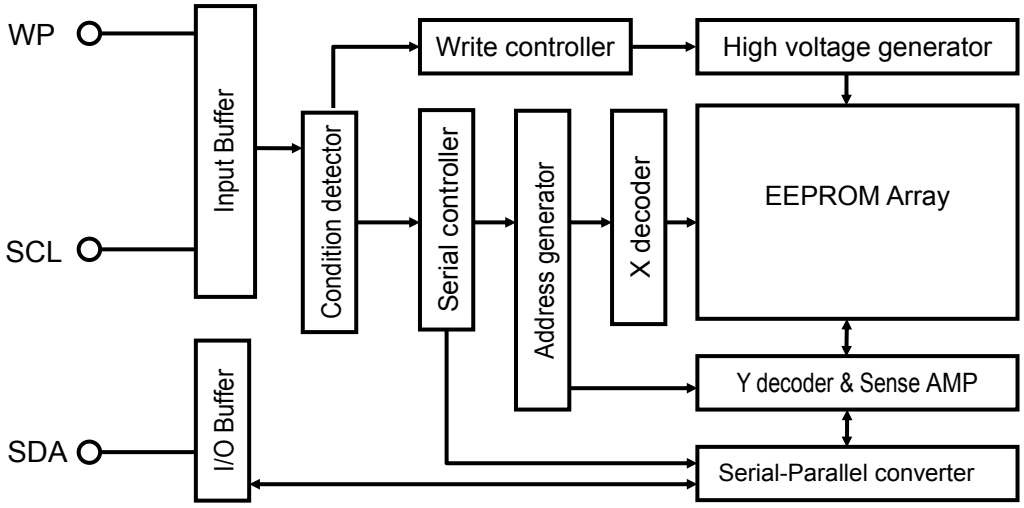
Pin Assignment



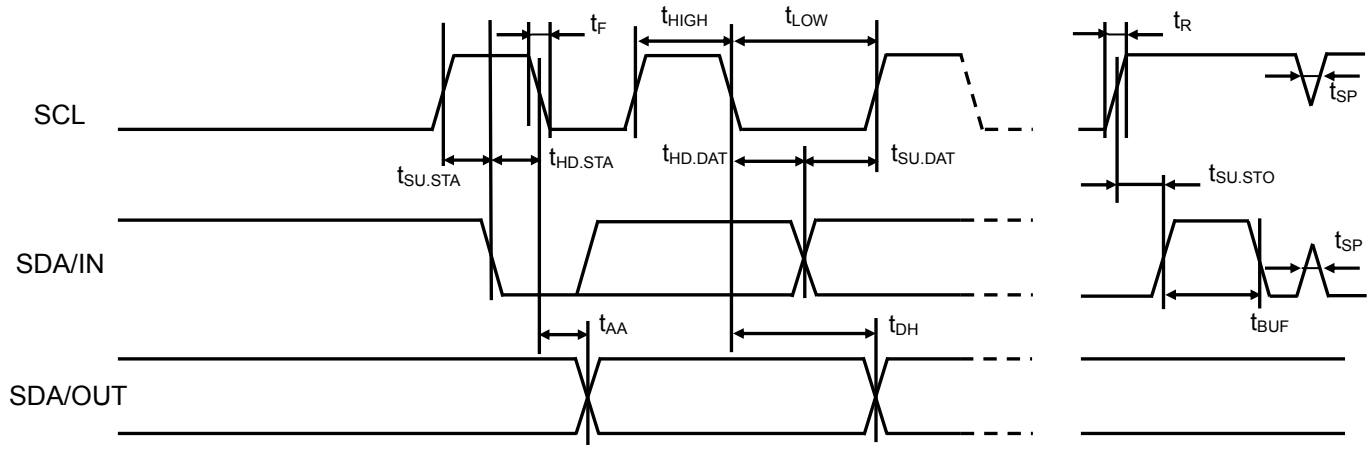
Pin Descriptions

A1	WP	Write protect
A2	VDD	Power supply
B1	SCL	Serial clock input
B2	-	-
C1	SDA	Serial data in/output
C2	VSS	Ground

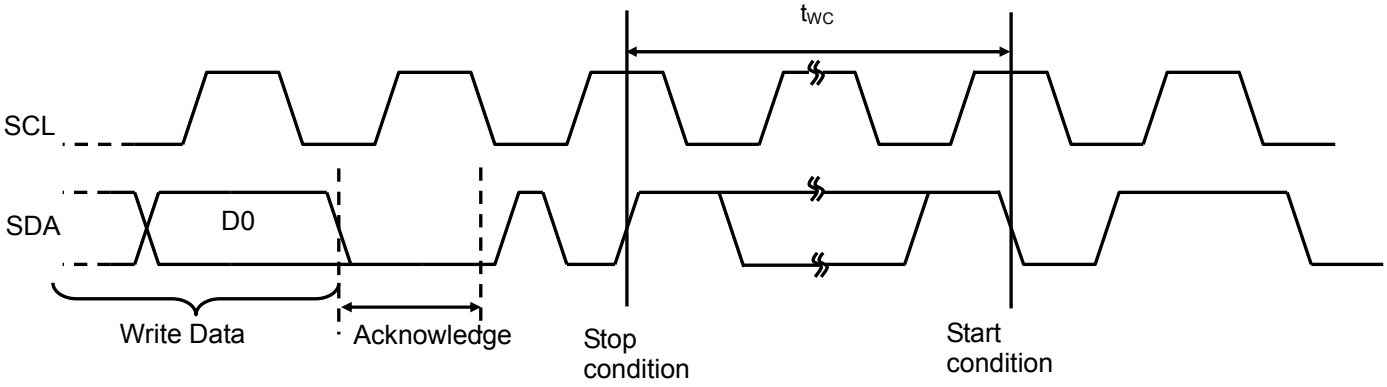
Block Diagram



Bus timing



Write timing



Pin Function

SCL (Serial clock)

The SCL signal is used to control serial input data timing. The SCL is used to latch input data synchronously at the rising edge and read output data synchronously at the falling edge.

SDA (Serial input / output data)

The SDA pin is bidirectional for serial data transfer. It is an open-drain structure that needs to be pulled up by resistor.

WP (Write protect)

When the WP input is high, write protection is enabled. When WP input is either low or floating, write protection is disabled. The read operation is always activated irrespective of the WP pin status.

Functional Description

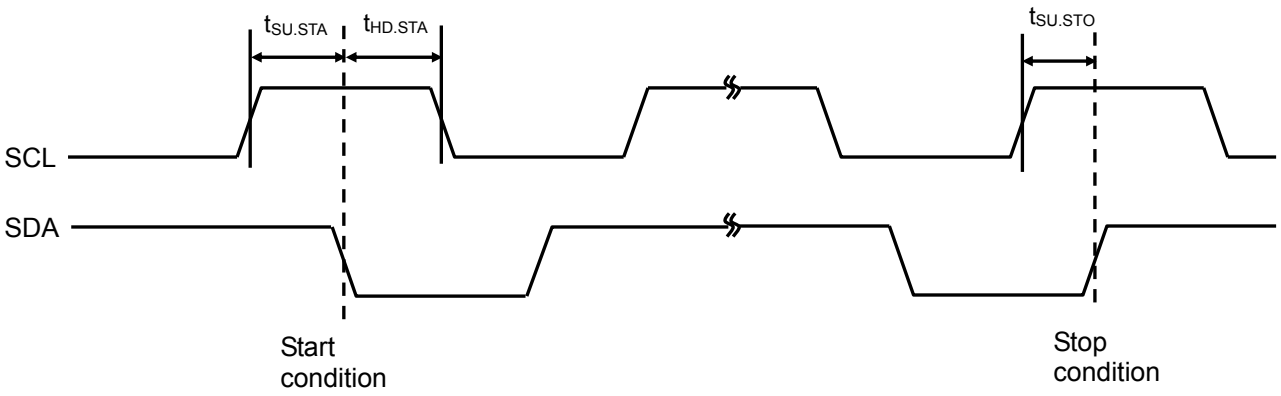
The device supports the I^2C protocol. Any device that sends data on to the bus is defined to be a transmitter, and any device that reads the data to a receiver. The device that controls the data transfer is known as the bus master, and the other as the slave device.

1) Start Condition

A Start condition needs to start the EEPROM operation, it is to set falling edge of the SDA while the SCL is stable in the high status.

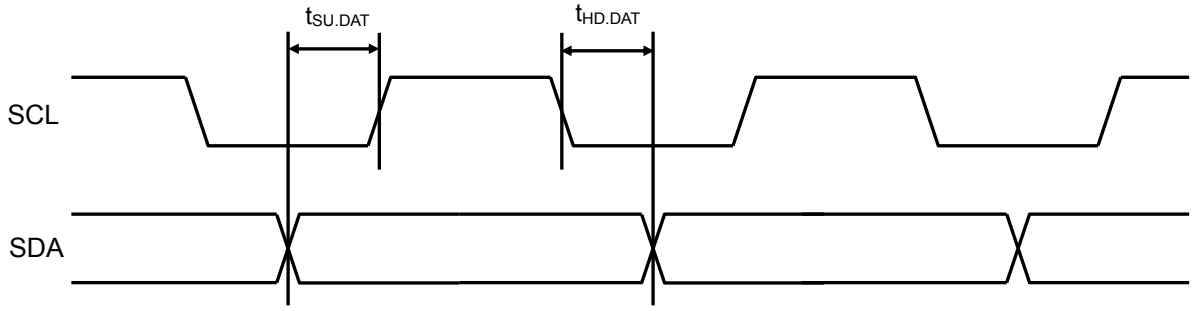
2) Stop Condition

A Start condition is identified by rising edge of the SDA signal while the SCL is stable in the high status. The device becomes the standby mode from a Read operation by a Stop condition. In a write sequence, a stop condition is trigger to terminate the write data inputs and it is trigger to start the internal write cycle. After the internally write cycle time which is specified as tWC, the device enters a standby mode.



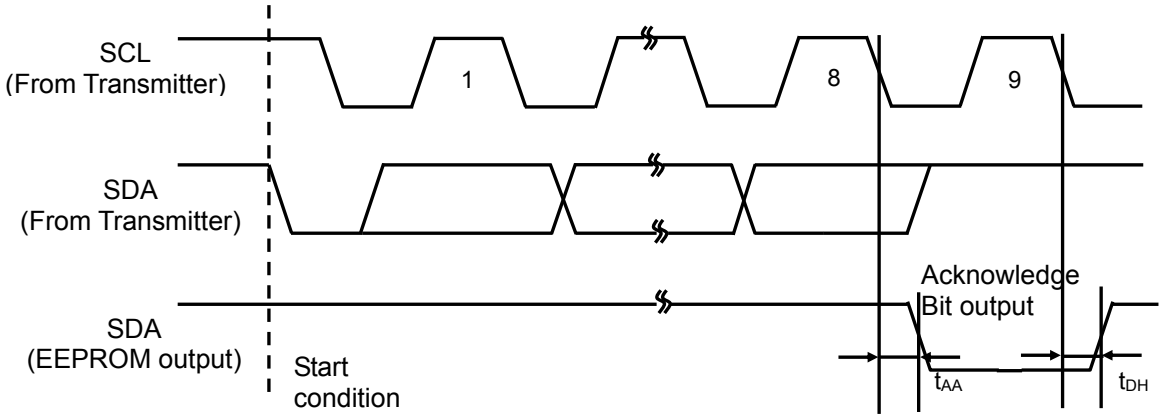
3) Data Input

During data input, the device latches the SDA on the rising edge of the SCL. For correct the operation, The SDA must be stable during the rising edge of the SCL.



4) Acknowledge Bit (ACK)

The Acknowledge Bit is used to indicate a successful byte data transfer. The receiver sends a zero to acknowledge that it has received each word (Device Code, Slave Address etc) from the transmitter.

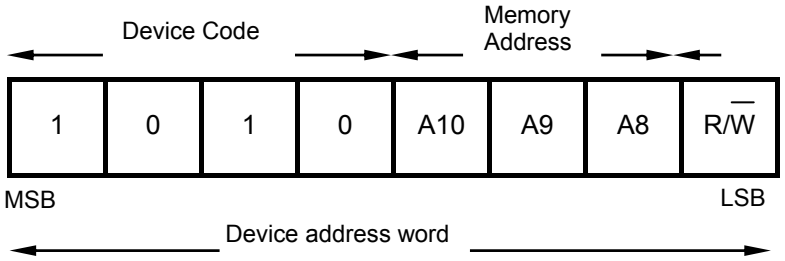


5) Device addressing

To transmit between the bus master and slave device (EEPROM), the master must send a Start condition to the EEPROM. The device address word of the EEPROM consists of 7-bit Device address code and 1-bit read/write code. By sending these, it becomes possible to communicate between the bus master and the EEPROM.

The upper 4-bit of the device address word are called the Device Code, the Device Code of the EEPROM uses 1010b fixed code. This device does not have the Slave address.

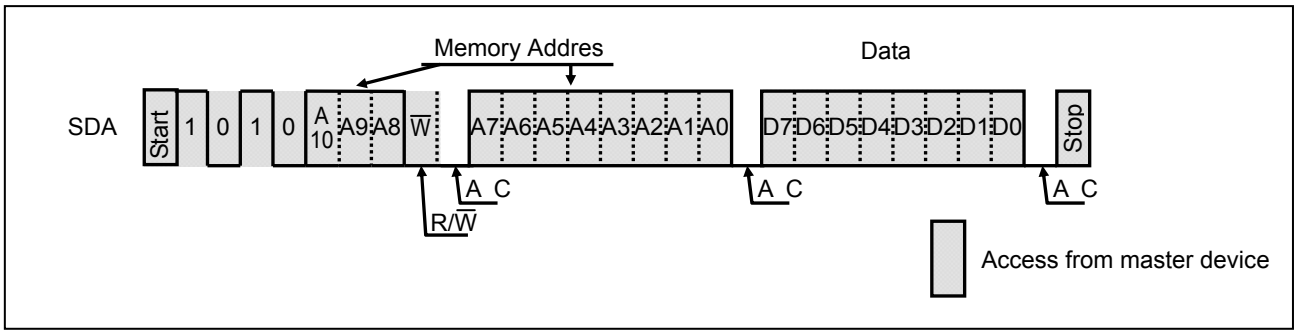
The 8th bit is the read/write bit. The bit is set to 1 for Read operation and 0 for Write operation. If a match occurs on the Device Code, the corresponding device gives an acknowledgement on SDA during the 9th bit time. If device dose not match the Device Code, it deselects itself from the bus, and goes into the Standby mode. Use the Random Read command when you execute reading after the slave device was switched.



6) EEPROM Write Operation

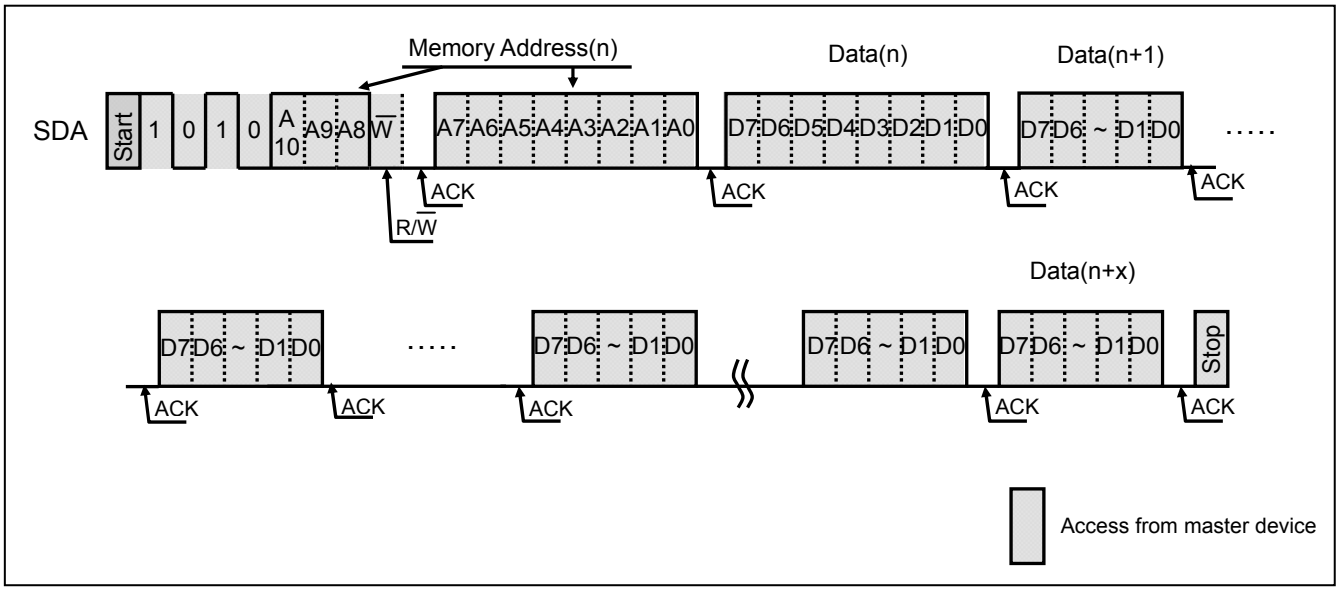
6)-1. Byte Write

The write operation requires an 8-bit device address word with the 8th bit = 0 (write). Then the EEPROM sends acknowledgement 0 at the 9th clock cycle. After these, the EEPROM receives 8-bit memory address word, and the EEPROM outputs acknowledgement 0 at receipt of this memory address. Then the EEPROM receives 8-bit write data, the EEPROM outputs acknowledgement 0 after receipt of write data. If the EEPROM receives a stop condition, the EEPROM enters an internally timed (tWC) write cycle and terminates receipt of inputs until completion of the write cycle.



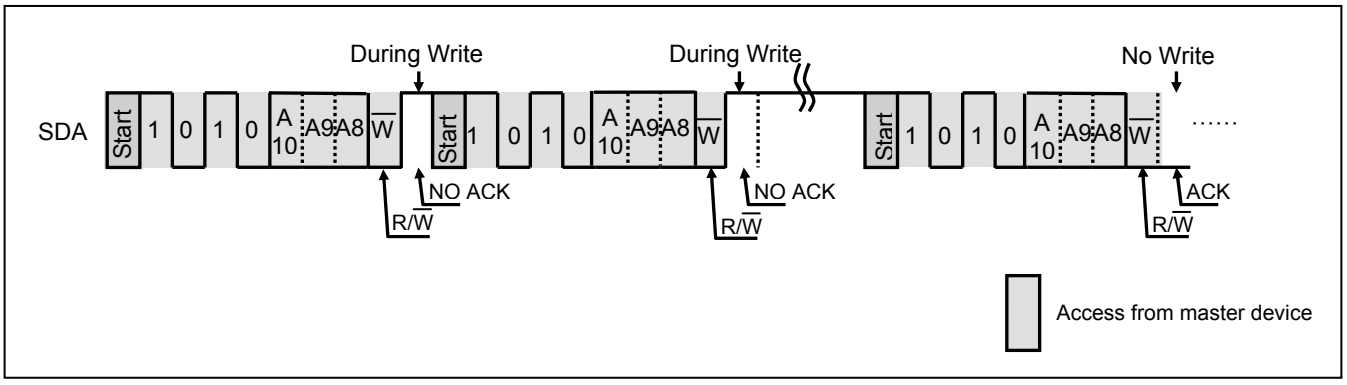
6)-2. Page Write

The Page write allows up to 16 bytes to be written in a single write cycle. The page write is the same sequence as the byte write except for inputting the more write data. The page write is initiated by a start condition, device code, device address, memory address(n) and write data(n) with every 9th bit acknowledgement. The device enters the page write operation if this device receives more write data(n+1) instead of receiving a stop condition. The page address (A0 to A3) bits are automatically incremented on receiving write data(n+1). The device can continue to receive write data up to 16 bytes. If the page address bits reaches the last address of the page, the page address bits will roll over to the first address of the same page and previous write data will be overwritten. After these, if the device receives a stop condition, the device enters an internally timed (tWC×(n+x)) write cycle and terminates receipt of inputs until completion of the write cycle.



6)-3. Acknowledge Polling

The Acknowledge Polling operation is used to show if the EEPROM is in an internally timed write cycle or not. This operation is initiated by the stop condition after inputting write data. This requires the 8-bit device address word with the 8th bit = 0 (write) following the start condition during an internally timed write cycle. If the EEPROM is busy with the internal write cycle, no acknowledge will be returned. If the EEPROM has terminated the internal write cycle, it responds with an acknowledge. The terminated write cycle of the EEPROM can be known by this operation.

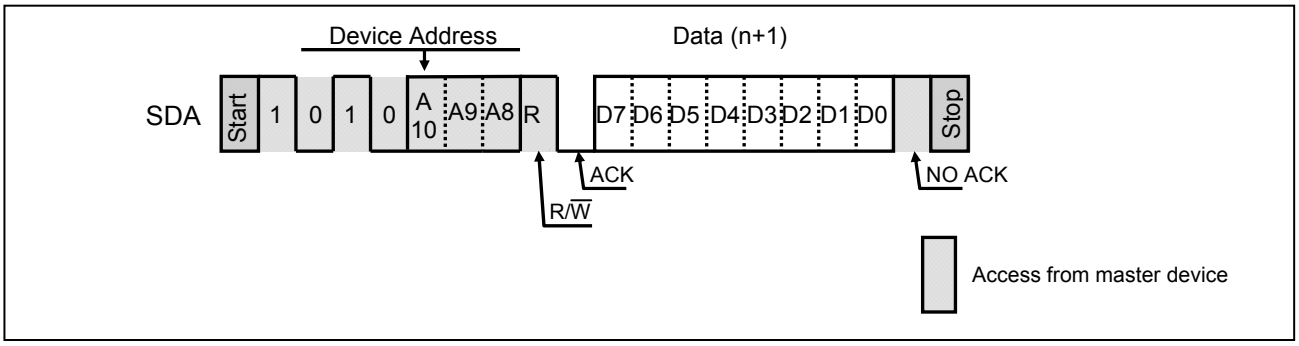


7) EEPROM Read Operation

7)-1. Current Address Read

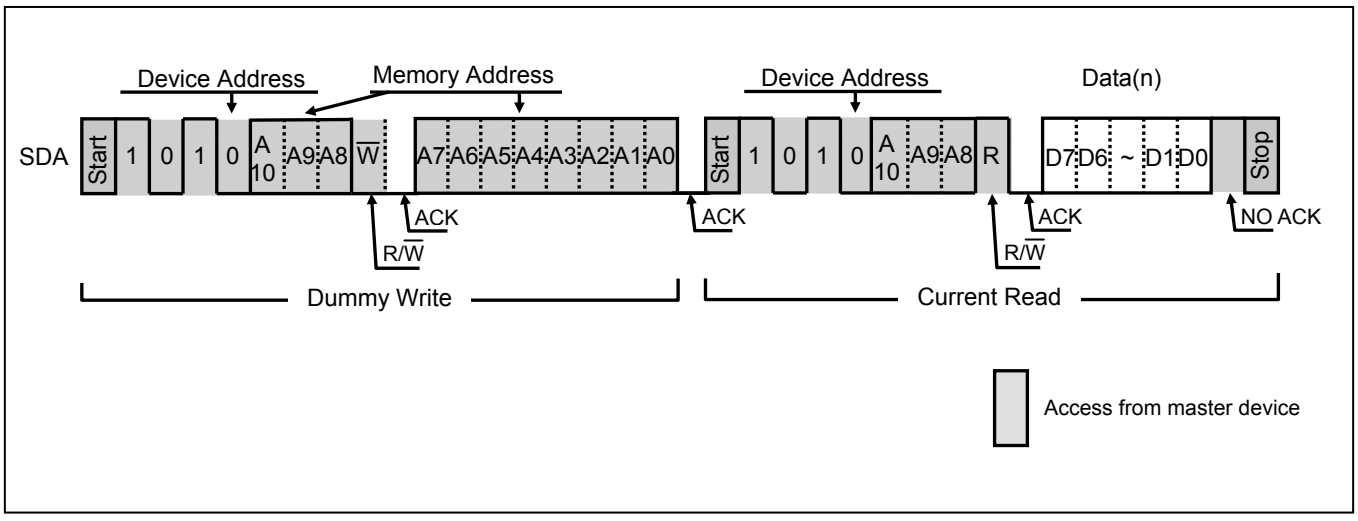
The device has an internal address counter. It maintains that last address during the last read or write operation, with incremented by one. The current address read accesses the address kept by the internal address counter. After receiving a start condition and the device address word with the 8th bit = 1 (Read), the EEPROM outputs the 8-bit current address data from following acknowledgement 0. If the EEPROM receives acknowledgement 1 and a following stop condition, the EEPROM stops the read operation and is returned to a standby mode. In case the EEPROM has accessed the last address of the last page at previous read operation, the current address will roll over and returns to zero address. In case EEPROM has accessed tha last address of the last page at previous write operation, the current address roll over within page addressing and returns to the first address in the same page.
The current address is valid while power is on. After power on, the current address will be reset (all 0).

Note: After the page write operation, the current address is the specified memory address in the last page write, if the write data is more than 16-bytes.



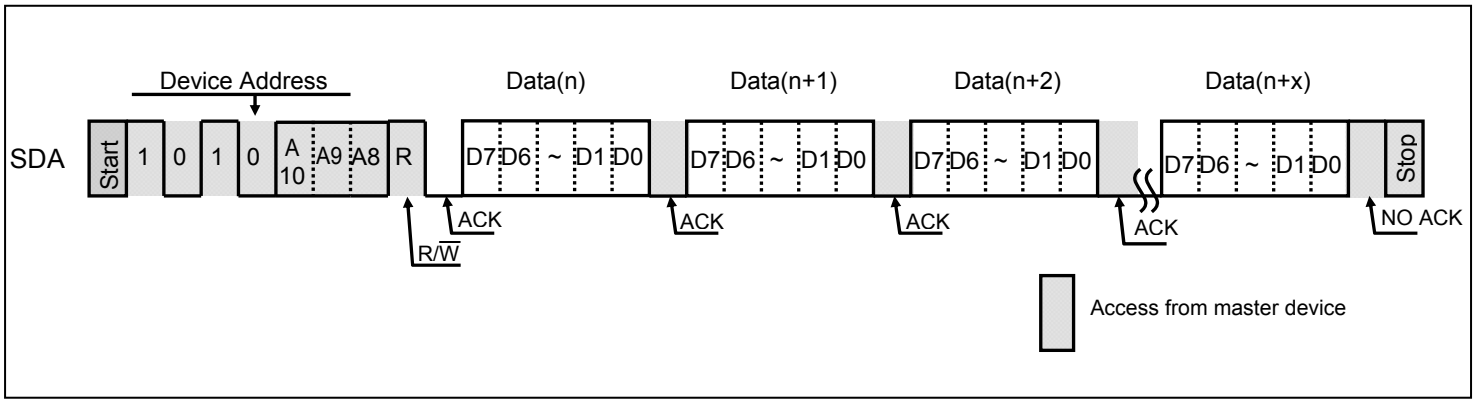
7)-2. Random Read

The random read requires a dummy write to set read address. The EEPROM receives a start condition and the device address word with the 8th bit = 0 (write), the memory address. The EEPROM outputs acknowledgement 0 after receiving memory address then enters a current address read with receiving a start condition. The EEPROM outputs the read data of the address which was defined in the dummy write operation. After receiving no acknowledgement and a following stop condition, the EEPROM stops the random read operation and returns to a standby mode.



7)-3. Sequential Read

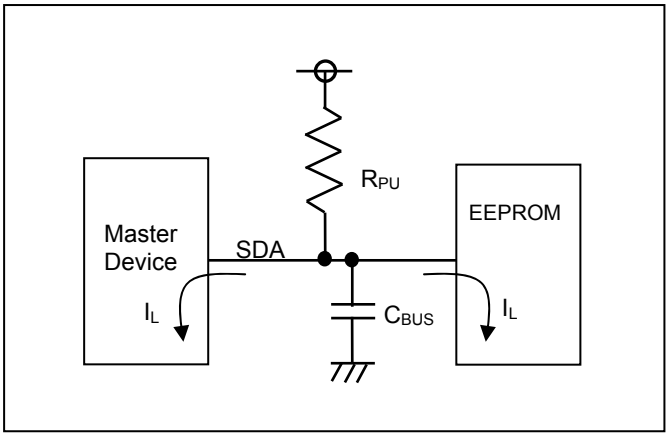
The sequential read operation is initiated by either a current address read or random read. If the EEPROM receives acknowledgement 0 after 8-bit read data, the read address is incremented and the next 8-bit read data outputs. The current address will not roll over and returns address zero if it reaches the last address of the last page. Please don't access it except the valid address range (000h ~ 7FFh). The sequential read is terminated if the EEPROM receives no acknowledgement and a following stop condition.



Application Notes

1) Pull-up resistor of SDA pin

Due to the demands of the I^2C bus protocol function, the SDA pin must be connected to a pull-up resistor (with a resistance from several kΩ to several tens of kΩ) without fail. The appropriate value must be selected for this resistance (R_{PU}) on the basis of the V_{IL} and I_{IL} of the microcontroller and other devices controlling this product as well as the $V_{OL} – I_{OL}$ characteristics of the product. Generally, when the resistance is too high, the operating frequency will be restricted; conversely, when it is too low, the operating current consumption will increase.



R_{PU} maximum value

The maximum resistance must be set in such a way that the bus potential, which is determined by the sum total (I_L) of the input leaks of the devices connected to the SDA bus and by R_{PU}, can completely satisfy the input high level (V_{IH} min) of the microcontroller and EEPROM. However, a resistance value that satisfies SDA rise time tR and fall time tF must be set.

R_{PU} maximum value = $(VCC - V_{IH})/I_L$

Example: When VCC = 3.0 V and I_L = 2 μA
R_{PU} maximum value = $(3.0\ V - 3.0\ V \times 0.8)/2\ \mu A = 300\ k\Omega$

R_{PU} minimum value

A resistance corresponding to the low-level output voltage (V_{OL} max) of EEPROM must be set.

R_{PU} minimum value = $(VCC - V_{OL})/I_{OL}$

Example: When VCC = 3.0 V, V_{OL} = 0.4 V and I_{OL} = 1 mA
R_{PU} minimum value = $(3.0\ V - 0.4)/1\ mA = 2.6\ k\Omega$

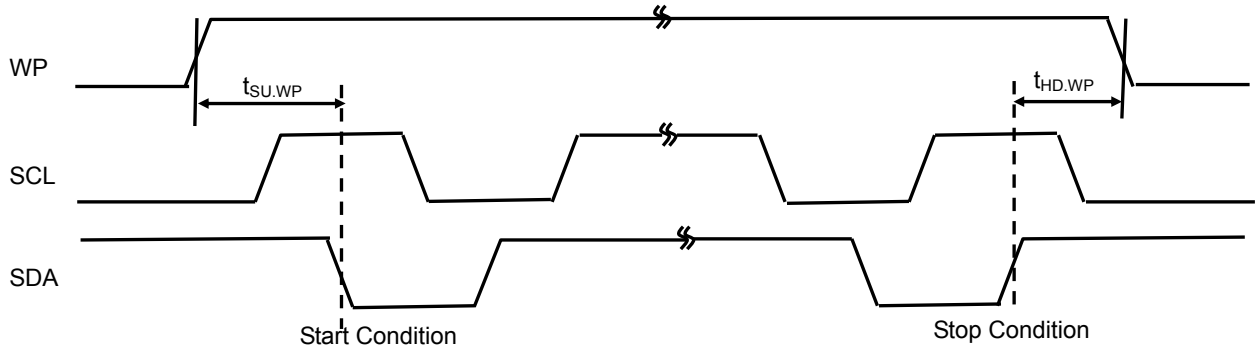
Recommended R_{PU} setting

R_{PU} is set to strike a good balance between the operating frequency requirements and power consumption. If it is assumed that the SDA load capacitance is 50 pF and the SDA output data strobe time is 500 ns, R_{PU} will be about R_{PU} = 500 ns/50 pF = 10 kΩ.

2) Notes on write protect operation

This product prohibits all memory array writing when the WP pin is high. To ensure full write protection, the WP is set high for all periods from the start condition to the stop condition, and the conditions below must be satisfied.

symbol	Parameter	Spec.			Unit
		Min.	Typ.	Max.	
$t_{SU.WP}$	WP Setup time	600	–	–	ns
$t_{HD.WP}$	WP Hold time	600	–	–	ns



3) Noise filter for the SCL and SDA pins

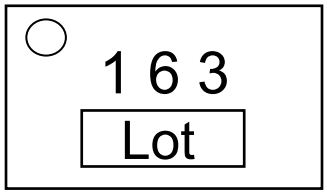
This product contains a filter circuit for eliminating noise at the SCL and SDA pins. Pulses of 100 ns or less are not recognized because of this function.

4) Function to inhibit writing when supply voltage is low

This product contains a supply voltage monitoring circuit that inhibits inadvertent writing below the guaranteed operating supply voltage range. The data is protected by ensuring that write operations are not started at voltages (typ.) of 1.3 V and below.

MARKING INFORMATION

LE24163LBXA WLCSP5, 1.20x0.80



Part ID: 163
Lot Number: 3digits

ORDERING INFORMATION

Device	Package	Shipping (Qty / Packing)
LE24163LBXA-SH	WLCSP5, 1.20x0.80 (Pb-Free / Halogen Free)	5000 / Tape & Reel

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